

QUADRATURE CLOCK CONVERTER

June 2015

FEATURES:

- x1 and x4 mode selection
- Up to 16MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +3V to +12V operation ($V_{DD} - V_{SS}$)
- **LS7083N, LS7084N** (DIP);
- **LS7083NS, LS7084NS** (SOIC) - See Figure 1

Applications:

- Interface incremental encoders to Up / Down Counters (See Figure 6A and Figure 6B)
- Interface rotary encoders to Digital Potentiometers (See Figure 7)

DESCRIPTION:

The **LS7083N** and **LS7084N** are CMOS quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the **LS7083N** or **LS7084N**, are converted to strings of Up Clocks and Down Clocks (**LS7083N**) or to a Clock and an Up/Down direction control (**LS7084N**). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

RBIAS (Pin 1)

Input for external component connection. A resistor connected between this input and V_{SS} adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A, B pulse separation ($TOW \leq T_{PS}$).

V_{DD} (Pin 2)

Supply Voltage positive terminal.

V_{SS} (Pin 3)

Supply Voltage negative terminal.

A (Pin 4)

Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

B (Pin 5)

Quadrature Clock Input B. This input has a filter circuit identical to input A.

Mode (Pin 6)

Mode is a 3-state input to select resolutions x1, x2 or x4. The selected resolution multiplies the input quadrature clock rate by 1, 2 and 4, respectively, in producing the outputs \overline{UPCK} / \overline{DNCK} and CLK (see Figure 2).

The Mode input logic levels selects resolutions as follows:

Logic 0 = x1 Float = x2 Logic 1 = x4

PIN ASSIGNMENT - TOP VIEW

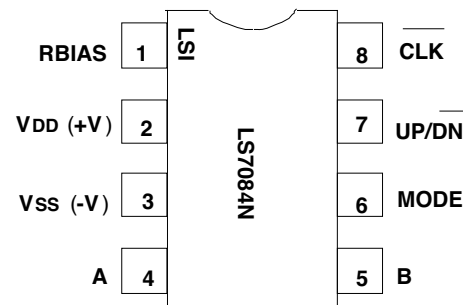
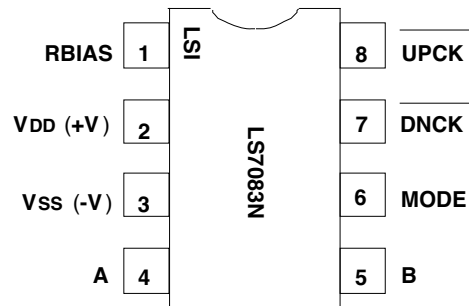


FIGURE 1

LS7083N - \overline{DNCK} (Pin 7)

In **LS7083N**, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

LS7084N - $\overline{UP/DN}$ (Pin 7)

In **LS7084N**, this is the count direction indication output. When A input leads the B input, the $\overline{UP/DN}$ output goes high indicating that the count direction is UP. When A input lags the B input, $\overline{UP/DN}$ output goes low, indicating that the count direction is DOWN.

LS7083N - \overline{UPCK} (Pin 8)

In **LS7083N**, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

LS7084N - CLK (Pin 8)

In **LS7084N**, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the $\overline{UP/DN}$ output (Pin 7).

NOTE: For the **LS7084N**, the timing of \overline{CLK} and $\overline{UP/DN}$ requires that the counter interfacing with **LS7084N** counts on the rising edge of the CLK pulses.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	$V_{DD} - V_{SS}$	16	V
Voltage at any input	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating temperature	T_A	-20 to +85	°C
Storage temperature	T_{STG}	-55 to 150	°C

DC ELECTRICAL CHARACTERISTICS: (Unless otherwise specified $V_{DD} = 3V$ to $12V$ and $T_A = -20^\circ C$ to $+85^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITION
Supply Voltage	V_{DD}	3	-	12	V	-
Supply Current	I_{DD}	-	1.5	1.65	mA	$V_{DD} = 12V$, all input frequencies=0 Hz and $R_{BIAS} = 2M\Omega$

MODE INPUT:

Logic 0	V_{ml}	-	-	0.5	V	-
Logic 1	V_{mh}	$V_{DD} - 0.5$	-	-	V	-
Logic Float	V_{mf}	$(V_{DD}/2) - 0.5$	$V_{DD}/2$	$(V_{DD}/2) + 0.5$	V	-
Logic 0 Input Current	I_{ml}	-	2.2	4.2	μA	$V_{DD} = 3V$
	I_{ml}	-	3.5	6.9	μA	$V_{DD} = 5V$
	I_{ml}	-	8.3	16.2	μA	$V_{DD} = 12V$
Logic 1 Input Current	I_{mh}	-	-2	-9.8	μA	$V_{DD} = 3V$
	I_{mh}	-	-3.4	-6.6	μA	$V_{DD} = 5V$
	I_{mh}	-	-8.2	-16	μA	$V_{DD} = 12V$

A,B INPUTS:

Logic 0	V_{ABl}	-	-	$0.25V_{DD}$	V	-
Logic 1	V_{ABh}	$0.7V_{DD}$	-	-	V	-
Input Current	I_{ABlk}	-	0	10	nA	-

RBIAS INPUT:

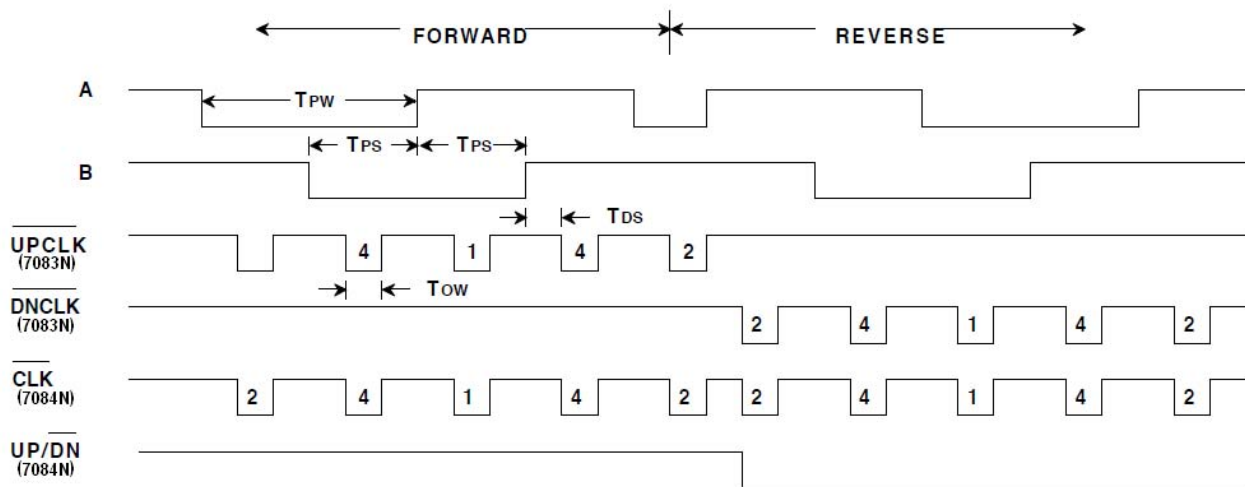
External Resistor	R_B	2K	-	10M	Ω	-
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ALL OUTPUTS:

Sink Current	I_{ol}	-	-3.2	-	mA
	I_{ol}	-	-4.8	-	mA
	I_{ol}	-	-7.2	-	mA
Source Current	I_{oh}	-	1.7	-	mA
	I_{oh}	-	2.2	-	mA
	I_{oh}	-	3.1	-	mA

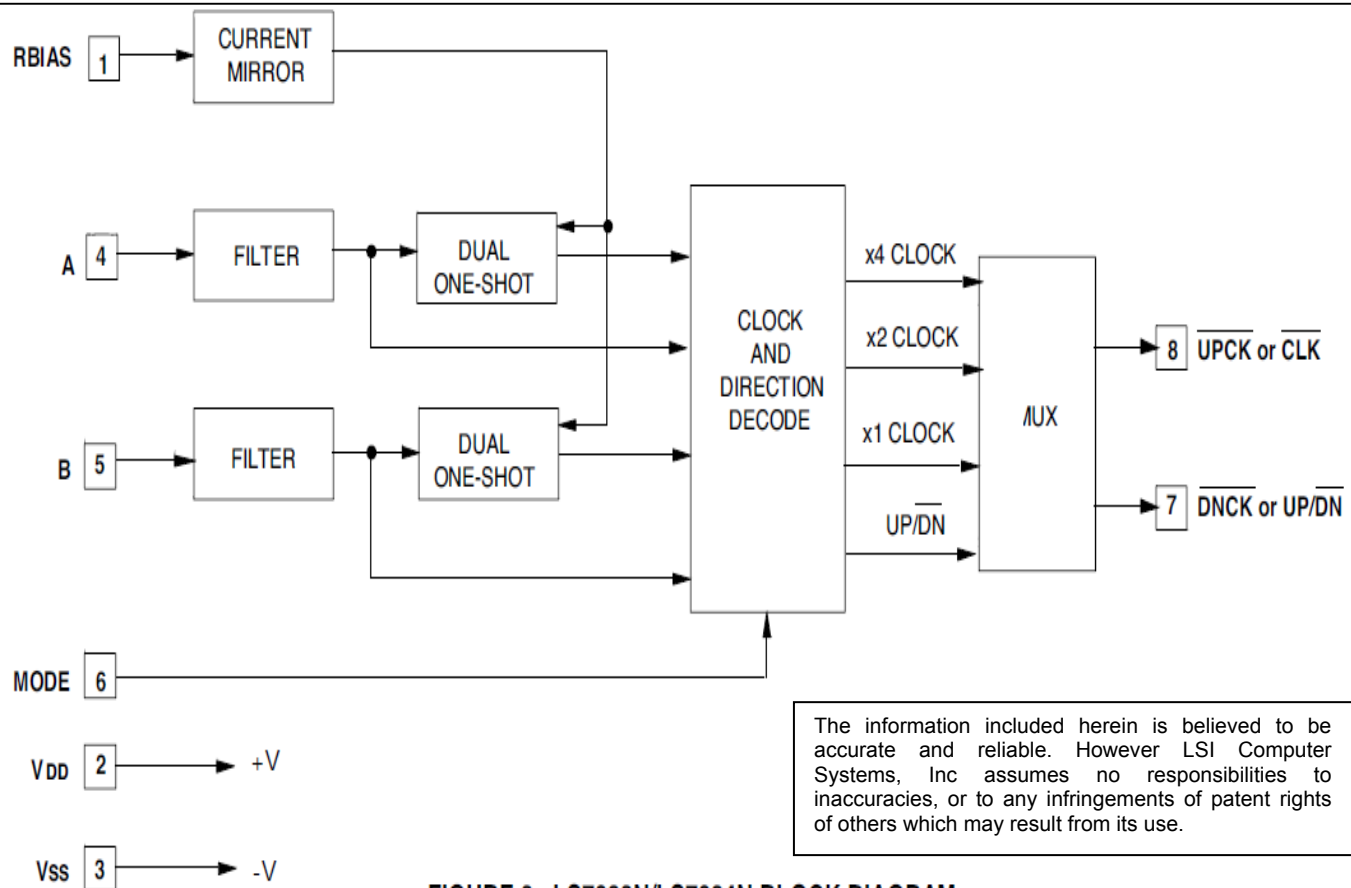
TRANSIENT CHARACTERISTICS ($T_A = -20^\circ C$ to $+85^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITION
Output Clock Pulse Width	T_{OW}	540	-	-	ns	$V_{DD} = 3V$
	T_{OW}	180	-	-	ns	$V_{DD} = 5V$
	T_{OW}	60	-	-	ns	$V_{DD} = 12V$
A,B INPUTS: Validation Delay	T_{VD}	-	450	-	-	$V_{DD} = 3V$
	T_{VD}	-	200	-	-	$V_{DD} = 5V$
	T_{VD}	-	90	-	-	$V_{DD} = 12V$
Phase Delay	T_{PS}	$T_{VD}+T_{OW}$	-	∞	s	-
Pulse Width	T_{PW}	$2T_{PS}$	-	∞	s	-
Frequency	$f_{A,B}$	-	-	$1/(2T_{PW})$	Hz	-
Input to output Delay	T_{DS}	-	490	565	ns	$V_{DD} = 3V$
	T_{DS}	-	220	345	ns	$V_{DD} = 5V$
	T_{DS}	-	125	135	ns	$V_{DD} = 12V$



NOTE: Output clocks labeled 1, 2 and 4 have the following interpretations.
 1: Generated in x1, x2 and x4 modes
 2: Generated in x2 and x4 modes only
 4: Generated in x4 mode only

FIGURE 2. LS7083N / LS7084N INPUT / OUTPUT TIMING



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FIGURE 3. LS7083N/LS7084N BLOCK DIAGRAM

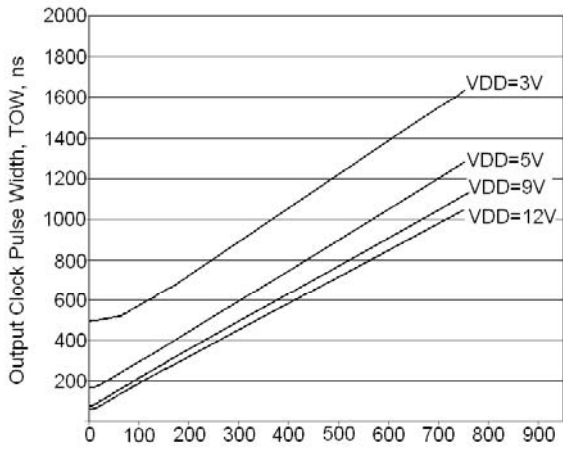


Figure 4. T_{OW} vs. R_{BIAS} (R in KΩ)

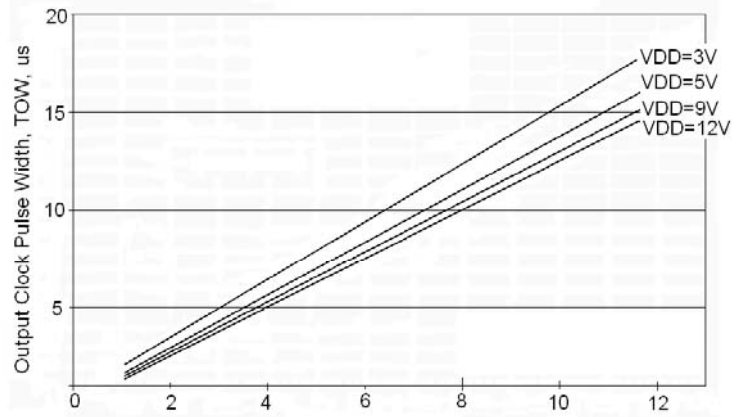


Figure 5. T_{OW} vs. R_{BIAS} (R in MΩ)

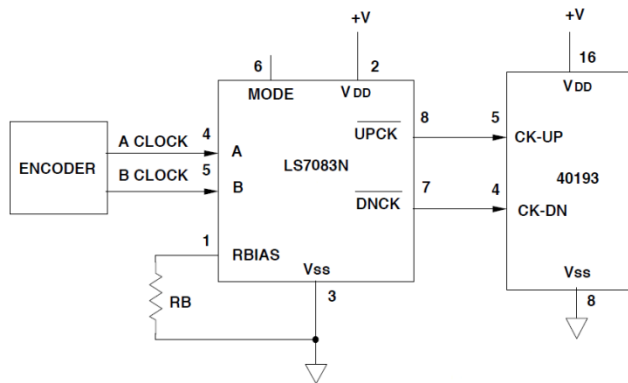


Figure 6A. Typical application for 7083N in x4 mode

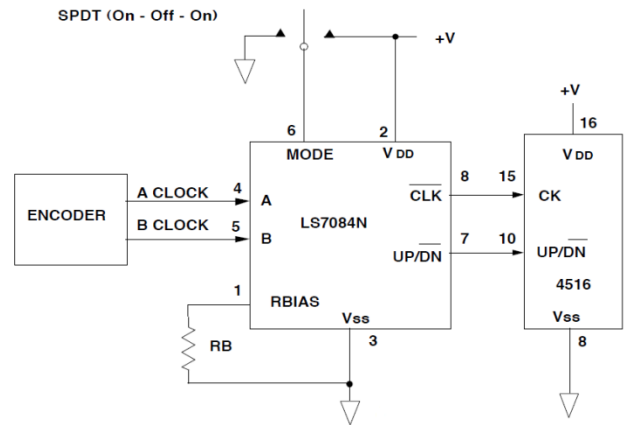


Figure 6B. Typical application for LS7084N in x2 mode

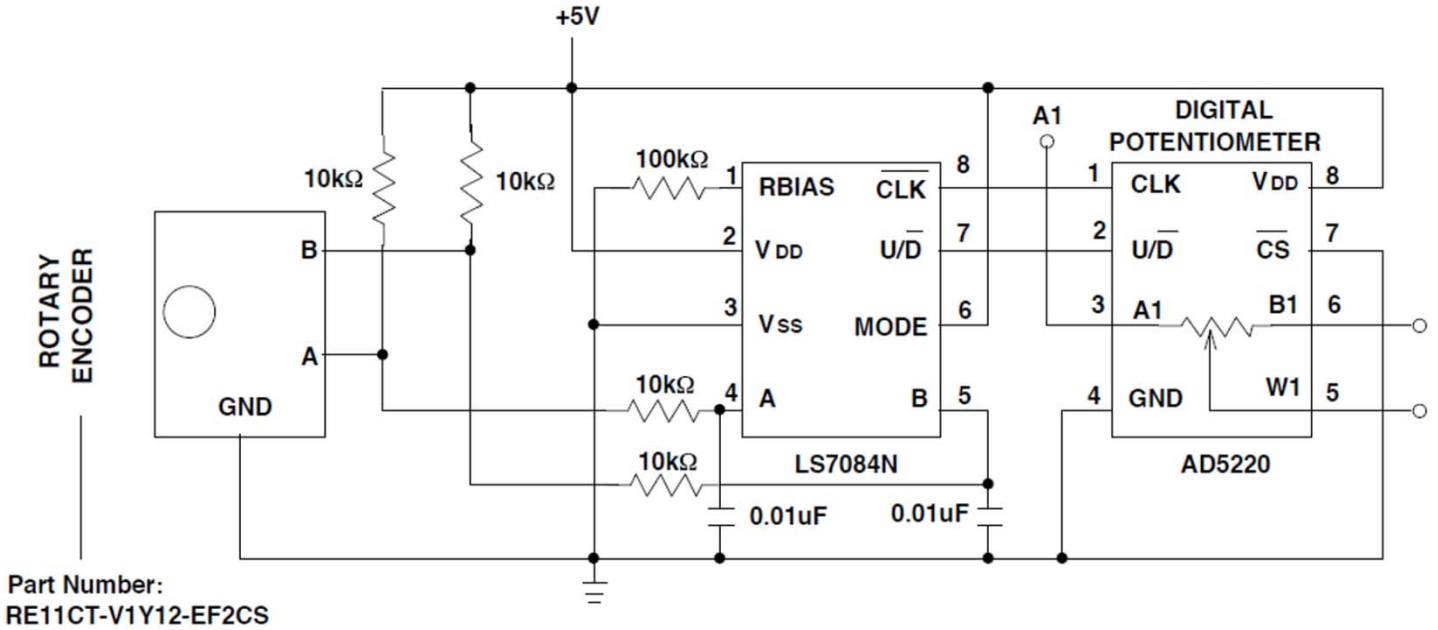


Figure 7. Rotary encoder control of digital potentiometer