CD74FCT157T, CD74FCT257T, CD74FCT2157T, CD74FCT2257T

December 1996

Fast CMOS Quad 2-Input Multiplexers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor On All Outputs (FCT2XXX Only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs (25Ω Series Only)**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT157TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157DTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157DTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT157ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT157CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT157DTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT257TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT257ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT257CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2157TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2157ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2157CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2257TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2257ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2257CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

These devices are high-speed quad 2-input multiplexers. The common select input can be used to select four bits of data from two sources. The four buffered outputs present the selected data in the true (non-inverting) form.

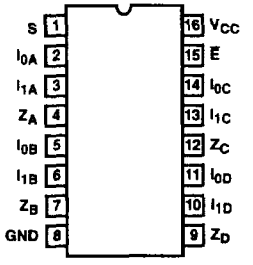
The CD74FCT157T and CD74FCT2157T have a common, active-LOW, Enable input ($\overline{E}$). When $\overline{E}$ is inactive, all four outputs are held LOW. The CD74FCT157T and CD74FCT2157T can generate any four of the 16 different funtions of two variables with one common variable. They can be used as a function generator or to move data from two different groups of registers to a common bus.

The CD74FCT257T and CD74FCT2257T have a common Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

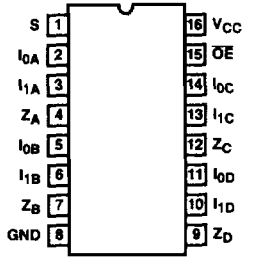
The CD74FCT2157T and CD74FCT2257T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinout

CD74FCT157T, 7CD74FCT2157T
(QSOP, SOIC)
TOP VIEW



CD74FCT257T, 7CD74FCT2257T
(QSOP, SOIC)
TOP VIEW



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OCTAL 5V FCT
5V FCT 25Ω

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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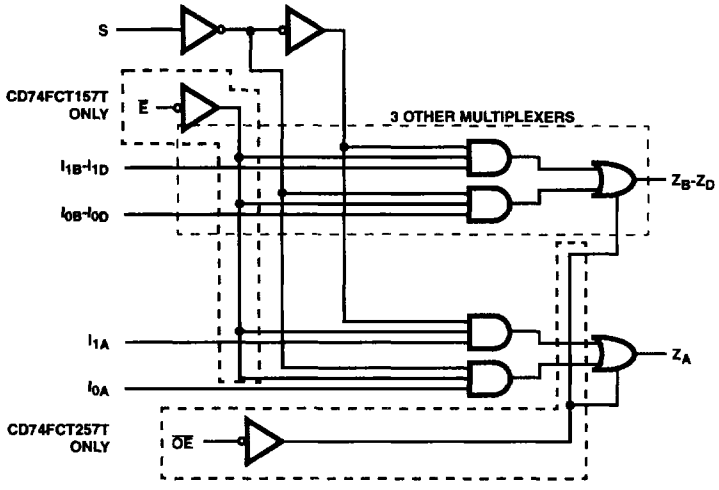
File Number **4166.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS Z_N	
$\overline{E}/\overline{OE}$	S	I0	I1	CD74FCT157T, CD74FCT2157T	CD74FCT257T, CD74FCT2257T
H	X	X	X	L	Z
L	H	X	L	L	L
L	H	X	H	H	H
L	L	L	X	L	L
L	L	H	X	H	H

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
I_{0A}-I_{0D}	Source 0 Data Inputs
I_{1A}-I_{1D}	Source 1 Data Inputs
$\overline{E}$	Enable Input (Active LOW) CD74FCT157T, CD74FCT2157T
$\overline{OE}$	Output Enable (Active LOW) CD74FCT257T,CD74FCT2257T
S	Select Input
Z_A-Z_D	Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	97
QSOP Package	140

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
	I_{OZL}		V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 9)	
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND Four Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	
			V_{IN} = 3.4V V_{IN} = GND	-	2.5	7.5 (Note 9)	

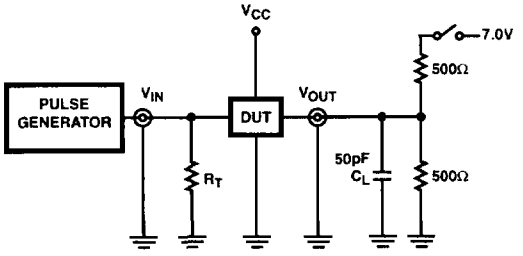
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	(CD74FCT157T ONLY) DT (NOTE 12) MIN	(CD74FCT157T ONLY) DT MAX	UNITS
CD74FCT157T, CD74FCT2157T											
Propagation Delay In to Z_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.0	1.5	4.3	1.5	3.9	ns
Propagation Delay $\overline{E}$ to Z_N	t_{PLH}, t_{PHL}		1.5	10.5	1.5	6.0	1.5	4.8	1.5	4.4	ns
Propagation Delay S to Z_N	t_{PLH}, t_{PHL}		1.5	10.5	1.5	7.0	1.5	5.2	1.5	4.6	ns
CD74FCT257T, CD74FCT2257T											
Propagation Delay In to Z_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.0	1.5	4.3	-	-	ns
Propagation Delay S to Z_N	t_{PLH}, t_{PHL}		1.5	10.5	1.5	7.0	1.5	5 2	-	-	ns
Output Enable Time $\overline{OE}$ to Z_N	t_{PZH}, t_{PZL}		1.5	8.5	1.5	7.0	1.5	6.0	-	-	ns
Output Disable Time $\overline{OE}$ to Z_N (Note 13)	t_{PZH}, t_{PZL}		1.5	6.0	1.5	5.5	1.5	5.0	-	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. *Not more than one output should be shorted at one time. Duration of the test should not exceed one second.*
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. *This parameter is guaranteed but not production tested.*

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

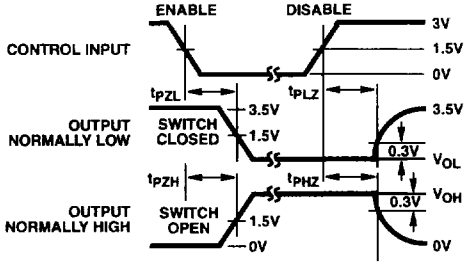


FIGURE 2. ENABLE AND DISABLE TIMING

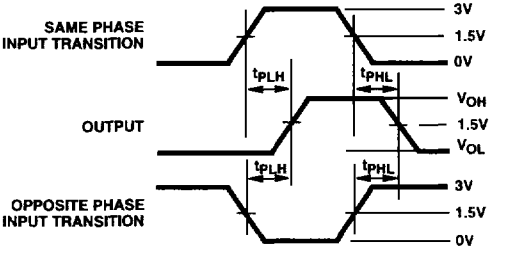


FIGURE 3. PROPAGATION DELAY