Integrated Device Technology, Inc.

OCTAL 2:1 MULTIPLEXER BUS SWITCH

IDT74FST3390
IDT74FST32390
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance:
  FST3xxx – 5Ω
  FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in 28-pin QSOP, SOIC and TSSOP

DESCRIPTION:

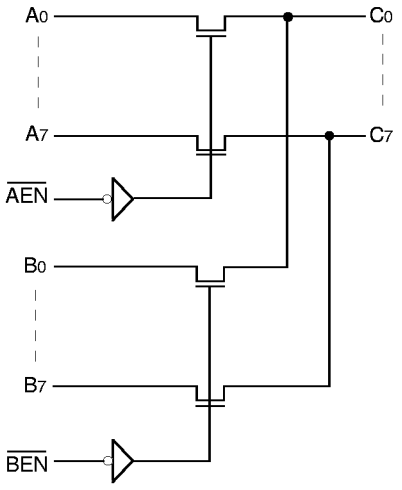
The FST3390/32390 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32390 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

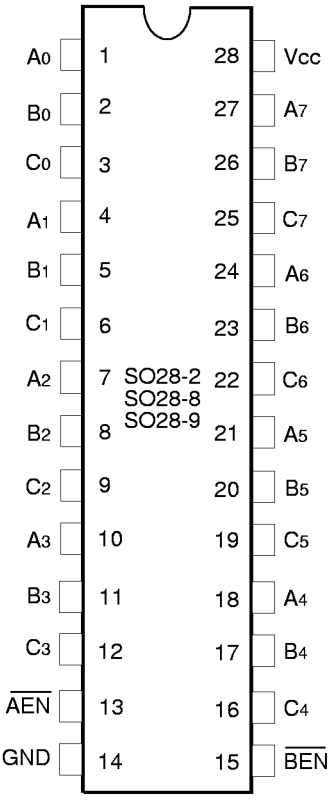
The FST3390 and FST32390 are 8-bit TTL-compatible 2:1 bus multiplexers. $\overline{AEN}$ = 0 connects port A to port C and $\overline{BEN}$ = 0 connects port B to port C. This device can be used to connect ports A & B to a common bus on port C or to broadcast data on port C to both ports A and B.

FUNCTIONAL BLOCK DIAGRAM



3260 drw 01

PIN CONFIGURATION



SOIC/
QSOP/TSSOP
TOP VIEW

3260 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
A0-7	I/O	Bus A
B0-7	I/O	Bus B
C0-7	I/O	Bus C
$\overline{AEN}$, $\overline{BEN}$	I	Bus Switch Enable (Active LOW)

3260 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Maximum Continuous Channel Current	128	mA

3260 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condiitions for extended periods may affect reliability.
2. V_{CC}, Control and Switch terminals.

FUNCTION TABLE

$\overline{AEN}$	$\overline{BEN}$	A	B	Description
H	H	Off	Off	Disconnect
L	H	On	Off	A to C
H	L	Off	On	B to C
L	L	On	On	A, B to C

3260 tbl 03

CAPACITANCE(1)

Symbol	Parameter	Conditions(2)	Typ.	Unit
C_{IN}	Control Input Capacitance		4	pF
$C_{I/O}$	Switch Input/Output Capacitance	Switch Off		pF

3260 tbl 04

NOTES:
1. Capacitance is characterized but not tested
2. T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min. V_{IN} = 0.0V	3xxx	—	5	7	Ω
		I_{ON} = 30mA	32xxx	17	28	40	
		V_{CC} = Min. V_{IN} = 2.4V	3xxx	—	10	15	Ω
		I_{ON} = 15mA	32xxx	20	35	48	
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	3	µA

3260 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	3.2	mA
		(8 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	2.7	4.0	

NOTES: 3260 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

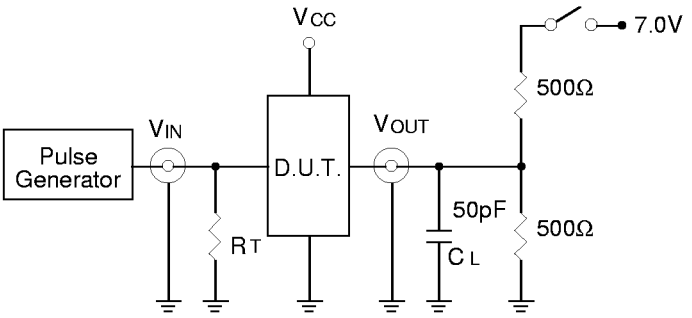
Symbol	Description	Condition[1]	Min.[2]	Typ.	3390 Max.	32390 Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay A, B to/from C[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	1.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\overline{AEN}$/$\overline{BEN}$ to A, B, C		1.5	—	6.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\overline{AEN}$, $\overline{BEN}$ to A, B, C[3]		1.5	—	5.5	5.5	ns
$\|Q_{CI}\|$	Charge Injection[5,6]		—	1.5	—	—	pC

NOTES: 3260 tbl 07

1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3260 lnk 03

SWITCH POSITION

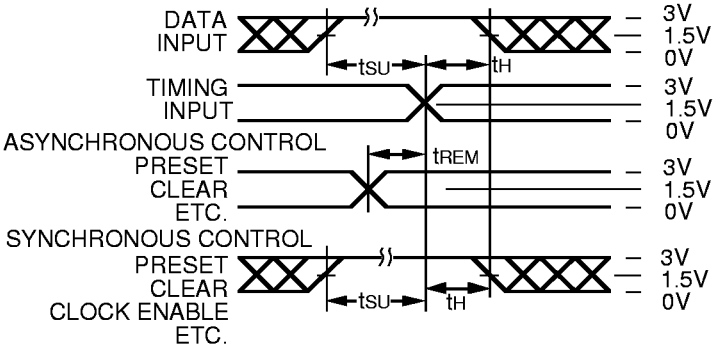
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

3260 lnk 08

DEFINITIONS:

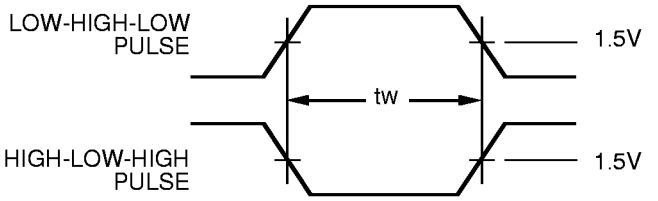
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



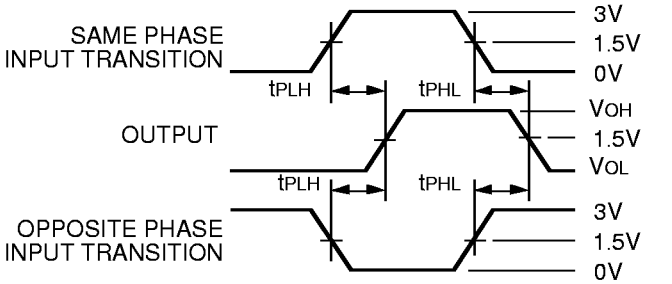
3260 lnk 04

PULSE WIDTH



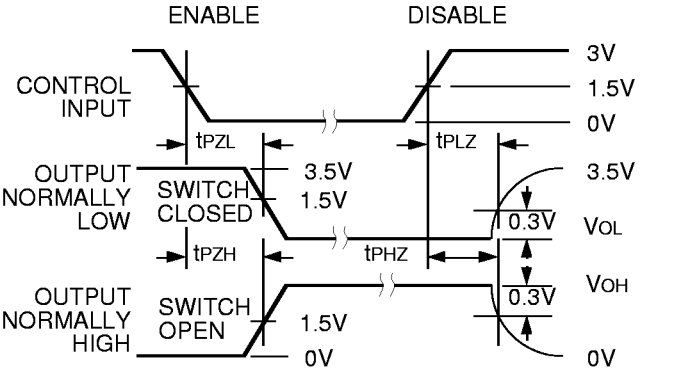
3260 lnk 05

PROPAGATION DELAY



3260 lnk 06

ENABLE AND DISABLE TIMES

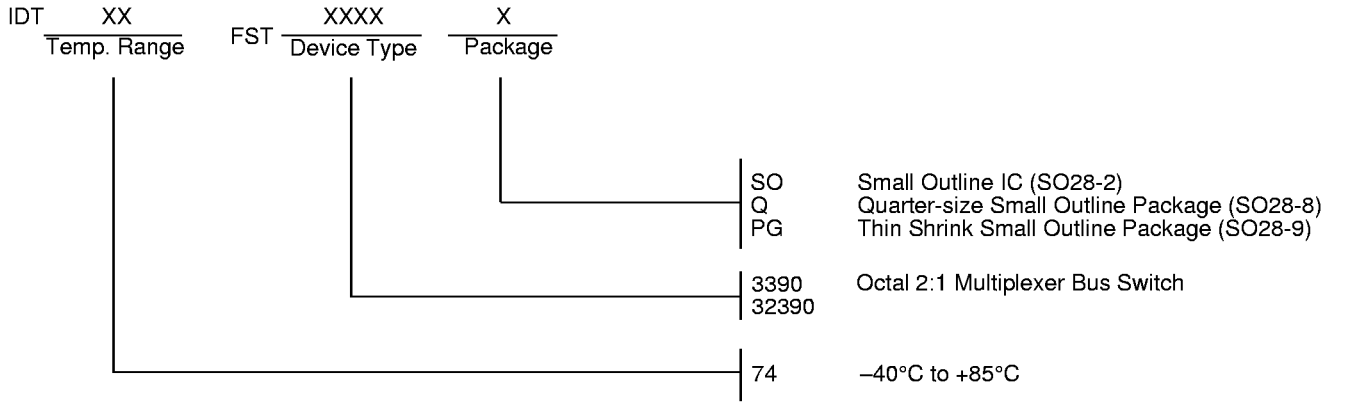


3260 lnk 07

NOTES:

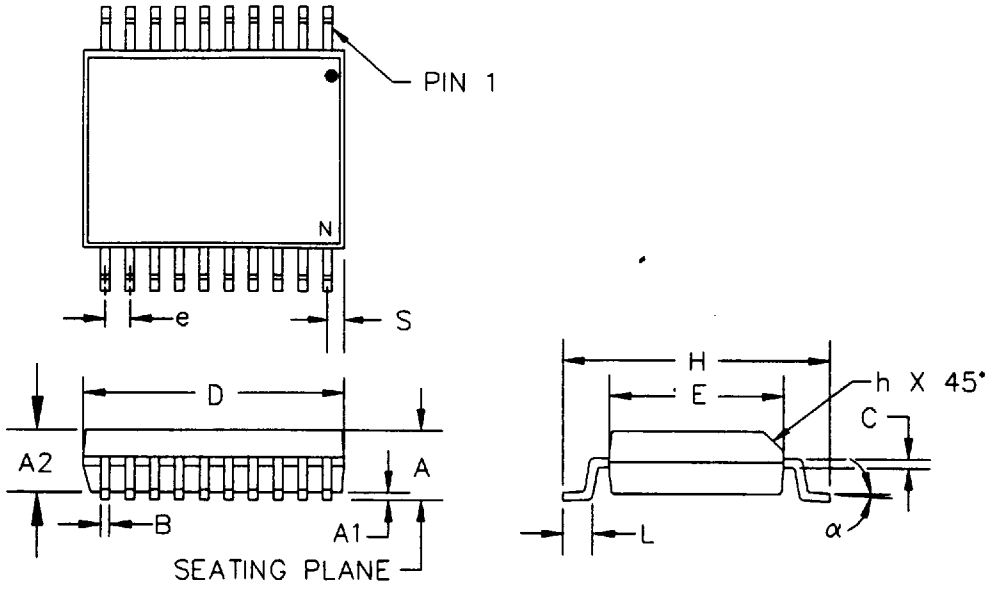
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



3260 drw 08

QUARTER SIZE OUTLINE PACKAGE



NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. D & E REF DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" PER SIDE.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003" AT SEATING PLANE.

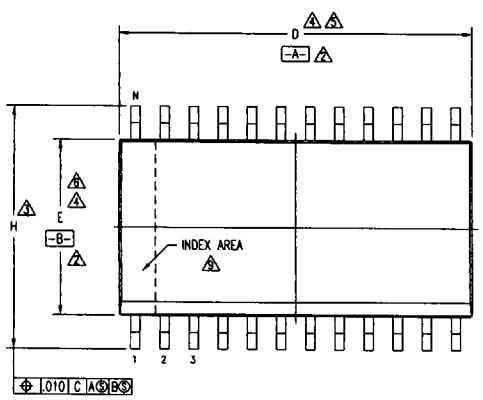
16-28 LEAD QSOP (.150" BODY WIDTH)

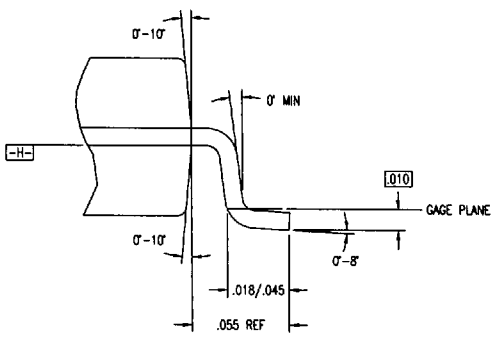
DWG #	SO16-7		SO20-8		SO24-8		SO28-8	
No. OF LD	16		20		24		28	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.068	.061	.068	.061	.068	.061	.068
A1	.004	.0098	.004	.0098	.004	.0098	.004	.0098
A2	.055	.061	.055	.061	.055	.061	.055	.061
B	.0078	.0122	.0078	.0122	.0078	.0122	.0078	.0122
C	.0075	.0098	.0075	.0098	.0075	.0098	.0075	.0098
D	.189	.196	.337	.344	.337	.344	.386	.393
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
E	.150	.157	.150	.157	.150	.157	.150	.157
H	.230	.244	.230	.244	.230	.244	.230	.244
h	.010	.016	.010	.016	.010	.016	.010	.016
L	.016	.035	.016	.035	.016	.035	.016	.035
S	.002	.007	.050	.055	.025	.030	.025	.030
α	0°	8°	0°	8°	0°	8°	0°	8°

PACKAGE DIAGRAM OUTLINES

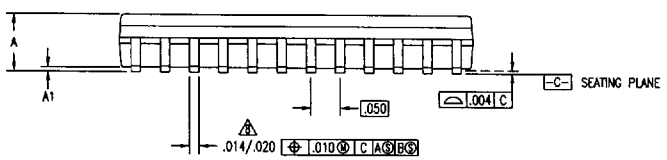
SOIC

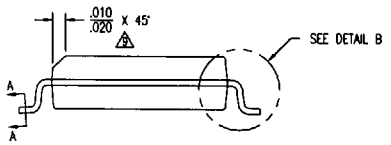
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

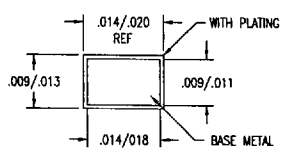




DETAIL B







SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL XX± XXX± XXXX±	ANGULAR ±	
APPROVALS	DATE	TITLE PS PACKAGE OUTLINE .300" BODY WIDTH SOIC .050" PITCH
DRAWN	03/15/89	
CHECKED		SIZE C / DRAWING No. PSC-4007 / REV 06
		DO NOT SCALE DRAWING

SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	SO16-1			
SYMBOL	JEDEC VARIATION AA			NOTE
	MIN	NOM	MAX	
A	.095	.100	.104	
A1	.005	.008	.012	
D	.403	.408	.413	4,5
E	.292	.296	.299	4,6
H	.400	.406	.419	3
N	16			

DWG #	SO18-1			
SYMBOL	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.095	.100	.104	
A1	.005	.008	.012	
D	.447	.454	.462	4,5
E	.292	.296	.299	4,6
H	.400	.406	.419	3
N	18			

DWG #	SO20-2			
SYMBOL	JEDEC VARIATION AC			NOTE
	MIN	NOM	MAX	
A	.095	.100	.104	
A1	.005	.008	.012	
D	.497	.504	.511	4,5
E	.292	.296	.299	4,6
H	.400	.406	.419	3
N	20			

DWG #	SO24-2			
SYMBOL	JEDEC VARIATION AD			NOTE
	MIN	NOM	MAX	
A	.095	.100	.104	
A1	.005	.008	.012	
D	.600	.607	.614	4,5
E	.292	.296	.299	4,6
H	.400	.406	.419	3
N	24			

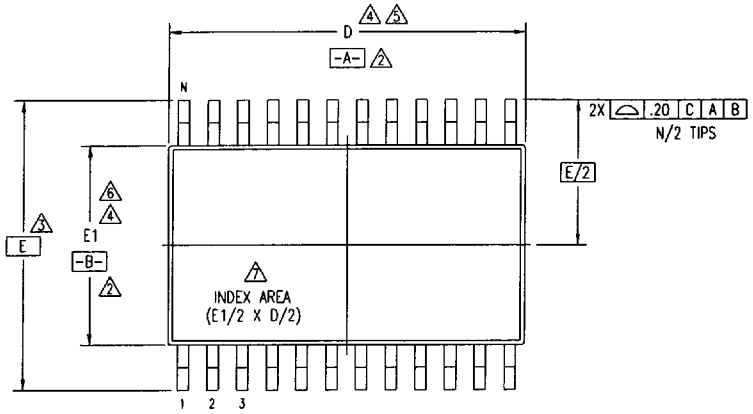
DWG #	SO28-2			
SYMBOL	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX	
A	.095	.100	.104	
A1	.005	.008	.012	
D	.700	.706	.712	4,5
E	.292	.296	.299	4,6
H	.400	.406	.419	3
N	28			

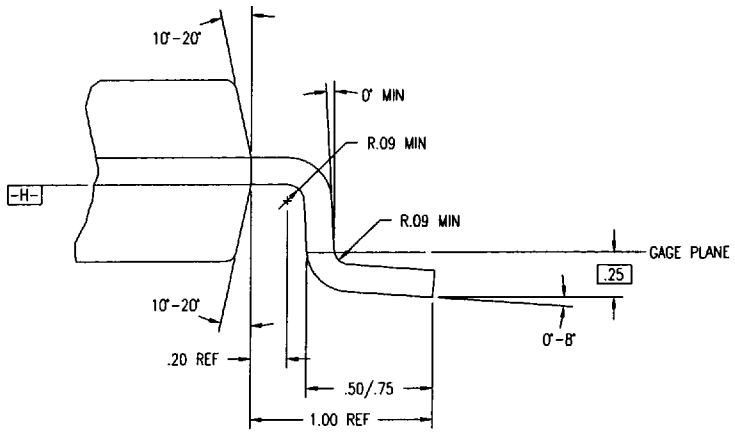
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION H TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
6. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-013, VARIATION AA, AB, AC, AD & AE

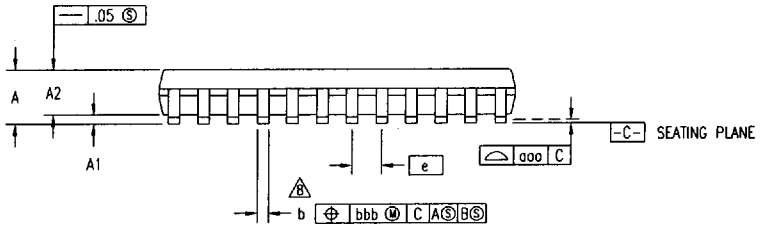
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL XX± XXX± XXXX±	ANGULAR ±	2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
APPROVALS	DATE	TITLE PS PACKAGE OUTLINE .300" BODY WIDTH SOIC .050" PITCH
DRAWN dd	03/15/89	
CHECKED		SIZE C DRAWING No. PSC-4007 REV 06
		DO NOT SCALE DRAWING

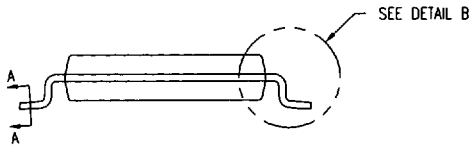
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28794	00	INITIAL RELEASE	04/01/96	T. VU
29022	01	DELETE 48 & 56 LD	06/20/96	

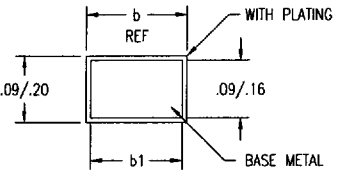




DETAIL B







SECTION A-A

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

APPROVALS	DATE
DRAWN JV	01/15/96
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE PG PACKAGE OUTLINE
4.4 mm BODY WIDTH TSSOP
.65 mm LEAD PITCH

SIZE	DRAWING No.	REV
C	PSC-4056	01

DO NOT SCALE DRAWING SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28794	00	INITIAL RELEASE	04/01/96	T. VU
29022	01	DELETE 48 & 56 LD	06/20/96	

SYMBOL	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.20		–	–	1.20		–	–	1.20	
A1	.05	–	.15		.05	–	.15		.05	–	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	6.40	6.50	6.60	4,5	7.70	7.80	7.90	4,5	9.60	9.70	9.80	4,5
E	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3
E1	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6
e	.65 BSC				.65 BSC				.65 BSC			
b	.19	–	.30		.19	–	.30		.19	–	.30	
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25	
aaa	–	–	.10		–	–	.10		–	–	.10	
bbb	–	–	.10		–	–	.10		–	–	.10	
N	20				24				28			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

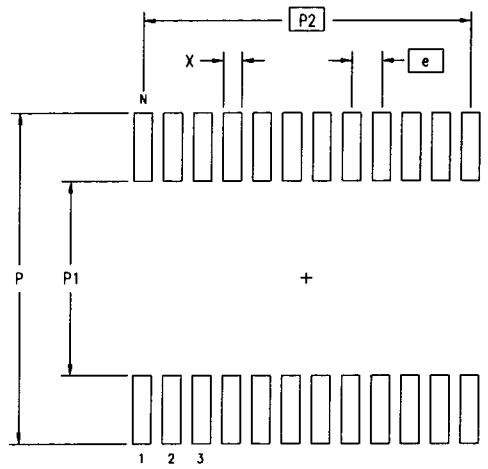
8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION AC, AD & AE

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40
P2	5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC	
N	20		24		28	

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

APPROVALS	DATE
DRAWN JTJ	01/15/96
CHECKED	

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TITLE PG PACKAGE OUTLINE
4.4 mm BODY WIDTH TSSOP
.65 mm LEAD PITCH

SIZE	DRAWING No.	REV
C	PSC–4056	01

DO NOT SCALE DRAWING SHEET 2 OF 2