



DUAL 4-BIT TO 1-BIT FET MULTIPLEXER/ DEMULTIPLEXER

IDT74FST3253

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance: 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and SOIC Packages

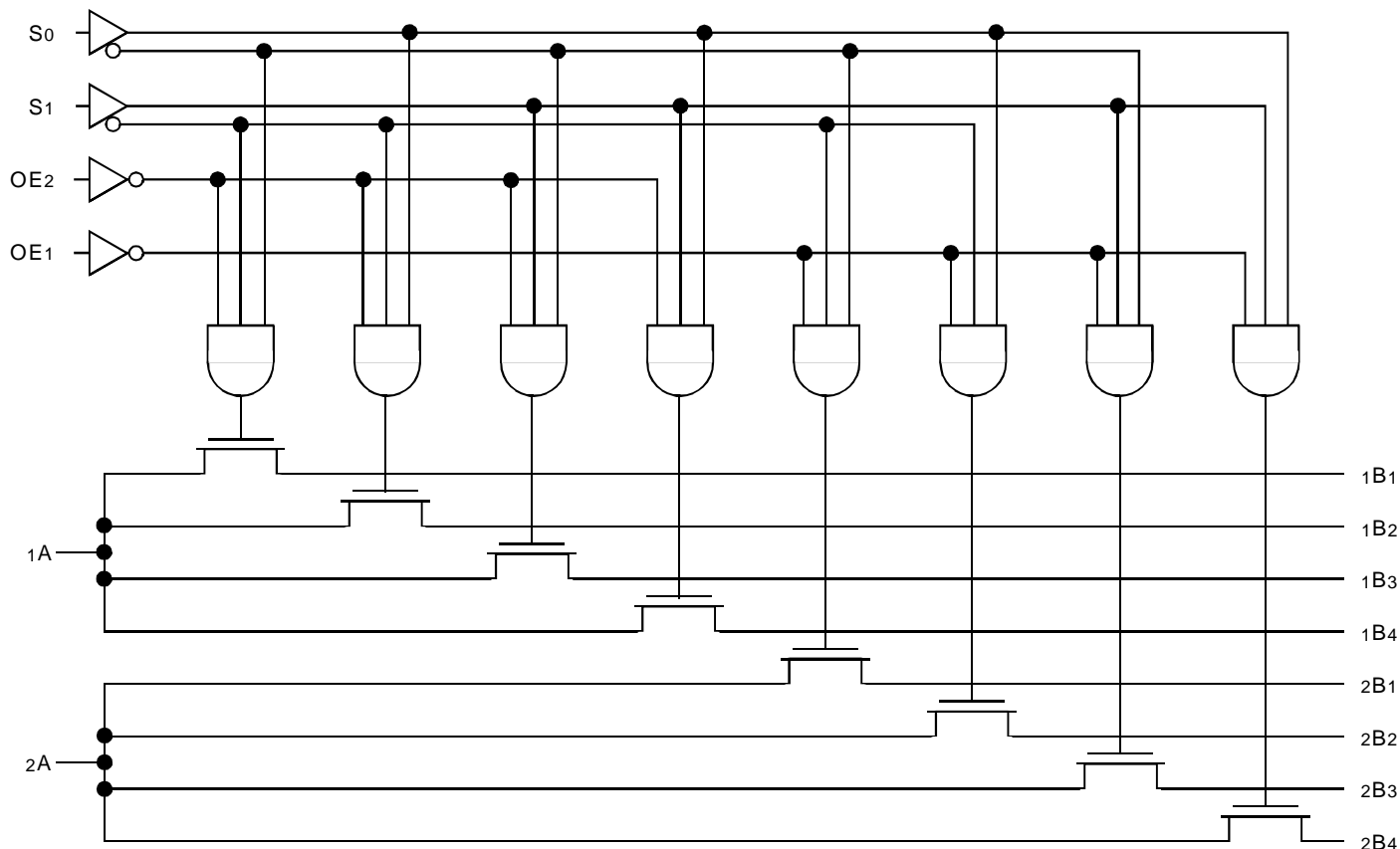
DESCRIPTION:

The FST3253 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.

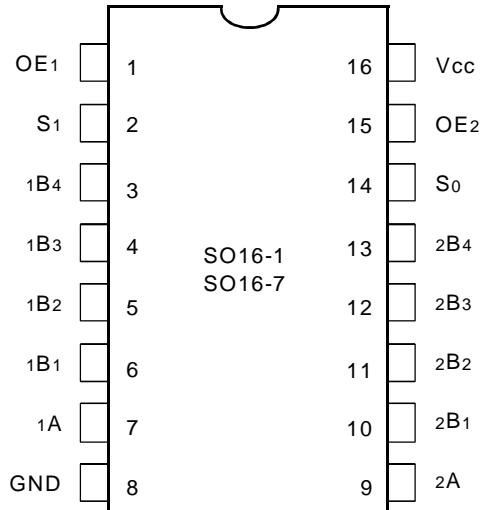
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST3253 is a dual, bidirectional 4 to 1 mux/demux. It is ideal for use in high speed interleaving or bus selection applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
 TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	Maximum Continuous Channel Current	128	mA

FST LINK

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{cc}, Control, and Switch terminals.

CAPACITANCE (1)

Symbol	Parameter	Conditions(2)	Typ.	Unit
C _{IN}	Control Input Capacitance		4	pF
C _{I/O}	Switch Input/Output Capacitance	Switch Off		pF

NOTES:

- Capacitance is characterized but not tested.
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

PIN DESCRIPTION

Pin Names	I/O	Description
xA	I/O	Muxed BUs
xBy	I/O	Demux Bus
\overline{OE}_x	I	Output Enable
S ₀ , S ₁	I	Mux Select

FUNCTIONAL TABLE (1)

S ₁	S ₀	\overline{OE}_1	\overline{OE}_2	Function
X	X	H	X	Disconnect 1A
X	X	X	H	Disconnect 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	H	L	L	1A to 1B2 and 2A to 2B2
H	L	L	L	1A to 1B3 and 2A to 2B3
H	H	L	L	1A to 1B4 and 2A to 2B4

NOTE:

- H = HIGH
 L = LOW
 X = Don't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$	—	—	± 1	μA
I_{IL}	Input LOW Current		$V_I = \text{GND}$	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$ $V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	—	300	—	mA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 64\text{mA}$	—	5	7	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$	—	5	7	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	10	15	Ω
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$	—	—	± 1	μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_I = \text{GND}$ or V_{CC}	—	0.1	3	μA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open One Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—			$\mu A/$ MHz/ Switch
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open Two Enable Pins Toggling (2 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—			mA
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—			

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_i N)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Input Frequency
 N = Number of Switches Toggling at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: $T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = 5.0V \pm 10\%$

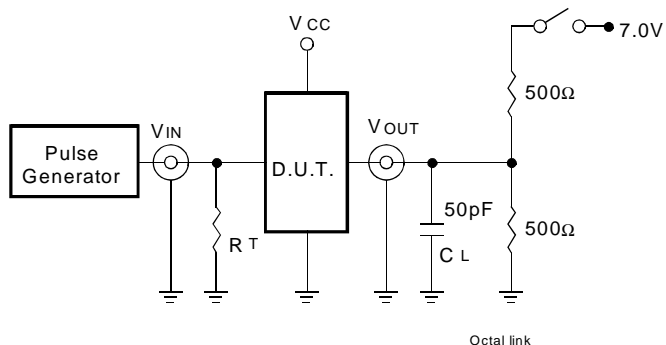
Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay x_A to x_{By} ^(3,4)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	—	0.25	ns
t_{BX}	Switch Multiplex Delay S_x to A_x , x_{By}		1.5	—	6.5	ns
t_{PZH} t_{PZL}	Switch Turn on Delay \overline{OE} to A_x , x_{By}		1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay \overline{OE} to A_x , x_{By} ⁽³⁾		1.5	—	5.5	ns
$ Q_{CI} $	Charge Injection, Typical ^(5,7)		—	1.5	—	pC
$ Q_{CDI} $	Charge Injection, Typical ^(6,7)		—	0.5	—	

NOTES:

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 m Ω scope probe, $V_{IN} = 0.0$ volts.
- Measured at switch turn off through bus multiplexer, (e.g. B_1 to $A = > B_2$ to A), load = 50 pF in parallel with 10 M Ω scope probe, V_{IN} at $A = 0.0$ volts. Charge injection is reduced because the injection from the turn off of the B_1 to A switch is compensated by the turn on of the B_2 to A switch.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

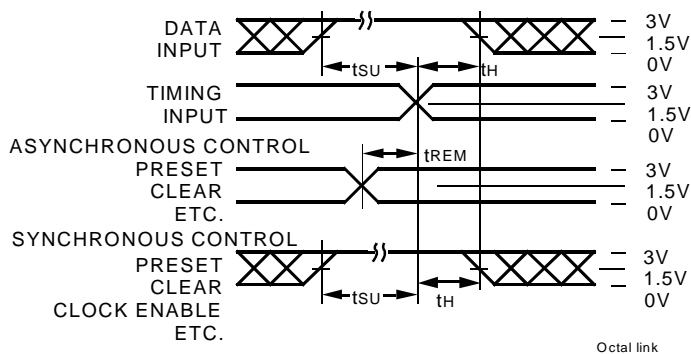
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

FCT LINK

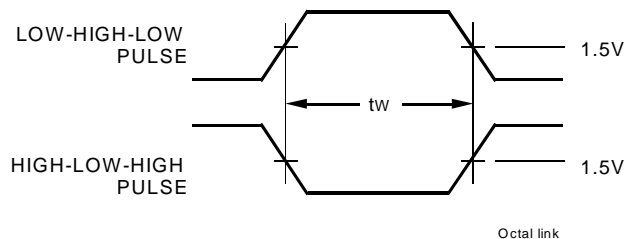
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

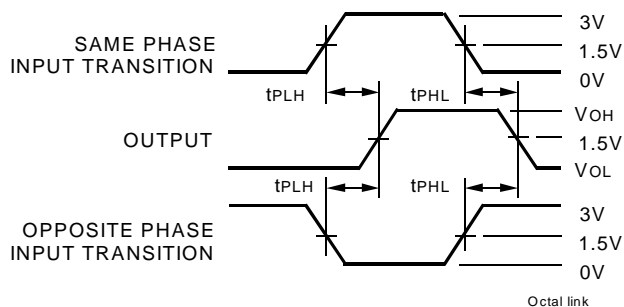
SET-UP, HOLD, AND RELEASE TIMES



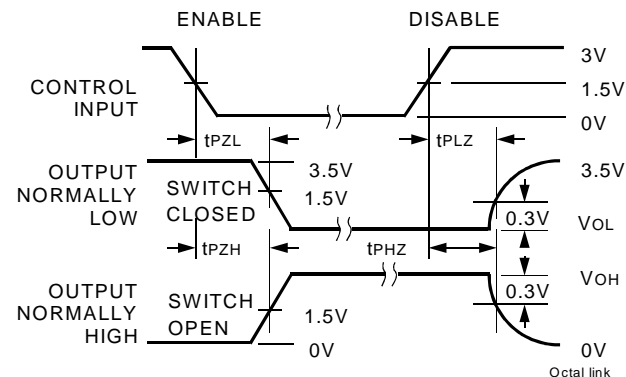
PULSE WIDTH



PROPAGATION DELAY



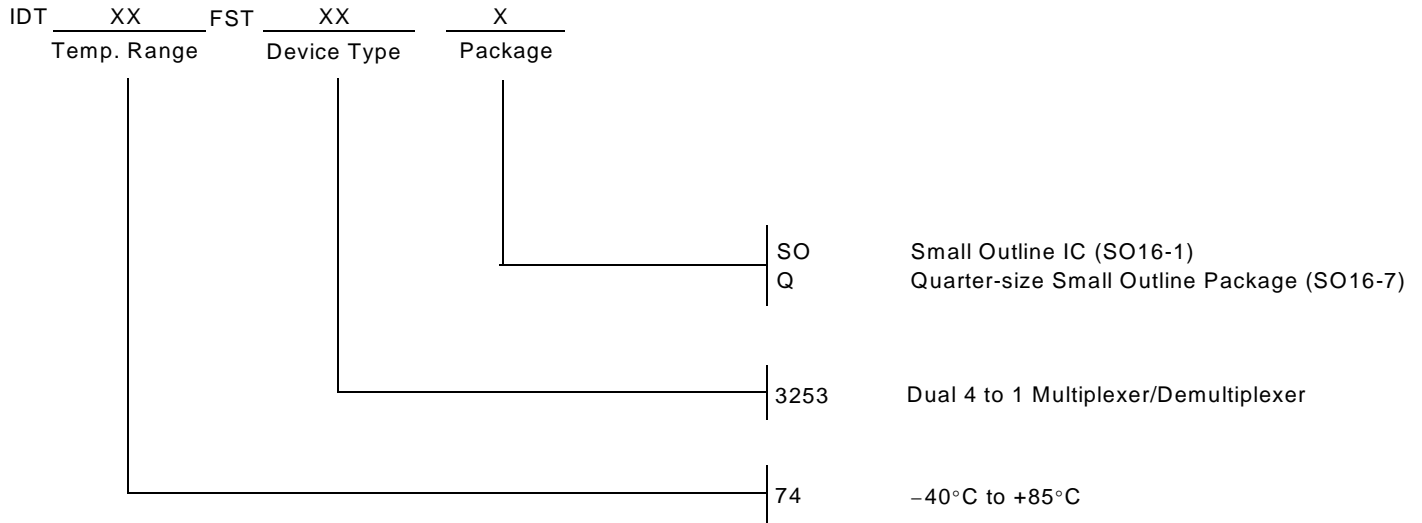
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

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