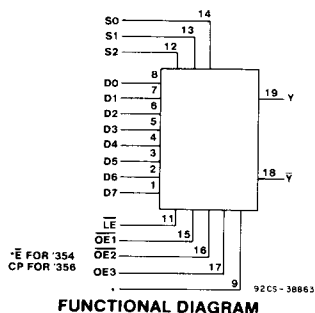


# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356

## High-Speed CMOS Logic



### 8-Input Multiplexer/Register, 3-State

CD54/74HC/HCT354 — Transparent Data & Select Latches

CD54/74HC/HCT356 — Edge-Triggered Data Flip-Flops  
Transparent Select Latches

#### Type Features:

- Buffered inputs
- 3-State Complementary Outputs
- Bus Line Driving Capability
- Typical propagation delay:  $V_{CC} = 5V, C_L = 15 pF, T_A = 25^\circ C$   
Data to Output (354) = 18 ns  
Clock to Output (356) = 22 ns

#### Family Features:

- Fanout (Over Temperature Range):  
Standard Outputs - 10 LSTTL Loads  
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:  
CD74HC/HCT:  $-40$  to  $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:  
2 to 6 V Operation  
High Noise Immunity:  
 $N_{IL} = 30\%, N_{IH} = 30\%$  of  $V_{CC}$ : @  $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:  
4.5 to 5.5 V Operation  
Direct LSTTL Input Logic Compatibility  
 $V_{IL} = 0.8 V$  Max.,  $V_{IH} = 2 V$  Min.  
CMOS Input Compatibility  
 $I_i \leq 1 \mu A$  @  $V_{OL}, V_{OH}$

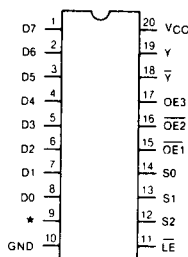
The RCA-CD54/74HC/HCT354 and CD54/74HC/HCT356 are data selectors/multiplexers that select one of eight sources. In both the HC/HCT354 and HC/HCT356 the data select bits S0, S1, and S2 are stored in transparent latches that are enabled by a low latch enable input, LE.

In the HC/HCT354 the data enable input, E, controls transparent latches that pass data to the outputs when E is high and latches in new data when E is low.

In the HC/HCT356 the data is stored in edge-triggered flip-flops that are triggered by a low-to-high clock transition.

In both types the three-state outputs are controlled by three output-enable inputs OE1, OE2, and OE3.

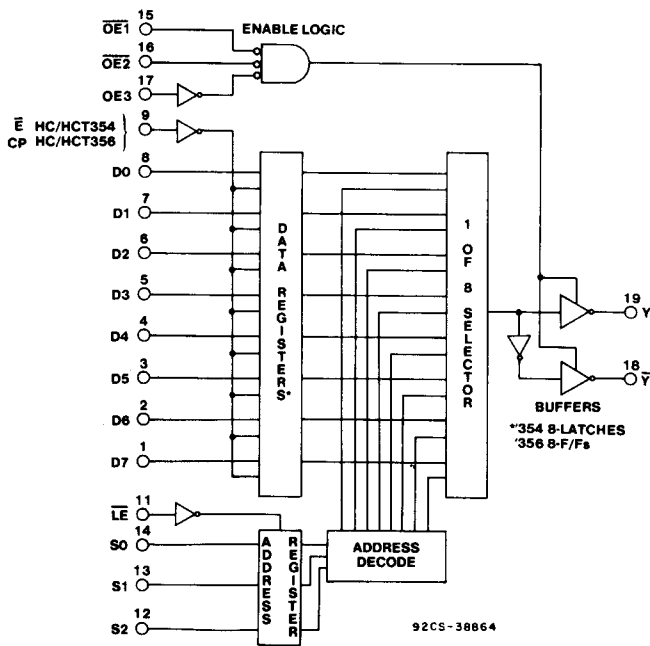
The CD54HC/HCT354/356 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT354/356 are supplied in 20-lead plastic dual-in-line plastic packages (E suffix). The CD54/74HC/HCT354/356 are also supplied in chip form (H suffix). The CD74HC/HCT354/356 are also available in plastic surface mounted packages (M suffix).



\*E for 354  
CP for 356

#### TERMINAL ASSIGNMENT

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356



Block Diagram

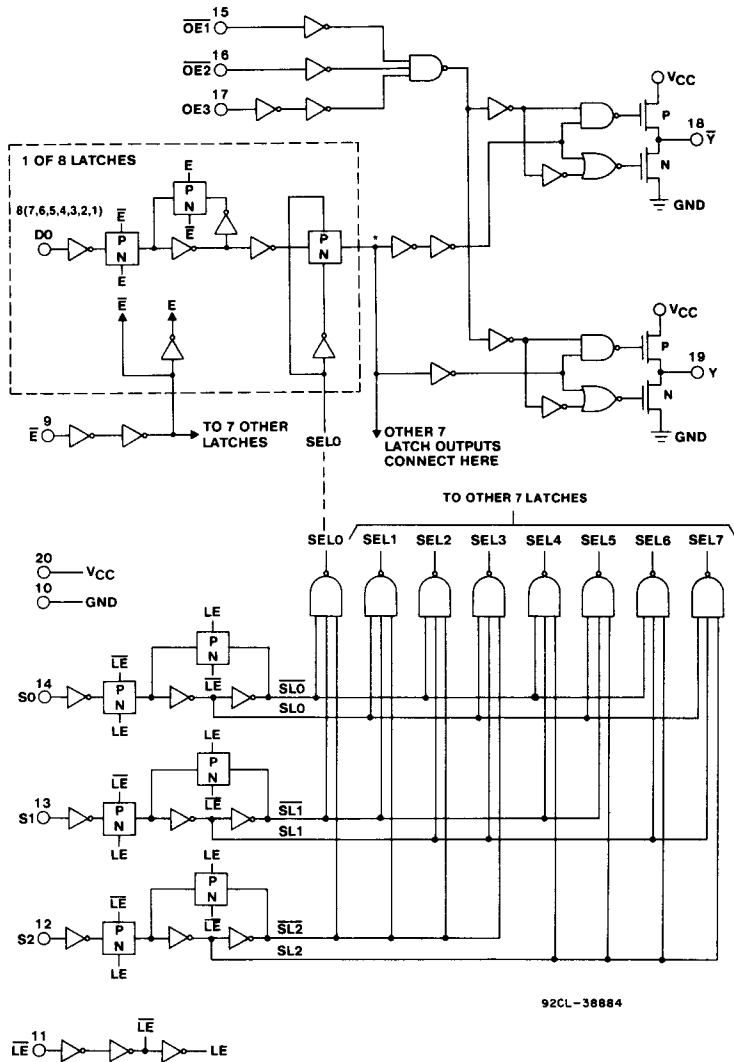
### TRUTH TABLE

Select #			Inputs				Output Enables			Outputs	
S2	S1	S0	Enable Data 'HC354 'HCT354	Clock 'HC356 'HCT356	OE1	OE2	OE3	Y	Y		
X	X	X	X	X	H	X	X	Z	Z		
X	X	X	X	X	X	H	X	Z	Z		
X	X	X	X	X	X	X	L	Z	Z		
L	L	L	L	↔	L	L	H	$\overline{D_0}$	D0		
L	L	L	H	H or L	L	L	H	$\overline{D_0}$	D0 <sub>n</sub>		
L	L	H	L	↔	L	L	H	$\overline{D_1}$	D1		
L	L	H	H	H or L	L	L	H	$\overline{D_1}$	D1 <sub>n</sub>		
L	H	L	L	↔	L	L	H	$\overline{D_2}$	D2		
L	H	L	H	H or L	L	L	H	$\overline{D_2}$	D2 <sub>n</sub>		
L	H	H	L	↔	L	L	H	$\overline{D_3}$	D3		
L	H	H	H	H or L	L	L	H	$\overline{D_3}$	D3 <sub>n</sub>		
H	L	L	L	↔	L	L	H	$\overline{D_4}$	D4		
H	L	L	H	H or L	L	L	H	$\overline{D_4}$	D4 <sub>n</sub>		
H	L	H	L	↔	L	L	H	$\overline{D_5}$	D5		
H	L	H	H	H or L	L	L	H	$\overline{D_5}$	D5 <sub>n</sub>		
H	H	L	L	↔	L	L	H	$\overline{D_6}$	D6		
H	H	L	H	H or L	L	L	H	$\overline{D_6}$	D6 <sub>n</sub>		
H	H	H	L	↔	L	L	H	$\overline{D_7}$	D7		
H	H	H	H	H or L	L	L	H	$\overline{D_7}$	D7 <sub>n</sub>		

**Notes**

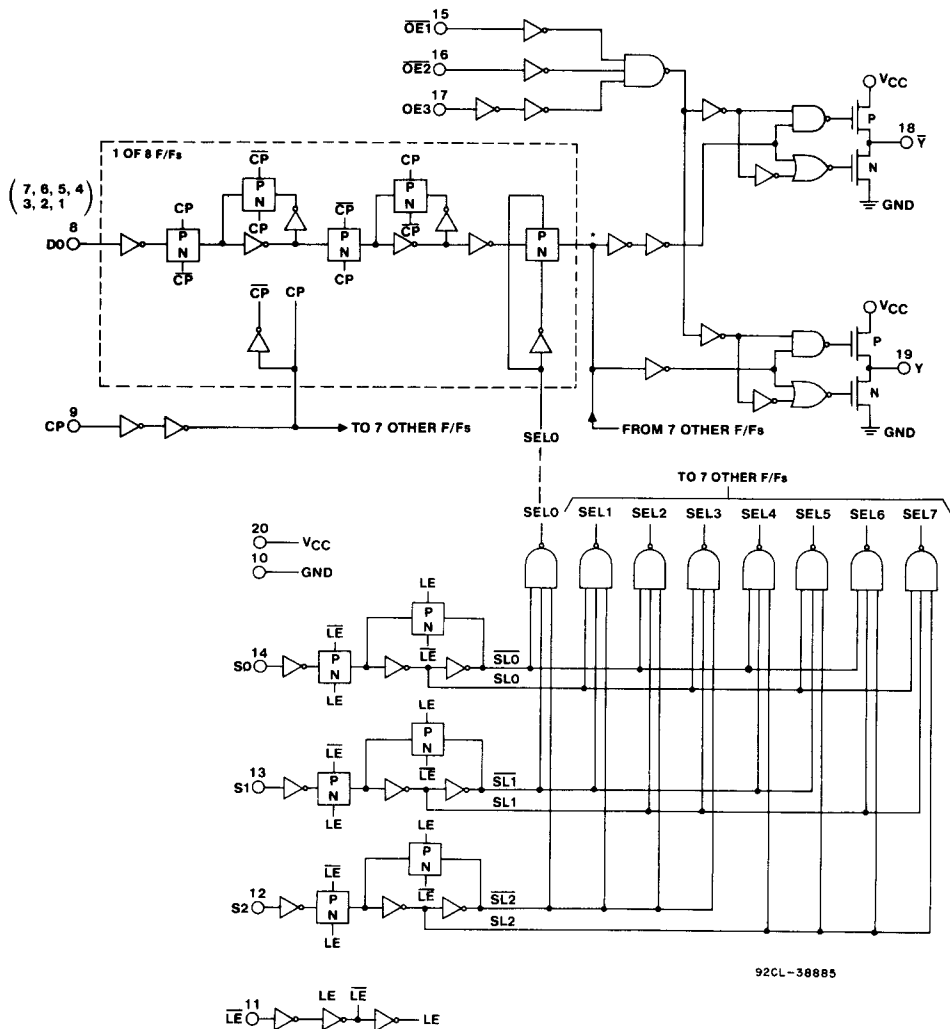
- H = high level (steady state)
- L = low level (steady state)
- X = irrelevant (any input, including transitions)
- Z = high-impedance state (off state)
- ↔ = transition from low to high level
- D0 ... D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of HC356
- D0<sub>n</sub> ... D7<sub>n</sub> = the level of steady state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock
- # This column shows the input address setup with  $\overline{LE}$  low

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356



HC/HCT354 Logic Diagram

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356



HC/HCT356 Logic Diagram

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE, ( $V_{cc}$ ) (Voltages referenced to ground)	-0.5 to +7V
DC INPUT DIODE CURRENT, $I_{ik}$ (FOR $V_i < -0.5$ V OR $V_i > V_{cc} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{ok}$ (FOR $V_o < -0.5$ V OR $V_o > 0.5$ V + $V_{cc}$ )	$\pm 20$ mA
DC DRAIN CURRENT, PER OUTPUT ( $I_o$ ) (FOR $-0.5$ V $< V_o < V_{cc} + 0.5$ V)	$\pm 35$ mA
DC $V_{cc}$ OR GROUND CURRENT ( $I_{cc}$ )	$\pm 70$ mA
POWER DISSIPATION PER PACKAGE ( $P_o$ ):	
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F, H	-55 to $+125^\circ$ C
PACKAGE TYPE E, M	-40 to $+85^\circ$ C
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ$ C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max.	$+265^\circ$ C
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ$ C

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range) CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage $V_i, V_o$	0	$V_{cc}$	V
Operating Temperature $T_A$ : CD74 Types CD54 Types	-40 -55	+85 +125	$^\circ$ C
Input Rise and Fall Times $t_r, t_f$ at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

\*Unless otherwise specified, all voltages are referenced to Ground.

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC354/356/CD54HC354/356										CD74HCT354/356/CD54HCT354/356								UNITS				
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE					
	V <sub>I</sub> V	I <sub>O</sub> mA	V <sub>CC</sub> V	+25° C			-40/ +85° C		-55/ +125° C		V <sub>I</sub> V	V <sub>CC</sub> V	+25° C			-40/ +85° C		-55/ +125° C					
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max			
High-Level Input Voltage V <sub>IH</sub>			2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V		
			4.5	3.15	—	—	3.15	—	3.15	—		5.5											
			6	4.2	—	—	4.2	—	4.2	—													
Low-Level Input Voltage V <sub>IL</sub>			2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	—	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5											
			6	—	—	1.8	—	1.8	—	1.8	—												
High-Level Output Voltage V <sub>OH</sub>	V <sub>IL</sub>	-0.02	2	1.9	—	—	1.9	—	1.9	—	V <sub>IL</sub>	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V	
or			4.5	4.4	—	—	4.4	—	4.4	—	or	5.5											
CMOS Loads	V <sub>IH</sub>		6	5.9	—	—	5.9	—	5.9	—	V <sub>IH</sub>												
TTL Loads (Bus Driver)	V <sub>IL</sub>										V <sub>IL</sub>	4.5	3.98	—	—	3.84	—	3.7	—			V	
or		-6	4.5	3.98	—	—	3.84	—	3.7	—	or	5.5											
V <sub>IH</sub>		-7.8	6	5.48	—	—	5.34	—	5.2	—	V <sub>IH</sub>												
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IL</sub>	0.02	2	—	—	0.1	—	0.1	—	0.1	V <sub>IL</sub>	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	—	V
or			4.5	—	—	0.1	—	0.1	—	0.1	—	5.5											
CMOS Loads	V <sub>IH</sub>		6	—	—	0.1	—	0.1	—	0.1	—	V <sub>IH</sub>											
TTL Loads (Bus Driver)	V <sub>IL</sub>										V <sub>IL</sub>	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	—	V
or		6	4.5	—	—	0.26	—	0.33	—	0.4	or	5.5	—	—	0.26	—	0.33	—	0.4	—	0.4	—	
V <sub>IH</sub>		7.8	6	—	—	0.26	—	0.33	—	0.4	V <sub>IH</sub>												
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub>		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V <sub>CC</sub> & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	—	μA
or																							
Gnd																							
Quiescent Device Current I <sub>CC</sub>	V <sub>CC</sub>		0	6	—	—	8	—	80	—	160	V <sub>CC</sub>	5.5	—	—	8	—	80	—	160	—	μA	
or																							
Gnd																							
Additional Quiescent Device Current per input pin: 1 unit load Δ I <sub>CC</sub> *												V <sub>CC</sub> -2.1	4.5	to	—	100	360	—	450	—	490	—	μA
													5.5										
3-State Leakage Current I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V <sub>IL</sub> or V <sub>IH</sub>	5.5	—	—	±0.5	—	±5.0	—	±10	—	±10	—	μA

\*For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356

HCT354 Input Loading Table

Input	Unit Loads*
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE}1, \overline{OE}2$	0.80
OE3	0.25
$\overline{LE}$	0.25
$\overline{E}$	0.60

\*Unit Load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 360  $\mu A$  max. @ 25°C.

HCT356 Input Loading Table

Input	Unit Loads*
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE}1, \overline{OE}2$	0.80
OE3	0.25
$\overline{LE}$	0.25
CP	0.60

\*Unit Load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 360  $\mu A$  max. @ 25°C.

## SWITCHING CHARACTERISTICS ( $V_{CC} = 5 V, T_A = 25^\circ C$ , Input $t_r, t_f = 6 ns$ ) — HC/HCT354

CHARACTERISTIC	$C_L$ (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay $D_n \rightarrow Y, \overline{Y}$	15	$t_{PLH}, t_{PHL}$	18	20	ns
$\overline{E} \rightarrow Y, \overline{Y}$	15	$t_{PLH}, t_{PHL}$	21	23	ns
$S_n \rightarrow Y, \overline{Y}$	15	$t_{PLH}, t_{PHL}$	22	25	ns
$\overline{LE} \rightarrow Y, \overline{Y}$	15	$t_{PLH}, t_{PHL}$	24	25	ns
Output Disabling Time	15	$t_{PLZ}, t_{PHZ}$	13	13, 16	ns
Output Enabling Time	15	$t_{PZL}, t_{PZH}$	12, 13	14	ns
Power Dissipation Capacitance*	—	$C_{PD}$	90	92	pF

\* $C_{PD}$  is used to determine the dynamic power consumption, per device.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where:

$f_i$  = input frequency,

$C_L$  = output load capacitance.

$V_{CC}$  = supply voltage

## PREREQUISITE FOR SWITCHING FUNCTION — HC/HCT354

CHARACTERISTIC	SYMBOL	$V_{CC}$	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{E}$ pulse width	$t_{PLH}$ $t_{PHL}$	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{LE}$ pulse width	$t_{PLH}$ $t_{PHL}$	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set Up Times $D_n \rightarrow \overline{E}$	$t_{SU}$	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
$S_n \rightarrow \overline{LE}$	$t_{SU}$	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Times $D_n \rightarrow \overline{E}$	$t_H$	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	
$S_n \rightarrow \overline{LE}$	$t_H$	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356

## SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns) — HC/HCT354

CHARACTERISTIC	SYMBOL	V <sub>CC</sub>	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, D <sub>n</sub> → Y, $\bar{Y}$	t <sub>PLH</sub>	2	—	210	—	—	—	265	—	—	—	315	—	—	ns
	t <sub>PHL</sub>	4.5	—	42	—	47	—	53	—	59	—	63	—	71	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
$\bar{E}$ → Y, $\bar{Y}$	t <sub>PLH</sub>	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t <sub>PHL</sub>	4.5	—	50	—	54	—	63	—	68	—	75	—	81	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
S <sub>n</sub> → Y, $\bar{Y}$	t <sub>PLH</sub>	2	—	260	—	—	—	325	—	—	—	390	—	—	ns
	t <sub>PHL</sub>	4.5	—	52	—	59	—	65	—	74	—	78	—	89	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
$\bar{LE}$ → Y, $\bar{Y}$	t <sub>PLH</sub>	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
	t <sub>PHL</sub>	4.5	—	58	—	63	—	73	—	79	—	87	—	94	
		6	—	49	—	—	—	62	—	—	—	74	—	—	
Output Disabling Time $\bar{O}E_n$ to Y, $\bar{Y}$	t <sub>PLZ</sub>	2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	33	—	39	—	41	—	47	—	50	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
OE3 to Y, $\bar{Y}$	t <sub>PHZ</sub>	2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	39	—	39	—	49	—	47	—	59	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Enabling Time $\bar{O}E_n$ to Y, $\bar{Y}$	t <sub>PZL</sub>	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	34	—	38	—	43	—	45	—	51	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
OE3 to Y, $\bar{Y}$	t <sub>PZH</sub>	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
		4.5	—	32	—	34	—	40	—	43	—	48	—	51	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C <sub>i</sub>		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-state Output Capacitance	C <sub>o</sub>		—	20	—	20	—	20	—	20	—	20	—	20	pF

## SWITCHING CHARACTERISTICS (V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns) — HC/HCT356

CHARACTERISTIC	C <sub>L</sub> (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay CP → Y, $\bar{Y}$	15	t <sub>PLH</sub> , t <sub>PHL</sub>	22	22	ns
		t <sub>PLH</sub> , t <sub>PHL</sub>	22	25	ns
		t <sub>PLH</sub> , t <sub>PHL</sub>	24	25	ns
Output Disabling Time	15	t <sub>PLZ</sub> , t <sub>PHZ</sub>	13	13, 15	ns
Output Enabling Time	15	t <sub>PZL</sub> , t <sub>PZH</sub>	12, 13	14	ns
Power Dissipation Capacitance*	—	C <sub>PD</sub>	51	52	pF

\*C<sub>PD</sub> is used to determine the dynamic power consumption, per device.

P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub>(C<sub>PD</sub> + C<sub>L</sub>) where:

f<sub>i</sub> = input frequency.

C<sub>L</sub> = output load capacitance.

V<sub>CC</sub> = supply voltage.



# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356

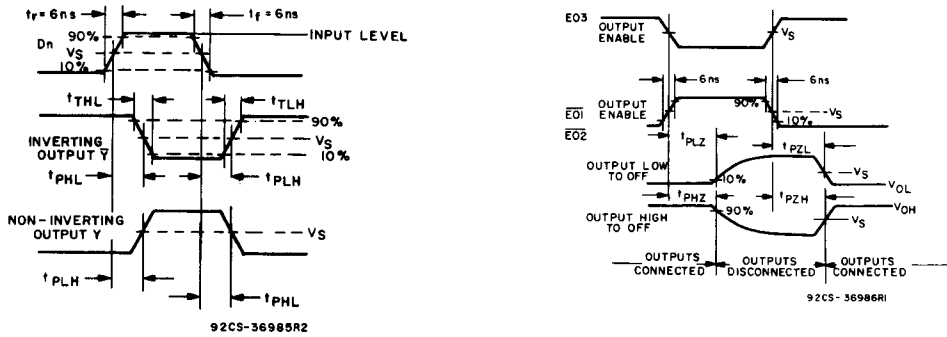
PREREQUISITE FOR SWITCHING FUNCTION — HC/HCT356

CHARACTERISTIC	SYMBOL	V <sub>CC</sub>	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t <sub>PLH</sub> t <sub>PHL</sub>	2	80	—	—	—	100	—	—	—	120	—	—	ns	
		4.5	16	—	20	—	20	—	25	—	24	—	30		—
		6	14	—	—	—	17	—	—	—	20	—	—		
LE Pulse Width	t <sub>PLH</sub> t <sub>PHL</sub>	2	80	—	—	—	100	—	—	—	120	—	—	ns	
		4.5	16	—	20	—	20	—	25	—	24	—	30		—
		6	14	—	—	—	17	—	—	—	20	—	—		
Set Up Times Dn → CP	t <sub>SU</sub>	2	5	—	—	—	5	—	—	—	5	—	—	ns	
		4.5	5	—	7	—	5	—	9	—	5	—	11		—
		6	5	—	—	—	5	—	—	—	5	—	—		
Sn → LE	t <sub>SU</sub>	2	5	—	—	—	5	—	—	—	5	—	—	ns	
		4.5	5	—	7	—	5	—	9	—	5	—	11		—
		6	5	—	—	—	5	—	—	—	5	—	—		
Hold Times Dn → CP	t <sub>H</sub>	2	45	—	—	—	55	—	—	—	70	—	—	ns	
		4.5	9	—	9	—	11	—	11	—	14	—	14		—
		6	8	—	—	—	9	—	—	—	12	—	—		
Sn → LE	t <sub>H</sub>	2	60	—	—	—	75	—	—	—	90	—	—	ns	
		4.5	12	—	12	—	15	—	15	—	18	—	18		—
		6	10	—	—	—	13	—	—	—	15	—	—		

SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns) — HC/HCT356

CHARACTERISTIC	SYMBOL	V <sub>CC</sub>	25°C				-40°C to +85°C				-55°C to +125°C				UNITS	
			HC		HCT		74HC		74HCT		54HC		54HCT			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay: CP → Y, Ȳ	t <sub>PLH</sub> t <sub>PHL</sub>	2	—	255	—	—	—	320	—	—	—	385	—	—	ns	
		4.5	—	51	—	51	—	64	—	64	—	77	—	77		—
		6	—	43	—	—	—	54	—	—	—	65	—	—		
Sn → Y, Ȳ	t <sub>PLH</sub> t <sub>PHL</sub>	2	—	260	—	—	—	325	—	—	—	390	—	—	ns	
		4.5	—	52	—	59	—	65	—	74	—	78	—	89		—
		6	—	44	—	—	—	55	—	—	—	66	—	—		
LE → Y, Ȳ	t <sub>PLH</sub> t <sub>PHL</sub>	2	—	290	—	—	—	365	—	—	—	435	—	—	ns	
		4.5	—	58	—	63	—	73	—	79	—	87	—	94		—
		6	—	49	—	—	—	62	—	—	—	74	—	—		
Output Disabling Time OE1, OE2 to Y, Ȳ OE3 to Y, Ȳ	t <sub>PLZ</sub> t <sub>PHZ</sub>	2	—	155	—	—	—	195	—	—	—	235	—	—	ns	
		4.5	—	31	—	33	—	39	—	41	—	47	—	50		—
		6	—	26	—	—	—	33	—	—	—	40	—	—		
Output Enabling Time OE1, OE2 to Y, Ȳ OE3 to Y, Ȳ	t <sub>PZL</sub> t <sub>PZH</sub>	2	—	150	—	—	—	190	—	—	—	225	—	—	ns	
		4.5	—	30	—	34	—	38	—	43	—	45	—	51		—
		6	—	26	—	—	—	33	—	—	—	38	—	—		
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>	2	—	60	—	—	—	75	—	—	—	90	—	—	ns	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18		—
		6	—	10	—	—	—	13	—	—	—	15	—	—		
Input Capacitance	C <sub>I</sub>		—	10	—	10	—	10	—	10	—	10	—	10	pF	
3-state Output Capacitance	C <sub>O</sub>		—	20	—	20	—	20	—	20	—	20	—	20	pF	

# CD54/74HC354, CD54/74HCT354 CD54/74HC356, CD54/74HCT356



	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
$V_S$	50% $V_{CC}$	1.3 V

Fig. 1 — Transition times and propagation delay times.

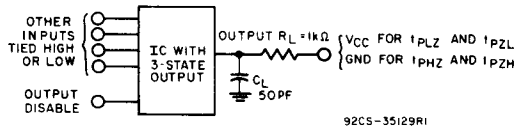


Fig. 2 — Three-state propagation delay test circuit.