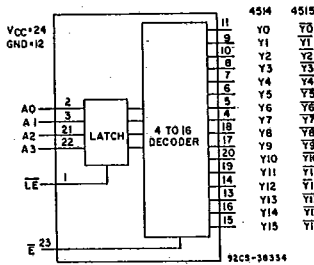


**CD54/74HC4514, CD54/74HCT4514  
CD54/74HC4515, CD54/74HCT4515**

File Number 1597

HARRIS SEMICONDUCTOR 27E D 4302271 0017981 9 HAS

**High-Speed CMOS Logic**



**4-to-16 Line Decoder/Demultiplexer  
with Input Latches**

- Type Features:**
- Multifunction capability:  
Binary to 1-of-16 decoder  
1-to-16 line demultiplexer

FUNCTIONAL DIAGRAM

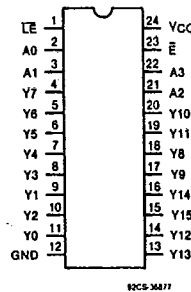
The RCA CD54/74HC4514, 4515 and CD54/74HCT4514, 4515 are high-speed silicon gate devices consisting of a 4-bit strobed latch and a 4-to-16 line decoder. The selected output is enabled by a low on the enable input ( $\bar{E}$ ). A high on  $\bar{E}$  inhibits selection of any output. Demultiplexing is accomplished by using the  $\bar{E}$  input as the data input and the select inputs (A0-A3) as addresses. This  $\bar{E}$  input also serves as a chip select when these devices are cascaded.

When Latch Enable ( $\bar{LE}$ ) is high the output follows changes in the inputs (see truth table). When  $\bar{LE}$  is low the output is isolated from changes in the input and remains at the level (high for the 4514, low for the 4515) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.

The CD54HC4514, 4515 and CD54HCT4514, 4515 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4514, 4515 and CD74HCT4514, are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

**Family Features**

- Fanout (over temperature range):  
Standard outputs — 10 LSTTL loads  
Bus driver outputs — 15 LSTTL loads
- Wide operating temperature range:  
CD74HC/HCT: -40 to +85°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Phillips/Signetics
- CD54HC/CD74HC types:  
2 to 6 V operation  
High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$ ;  
@  $V_{CC} = 5V$
- CD54HCT/CD74HCT types:  
4.5 to 5.5 V operation  
Direct LSTTL input logic compatibility  
 $V_{IL} = 0.8 V$  max.,  $V_{IH} = 2 V$  min.  
CMOS input compatibility  
 $I_i \leq 1 \mu A$  @  $V_{OL}$ ,  $V_{OH}$



TERMINAL ASSIGNMENT

# CD54/74HC4514, CD54/74HCT4514 CD54/74HC4515, CD54/74HCT4515

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{cc}$ ):	
(Voltages referenced to ground)	..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{ik}$ (FOR $V_i < -0.5$ V OR $V_i > V_{cc} + 0.5$ V)	..... $\pm 20$ mA
DC OUTPUT CURRENT, $I_{ok}$ (FOR $V_o < -0.5$ V OR $V_o > V_{cc} + 0.5$ V)	..... $\pm 20$ mA
DC DRAIN CURRENT, PER OUTPUT ( $I_o$ ) (FOR $-0.5$ V $< V_o < V_{cc} + 0.5$ V)	..... $\pm 25$ mA
DC $V_{cc}$ OR GROUND CURRENT, PER PIN ( $I_{cc}$ )	..... $\pm 50$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	..... 500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	..... Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	..... 500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	..... Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	..... 400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	..... Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F, H	..... -55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	..... -40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	..... -65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max.	..... $+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	..... $+300^\circ\text{C}$

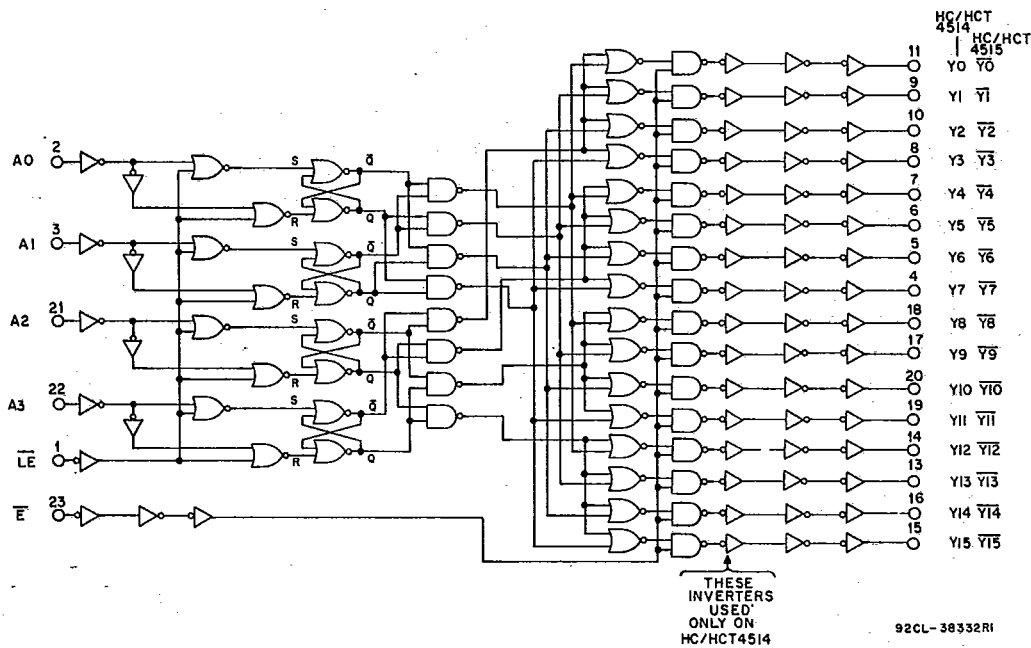


Fig. — Logic diagram for CD54/74HC4514, 4515 and CD54/74HCT4514, 4515.

HARRIS SEMICONDUCTOR 27E D 430227J 0017982 0 HAS

**CD54/74HC4514, CD54/74HCT4514**  
**CD54/74HC4515, CD54/74HCT4515**

HARRIS SEMICOND SECTOR 27E D 4302271 0017983 2 HAS

DECODE TRUTH TABLE (LE = 1)

ENABLE	DECODER INPUTS				ADDRESSED OUTPUT 4514 = Logic 1 (High) 4515 = Logic 0 (Low)
	A3	A2	A1	A0	
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All Outputs = 0, 4514 All Outputs = 1, 4515

X = Don't Care      Logic 1 = High      Logic 0 = Low

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$ .* CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature $T_A$ : CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, $t_r, t_f$ at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

\*Unless otherwise specified, all voltages are referenced to Ground.

**CD54/74HC4514, CD54/74HCT4514  
CD54/74HC4515, CD54/74HCT4515**

**STATIC ELECTRICAL CHARACTERISTICS**

CHARACTERISTIC	CD74HC4514/CD54HC4515										CD74HCT4514/CD54HCT4515										UNITS				
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE			54HC TYPE			TEST CONDITIONS			74HCT/54HCT TYPE			74HCT TYPE			54HCT TYPE			
	V <sub>I</sub> V	I <sub>O</sub> mA	V <sub>CC</sub> V	+25°C			-40/ +85°C			-55/ +125°C			V <sub>I</sub> V	V <sub>CC</sub> V	+25°C			-40/ +85°C				-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max			
High-Level Input Voltage V <sub>IH</sub>			2	1.5	—	—	1.5	—	1.5	—	—	4.5			2	—	—	2	—	2	—		V		
			4.5	3.15	—	—	3.15	—	3.15	—	—	to													
			6	4.2	—	—	4.2	—	4.2	—	—	5.5													
Low-Level Input Voltage V <sub>IL</sub>			2	—	—	0.5	—	0.5	—	0.5	—	4.5			—	—	0.8	—	0.8	—	0.8	—	V		
			4.5	—	—	1.35	—	1.35	—	1.35	—	to													
			6	—	—	1.8	—	1.8	—	1.8	—	5.5													
High-Level Output Voltage V <sub>OH</sub> CMOS Loads	V <sub>IL</sub> or V <sub>IH</sub>	-0.02	2	1.9	—	—	1.9	—	1.9	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—		V		
			4.5	4.4	—	—	4.4	—	4.4	—															
			6	5.9	—	—	5.9	—	5.9	—															
TTL Loads	V <sub>IL</sub> or V <sub>IH</sub>	-4 -5.2	4.5	3.98	—	—	3.84	—	3.7	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	3.98	—	—	3.84	—	3.7	—				V		
			6	5.48	—	—	5.34	—	5.2	—															
Low-Level Output Voltage V <sub>OL</sub> CMOS Loads	V <sub>IL</sub> or V <sub>IH</sub>	0.02	2	—	—	0.1	—	0.1	—	0.1	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	—	V		
			4.5	—	—	0.1	—	0.1	—	0.1															
			6	—	—	0.1	—	0.1	—	0.1															
TTL Loads	V <sub>IL</sub> or V <sub>IH</sub>	4 5.2	4.5	—	—	0.26	—	0.33	—	0.4	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.26	—	0.33	—	0.4	—			V		
			6	—	—	0.26	—	0.33	—	0.4															
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V <sub>CC</sub> & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	—	μA		
Quiescent Device Current I <sub>CC</sub>	V <sub>CC</sub> or Gnd	0	6	—	—	8	—	80	—	160	V <sub>CC</sub> or Gnd	5.5	—	—	8	—	80	—	160	—	160	—	μA		
Additional Quiescent Device Current per Input pin: 1 unit load ΔI <sub>CC</sub> *											V <sub>CC</sub> -2.1 4.5 to 5.5	—	100	360	—	450	—	490	—	490	—	μA			

\*For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

**HCT Input Loading Table**

Input	Unit Loads*
A0 — A3	0.15
LE	0.85
E	0.3

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HARRIS SEMICONDUCTOR 27E D 430227J 0017984 4 HAS

**CD54/74HC4514, CD54/74HCT4514**  
**CD54/74HC4515, CD54/74HCT4515**

SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 6\text{ ns}$ )

CHARACTERISTIC	SYMBOL	$C_L$ (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay Select to Output	$t_{PHL}$	15	23	25	ns
	$t_{PLH}$				
$\overline{LE}$ to Output	$t_{PHL}$	15	19	21	ns
	$t_{PLH}$				
$\overline{E}$ to Output	$t_{PHL}$	15	14	17	ns
	$t_{PLH}$				
Power Dissipation Capacitance*	$C_{PD}$	—	70	75	pF

\* $C_{PD}$  is used to determine the dynamic power consumption, per package.  
 $PD = V_{CC}^2 f_i (C_{PD} + C_L)$  where:  
 $f_i$  = input frequency,  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	$V_{CC}$	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{LE}$ Pulse Width	$t_w$	2	75	—	—	95	—	—	—	110	—	—	—	ns	
		4.5	15	—	30	—	19	—	38	—	22	—	45		
		6	13	—	—	16	—	—	—	19	—	—	—		
Select to $\overline{LE}$ Set-up time	$t_{su}$	2	100	—	—	125	—	—	—	150	—	—	—	ns	
		4.5	20	—	20	—	25	—	25	—	30	—	30		
		6	17	—	—	21	—	—	—	26	—	—	—		
Select to $\overline{LE}$ Hold Time	$t_H$	2	0	—	—	0	—	—	—	0	—	—	—	ns	
		4.5	0	—	5	—	0	—	5	—	0	—	5		
		6	0	—	—	0	—	—	—	0	—	—	—		

SWITCHING CHARACTERISTICS ( $C_L = 50\text{ pF}$ , Input  $t_r, t_f = 6\text{ ns}$ )

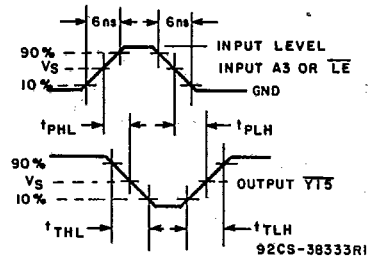
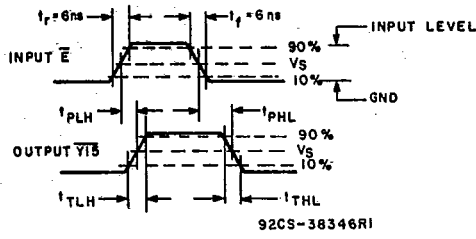
CHARACTERISTIC	SYMBOL	$V_{CC}$	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Select to Outputs	$t_{PLH}$ $t_{PHL}$	2	—	275	—	—	345	—	—	—	415	—	—	ns	
		4.5	—	55	—	55	—	69	—	69	—	83	—		83
		6	—	47	—	—	—	59	—	—	—	71	—		—
$\overline{LE}$ to Outputs	$t_{PLH}$ $t_{PHL}$	2	—	225	—	—	280	—	—	—	340	—	—	ns	
		4.5	—	45	—	50	—	56	—	63	—	68	—		75
		6	—	38	—	—	—	48	—	—	—	58	—		—
$\overline{E}$ to Outputs	$t_{PLH}$ $t_{PHL}$	2	—	175	—	—	220	—	—	—	265	—	—	ns	
		4.5	—	35	—	40	—	44	—	50	—	53	—		60
		6	—	30	—	—	—	37	—	—	—	45	—		—
Output Transition Time	$t_{TLH}$ $t_{THL}$	2	—	75	—	—	95	—	—	—	110	—	—	ns	
		4.5	—	15	—	15	—	19	—	19	—	22	—		22
		6	—	13	—	—	—	16	—	—	—	19	—		—
Input Capacitance	$C_i$	—	—	10	—	10	—	10	—	10	—	10	pF		

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 00J7985 6 HAS

**CD54/74HC4514, CD54/74HCT4514  
CD54/74HC4515, CD54/74HCT4515**

HARRIS SEMICONDUCTOR

27E D 4302271 0017986 8 HAS



	54/74HC	54/74HCT
Input Level	$V_{CC}$	3 V
Switching Voltage, $V_S$	50% $V_{CC}$	1.3 V

Propagation delay times and transition times for HC/HCT4515.

