### CD54HC138/3A CD54HCT138/3A

# Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

<b>OPEN</b> 7,9-15	GROUND 1-6,8	V <sub>cc</sub> (6V)	<b>OPEN</b> 7,9-15	GROUND 8	V <sub>cc</sub> (6V) 1-6,16
		16	7,9-15	8	1-6,16
1,3-10	. 0,0				
				OSCILLATOR	
OPEN	GROUND	1/2 V <sub>cc</sub> (3V)	V <sub>cc</sub> (6V)	50 kHz	25 kHz
	458	7.9-15	3,6,16	2	11
•	OPEN	<b>GROUND</b> - 4,5,8		0.12.1	OPEN GROUND 1/2 V <sub>cc</sub> (3V) V <sub>cc</sub> (6V) 50 kHz

NOTE: Each pin except Vcc and Gnd will have a resistor of 2k-47k ohms.

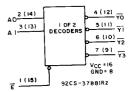
# **Dual 2-of-4-Line Decoder/Demultiplexer**

## CD54HC139/3A CD54HCT139/3A

The RCA-CD54HC139 and CD54HCT139 contain two independent binary to one-of-four decoders each with a single active low enable input ( $\overline{1E}$ , or  $\overline{2E}$ ). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally high outputs to go low.

If the enable input is high, all four outputs remain high. For demultiplexer operation, the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded. This device is functionally the same as the CD4556B and is pin compatible with it.

The outputs of these devices can drive 10 low-power Schottky TTL equivalent loads. The 54HCT logic family is functionally as well as pin equivalent to the 54 logic family.



#### **FUNCTIONAL DIAGRAM**

# **Package Specifications**

See Section 11, Fig. 11

### Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

	ĺ	TEST CONDITIONS						1			
					V <sub>IN</sub>						
		нс/нст		HC	HCT	LIMITS					
CHARACTERISTICS		V <sub>DD</sub>	V <sub>o</sub>	Io	V <sub>cc</sub> or GND	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>IL</sub> or V <sub>IH</sub>	MIN. MAX.		UNITS	
Quiescent	25° C	6			6, 0	_			8•		
Device Current	-55°C	6	_	_	6, 0	_	_	-	160•	μA	
lcc	+125°C	_									

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

#### **HCT INPUT LOADING TABLE**

INPUT	UNIT LOAD*				
All	0.7				

\*Unit load is  $\Delta l_{\rm CC}$  limit specified in Static Characteristics Chart, e.g., 360  $\mu$ A max. @ 25° C.

### CD54HC139/3A CD54HCT139/3A

### Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (CL = 50 pF, Input tr, tr = 6 ns)

		TEST CONDITIONS V <sub>cc</sub> V	LIMITS								
CHARACTERISTIC	SYMBOL		25° C				-55°C to +125°C				]
			нс		нст		54HC		54HCT		UNITS
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	1
Propagation Delay		2	_	145	_	I –	I –	220	_	-	
A0, A1 to Outputs  E to Outputs		4.5		29•	_	34•	-	44•	-	51•	
	t <sub>PLH</sub>	6	l —	25	_	_		38	_	_	ns
		2		135	_	-	_	205	<b>—</b>		
	+	4.5	_	27•	_	34•	_	41•	_	51•	
		6		23		_	_	35	_	l —	
Output Transition $ \begin{array}{c} t_{\text{TLH}} \\ t_{\text{THL}} \end{array} $	2	_	75	T —	_	I —	110		_	]	
	4.5	l —	15	_	15	l —	22	_	22		
	t <sub>THL</sub>	6	_	13	_	l —	_	19	l —	_	
Input Capacitance	Cı			10		10	_	10	_	10	pF

#### Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

01-4!-		STATIC BURN-	IN I	STATIC BURN-IN II				
Static	OPEN	GROUND	V <sub>cc</sub> (6V)	OPEN	GROUND	V <sub>cc</sub> (6V)		
CD54HC/HCT139	4,7,9,12	1-3,8,13-15	16	4-7,9-12	8	1-3,13-16		
	0.000	00011110	4/0.1/ /01/0	W (0)0	OSCILLATOR			
Dynamic	OPEN	GROUND	1/2 V <sub>cc</sub> (3V)	V <sub>cc</sub> (6V)	50 kHz	25 kHz		
CD54HC/HCT139	_	1,8,15	4-7,9-12	16	2,14	3,13		

NOTE: Each pin except Vcc and Gnd will have a resistor of 2k-47k ohms.

### CD54HC147/3A CD54HCT147/3A

# 10-to-4-Line Priority Encoder

The RCA-CD54HC147 and CD54HCT147 are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL).

The CD54HC147 and CD54HCT147 nine-input priority encoders accept data from nine active LOW inputs ( $\overline{I}_1$  to  $\overline{I}_3$ ) and provide binary representation on the four active LOW outputs ( $\overline{Y}_0$  to  $\overline{Y}_3$ ). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line  $\overline{I}_3$  having the highest priority.

These devices provide the 10-line-to-4-line priority encoding function by use of the implied decimal "zero." The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.



### Package Specifications

See Section 11, Fig. 11

**FUNCTIONAL DIAGRAM**