

**CD54AC258/3A**  
**CD54ACT258/3A**

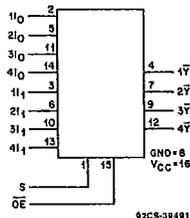
T-67-21-51

**Quad 2-Input Multiplexer with 3-State Inverting Outputs**

The RCA CD54AC258/3A and CD54ACT258/3A are quad 2-input multiplexers with 3-state outputs. These devices utilize the new RCA ADVANCED CMOS LOGIC technology. Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable (OE) is active LOW. When OE is HIGH, all of the outputs (Y) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the CD54AC/ACT258/3A. The state of the Select input determines the particular register from which the data comes. The CD54AC/ACT258/3A can also be used as function generators.

The CD54AC258/3A and CD54ACT258/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).



**Package Specifications**

See Section 11, Fig. 11

**FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT**



**Static Electrical Characteristics** (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			+25		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
3-State Leakage Current I <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5•	—	±10•	μA
Quiescent Supply Current (MSI) I <sub>CC</sub>	V <sub>CC</sub> or GND	0	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

**ACT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
Data	0.83
S	1.27
OE	1.27

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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**Burn-In Test-Circuit Connections**

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V <sub>CC</sub> (6V)	OPEN	GROUND	V <sub>CC</sub> (6V)
CD54AC/ACT258	4,7,9,12	1-3,5,6,8,10,11, 13-15	16	4,7,9,12	8	1-3,5,6,10,11,13-16
Dynamic	OPEN	GROUND	1/2 V <sub>CC</sub> (3V)	V <sub>CC</sub> (6V)	OSCILLATOR	
					50 kHz	25 kHz
CD54AC/ACT258	—	8,15	4,7,9,12	16	2,3,5,6,10,11, 13,14	1

NOTE: Each pin except V<sub>CC</sub> and Gnd will have a resistor of 2k-47k ohms.

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays I <sub>n</sub> to $\bar{Y}$	t <sub>PLH</sub>	1.5	—	100	ns
	t <sub>PHL</sub>	3.3*	2	14	
S to $\bar{Y}$	t <sub>PLH</sub>	1.5	—	168	ns
	t <sub>PHL</sub>	3.3	3.5	24	
$\bar{OE}$ to $\bar{Y}$	t <sub>PLZ</sub>	1.5	—	184	ns
	t <sub>PHZ</sub>	3.3	3.8	26	
	t <sub>PZL</sub>	5	2.5	14.7*	
	t <sub>PZH</sub>	5	2.5	14.7*	
Power Dissipation Capacitance	C <sub>PD§</sub>	—	130 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays I <sub>n</sub> to $\bar{Y}$	t <sub>PLH</sub>	5†	1.6	9.3*	ns
	t <sub>PHL</sub>	5	2.6	15.4*	
S to $\bar{Y}$	t <sub>PLH</sub>	5	2.6	15.4*	ns
	t <sub>PHL</sub>	5	2.6	15.4*	
$\bar{OE}$ to $\bar{Y}$	t <sub>PLZ</sub>	5	2.8	16.1*	ns
	t <sub>PHZ</sub>	5	2.8	16.1*	
	t <sub>PZL</sub>	5	2.8	16.1*	
	t <sub>PZH</sub>	5	2.8	16.1*	
Power Dissipation Capacitance	C <sub>PD§</sub>	—	170 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C<sub>PD</sub> is used to determine the dynamic power consumption per multiplexer.

For AC, P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>)

For ACT, P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) + V<sub>CC</sub> ΔI<sub>CC</sub> where  
f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage