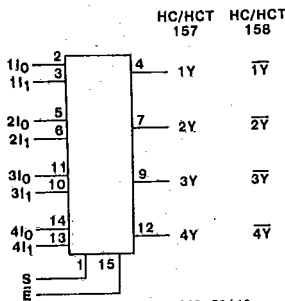


**CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158**

File Number 1642

HARRIS SEMICONDUCTOR 27E D 4302271 0017607 ? HAS

High-Speed CMOS Logic



Quad 2-Input Multiplexers

HC/HCT157 Non-Inverting
HC/HCT158 Inverting

Type Features:

- Buffered inputs
- Typical Propagation Delay (In to Output) = 10 ns (HC157) @ $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{ C}$

FUNCTIONAL DIAGRAM

The RCA-CD54/74HC157, 158 and CD54/74HCT157, 158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active LOW. When (\bar{E}) is HIGH, all of the outputs in the 158, the inverting type, (1Y-4Y) are forced HIGH and in the 157, the non-inverting type, all of the outputs (1Y-4Y) are forced LOW, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

The CD54HC157, 158 and CD54HCT157, 158 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC157, 158 and CD74HCT157, 158 are supplied in 16-lead dual-in-line plastic packages (E suffix). The CD74HC157, 158 and CD74HCT157, 158 are supplied in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ\text{ C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Sigmetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5\text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8\text{ V Max.}$, $V_{IH} = 2\text{ V Min.}$
CMOS Input Compatibility
 $I_1 \leq 1\text{ }\mu\text{A}$ @ V_{OL} , V_{OH}

FUNCTION TABLE

Enable	Select Input	Data Inputs		Output	
				157	158
\bar{E}	S	I_0	I_1	Y	\bar{Y}
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.

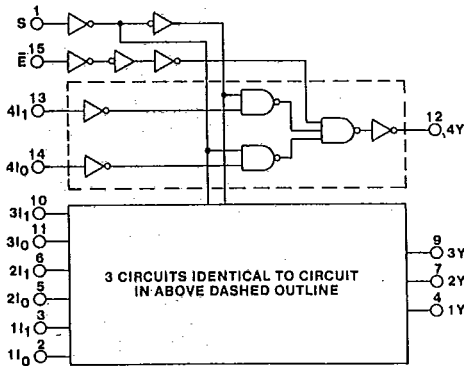
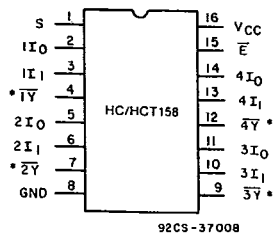
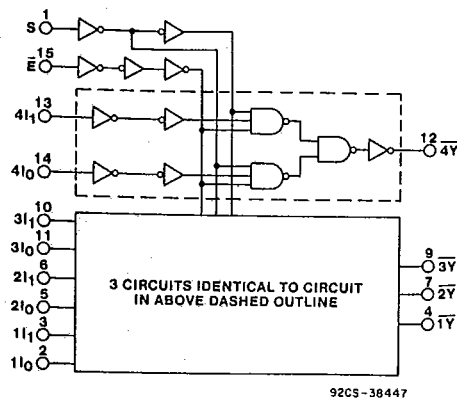


Fig. 1 - Logic Diagram for HC/HCT157.

92CM-38446

CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158



* For HC/HCT157 these outputs are 1Y, 2Y, 3Y, 4Y.

TERMINAL ASSIGNMENT

Fig. 2 - Logic Diagram for HC/HCT158.

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to +7 V
- DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < -0.5 V OR V_I > V_{CC} + 0.5 V) ±20 mA
- DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_O < -0.5 V OR V_O > V_{CC} + 0.5 V) ±20 mA
- DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} + 0.5 V) ±25 mA
- DC V_{CC} OR GROUND CURRENT (I_{CC}): ±50 mA
- POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) Derate Linearly at 6 mW/°C to 70 mW
- OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H -55 to +125°C
PACKAGE TYPE E, M -40 to +85°C
- STORAGE TEMPERATURE (T_{stg}) -65 to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V _{in} , V _{out}	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t _r , t _f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

HARRIS SEMICONDUCTOR 27E D 4302271 0017608 9 HAS

T-67-21-51

**CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158**

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC157/158/CD54HC157/158										CD74HCT157/158/CD54HCT157/158										UNITS			
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE			54HC TYPE			TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE				54HCT TYPE		
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C			-55/ +125°C			V _I V	V _{CC} V	+25°C			-40/ +85°C				-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max		Min	Max	
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5			2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	to			—	—	—	—	—	—	—		
			6	4.2	—	—	4.2	—	4.2	—	—	—	5.5			—	—	—	—	—	—	—		
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5			—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	to			—	—	—	—	—	—	—		
			6	—	—	1.8	—	1.8	—	1.8	—	—	5.5			—	—	—	—	—	—	—		
High-Level Output Voltage V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V	
CMOS Loads			4.5	4.4	—	—	4.4	—	4.4	—	—													
			6	5.9	—	—	5.9	—	5.9	—	—													
TTL Loads	V _{IL} or V _{IH}											V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	3.7	—	V	
			-4	4.5	3.98	—	—	3.84	—	3.7	—													
			5.2	6	5.48	—	—	5.34	—	5.2	—													
Low-Level Output Voltage V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	—	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	V	
CMOS Loads			4.5	—	—	0.1	—	0.1	—	0.1	—													
			6	—	—	0.1	—	0.1	—	0.1	—													
TTL Loads	V _{IL} or V _{IH}											V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	V	
			4	4.5	—	—	0.26	—	0.33	—	0.4													
			5.2	6	—	—	0.26	—	0.33	—	0.4													
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA	
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	—	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	—	160	μA	
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI _{CC} *												V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	490	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT 157	HCT 158
I (ALL)	0.95	0.4
\bar{E}	0.6	0.6
S	3	2.8

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 0017609 0 HAS

**CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158**

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES				UNITS
			HC157	HCT157	HC158	HCT158	
Data to Output	15	t_{PHL} t_{PLH}	10	12	11	13	ns
Enable to Output	15	t_{PHL} t_{PLH}	11	12	13	15	ns
Select to Output	15	t_{PHL} t_{PLH}	12	15	12	14	ns
Power Dissipation Capacitance*		C_{PD}	62	70	35	35	pF

* C_{PD} is used to determine the dynamic power consumption, per multiplexer.

$P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where: f_i = input frequency. C_L = output load capacitance.
 f_o = output frequency. V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

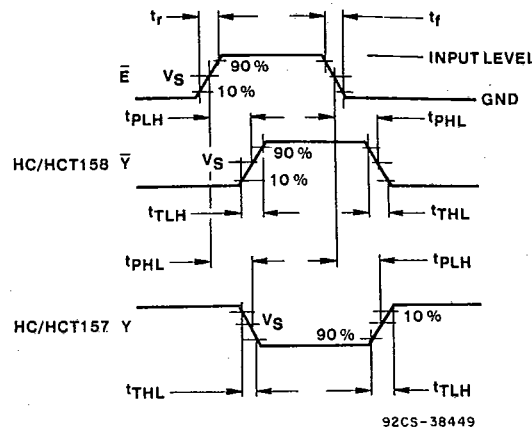
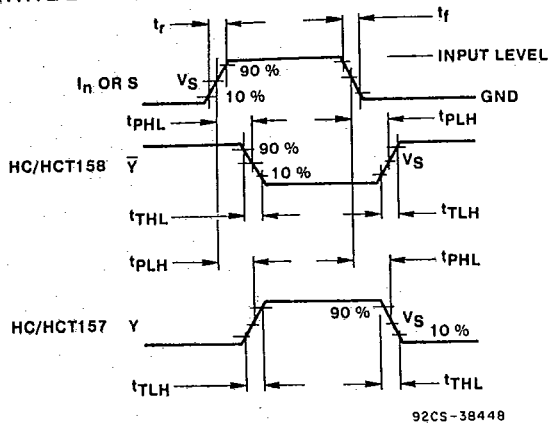
CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Data to Output (Figure 3) HC/HCT157	t_{PLH} t_{PHL}	2 4.5 6	— — —	125 25 21	— — —	— 30 —	— — —	155 31 26	— 38 —	— — —	190 38 32	— — —	— 45 —	ns	
Propagation Delay Enable to Output (Figure 4) HC/HCT157	t_{PLH} t_{PHL}	2 4.5 6	— — —	135 27 23	— — —	— 30 —	— — —	170 34 29	— 38 —	— — —	205 41 35	— — —	— 45 —	ns	
Propagation Delay Select to Output (Figure 3) HC/HCT157	t_{PLH} t_{PHL}	2 4.5 6	— — —	145 29 25	— — —	— 37 —	— — —	180 36 31	— 46 —	— — —	220 44 38	— — —	— 56 —	ns	
Propagation Delay Data to Output (Figure 3) HC/HCT158	t_{PLH} t_{PHL}	2 4.5 6	— — —	140 28 24	— — —	— 32 —	— — —	175 35 30	— 40 —	— — —	210 42 36	— — —	— 48 —	ns	
Propagation Delay Enable to Output (Figure 4) HC/HCT158	t_{PLH} t_{PHL}	2 4.5 6	— — —	160 32 27	— — —	— 37 —	— — —	200 40 34	— 46 —	— — —	240 48 41	— — —	— 56 —	ns	
Propagation Delay Select to Output (Figure 3) HC/HCT158	t_{PLH} t_{PHL}	2 4.5 6	— — —	150 30 26	— — —	— 35 —	— — —	190 38 33	— 44 —	— — —	225 45 38	— — —	— 53 —	ns	
Output Transition Time (Figure 3 or 4)	t_{TLH} t_{THL}	2 4.5 6	— — —	75 15 13	— — —	— 15 —	— — —	95 19 16	— — —	— 19 —	110 22 19	— — —	— 22 —	ns	
Input Capacitance	C_{in}		—	10	—	10	—	10	—	10	—	10	—	10	pF

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 0017610 ? HAS

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CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158

HARRIS SEMICOND SECTOR 27E D ■ 4302271 0017611 9 ■ HAS



	54/74HC	54/74HCT
Input Level	V _{cc}	3 V
V _s	50% V _{cc}	1.3 V

Fig. 3 - Inputs or select to output propagation delays and output transition times.

Fig. 4 - Enable to output propagation delays and output transition times.