2-A Power-Switching Transistors

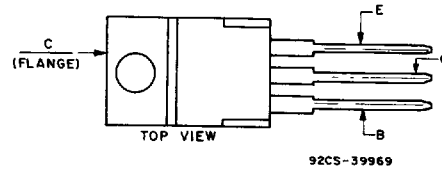
High-Voltage N-P-N Types for Off-Line Power Supplies and Other Switching Applications

Features:

- *Performance information tailored for switching applications*
- *100° C maximum limits specified for:*
  - *Switching times*
  - *Saturation voltages*
  - *Leakage currents*
- *300 to 400V $V_{CEO(sus)}$*
- *Very fast turn-off $t_f < 180$ nsec (typ.)@1.5A*

The D44TD-series of n-p-n power transistors are designed for use in switching applications requiring high-voltage capability, fast switching speeds, and low-saturation voltages. They are particulary suited for off-line switching power supplies, solid state lighting ballast, inverters, solenoid/relay drivers, and deflection circuits.

TERMINAL DESIGNATIONS



JEDEC TO-220AB

POWER TRANSISTORS

MAXIMUM RATINGS (T_A = 25° C) (unless otherwise specified)

RATING	SYMBOL	D44TD3	D44TD4	D44TD5	UNITS
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Collector-Emitter Voltage	V_{CEX}	300	350	400	Volts
Collector-Emitter Voltage	V_{CEV}	400	500	600	Volts
Emitter Base Voltage	V_{EBO}	7	7	7	Volts
Collector Current — Continuous Peak(1)	I_C I_{CM}	2 4	2 4	2 4	A
Base Current — Continuous Peak(1)	I_B I_{BM}	0.5 1	0.5 1	0.5 1	A
Total Power Dissipation @ Tc = 25°C @ Tc = 100°C Derate above 25°C	P_D	50 20 0.4	50 20 0.4	50 20 0.4	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	2.5	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	75	75	°C/W
Maximum Lead Temperature for Soldering Purpose: ⅛" from Case for 5 Seconds	T_L	260	260	260	°C

(1) Pulse condition, $t_p \leq 5$msec.

D44TD Series

ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

CHARACTERISTIC		SYMBOL	MIN	MAX	UNIT
OFF CHARACTERISTICS[1]				T-35-19	
Collector-Emitter Sustaining Voltage (I_C = 25mA, I_B = 0)	D44TD3 D44TD4 D44TD5	$V_{CEO(sus)}$	300 350 400	— — —	Volts
Collector-Emitter Voltage (I_C = 2.0mA, I_{B1} = I_{B2} = .4A) (V_{BE} = -5V, L = 200 μh)	D44TD3 D44TD4 D44TD5	V_{CEX}	300 350 400	— — —	Volts
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(OFF)}$ = -1.5V) (V_{CEV} = Rated Value, $V_{BE(OFF)}$ = -1.5V, T_C = 100°C)		I_{CEV}	— —	0.1 1.0	mA
Emitter Cutoff Current (V_{EB} = 7V, I_C = 0)		I_{EBO}	—	1.0	mA
SECOND BREAKDOWN					
Second Breakdown with Base Forward Biased		FBSOA	SEE FIGURE 13		
Clamped Inductive SOA with Base Reversed Bias		RBSOA	SEE FIGURE 14		
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 1A, V_{CE} = 2V) (I_C = 2A, V_{CE} = 3V)		h_{FE}	8 5	— —	—
Collector-Emitter Saturation Voltage (I_C = 1A, I_B = .2A) (I_C = 2A, I_B = .4A) (I_C = 1A, I_B = .2A, T_C = 100°C)		$V_{CE(SAT)}$	— — —	0.6 1.0 1.0	Volts
Base-Emitter Saturation Voltage (I_C = 2A, I_B = .4A) (I_C = 2A, I_B = .4A, T_C = 100°C)		$V_{BE(SAT)}$	— —	1.2 1.2	Volts
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = .25A, V_{CE} = 10V, f_{test} = 1.0 MHz)		f_T	15	50	MHz
Output Capacitance (V_{CB} = 10V, I_E = 0, f = 0.1 MHz)		C_{OB}	10	25	pF

SWITCHING CHARACTERISTICS

			MAXIMUM		
Resistive Load (See Figure 17 for Test Circuit)		T_C	25°C	100°C	
Delay Time	V_{CC} = 250V, I_C = 1.5A	t_d	.06	.08	μs
Rise Time	I_{B1} = I_{B2} = 0.3A, t_p = 25 μsec	t_r	0.6	0.8	μsec
Storage Time		t_s	2.5	3.0	μsec
Fall Time		t_f	0.5	0.8	μsec
Inductive Load, Clamped (See Figure 17 for Test Circuit)					
Storage Time	V_{CLAMP} = 250V, I_C = 1.5A,	t_{sv}	3.0	3.5	μs
Fall Time	I_{B1} = I_{B2} = 0.3A, t_p = 25μsec	t_f	0.3	0.6	μsec
	$V_{BE(OFF)}$ = -5V	TYPICAL			
Storage Time	L = 200 μh	t_s	2.1	2.6	μsec
Fall Time		t_f	0.18	0.23	μsec

(1) Pulse Duration = 300μs, Duty Factor ≤ 2%. Do not measure on a curve tracer.

TYPICAL DC CHARACTERISTICS T-35-19

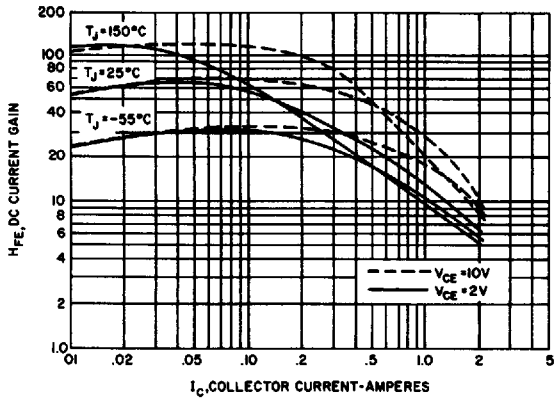


FIGURE 1. DC CURRENT GAIN

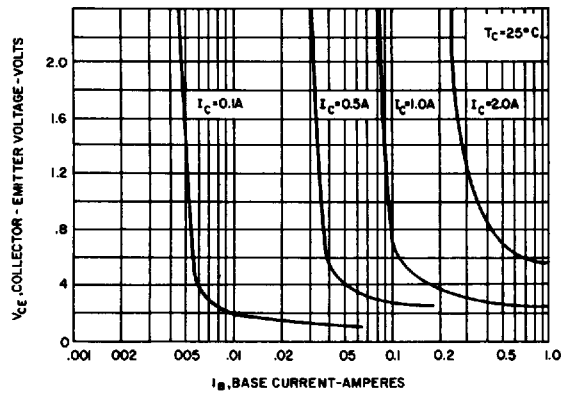


FIGURE 2. COLLECTOR SATURATION REGION

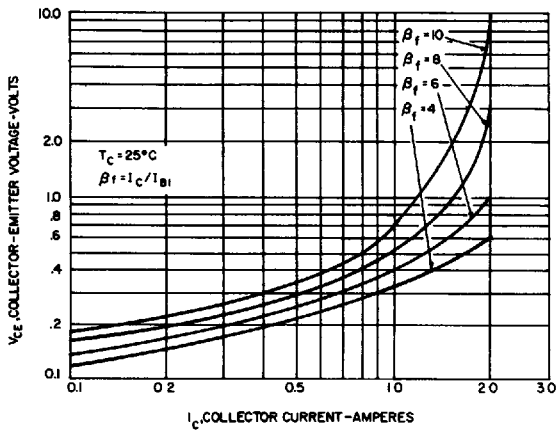


FIGURE 3. $V_{CE(SAT)}$ VS. I_C, T_C = 25°C

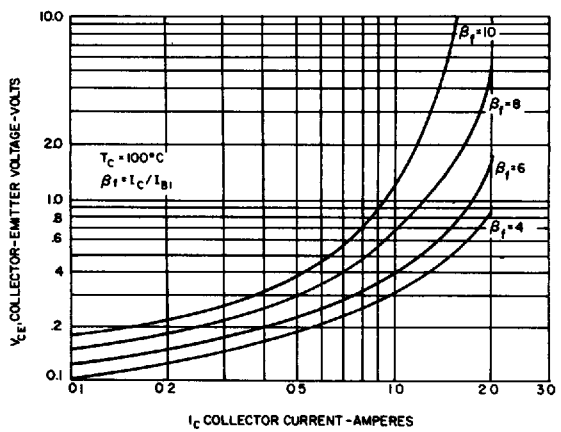


FIGURE 4. $V_{CE(SAT)}$ VS. I_C, T_C = 100°C

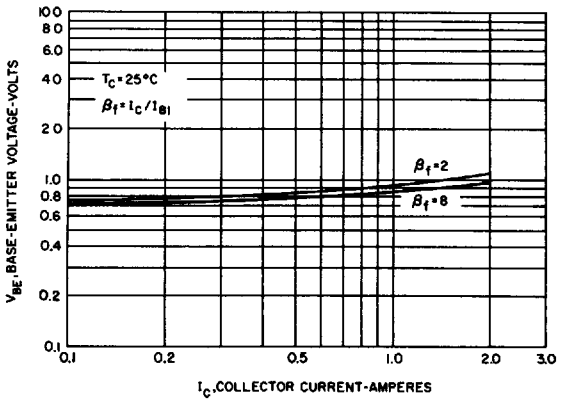


FIGURE 5. $V_{BE(SAT)}$ VS. I_C

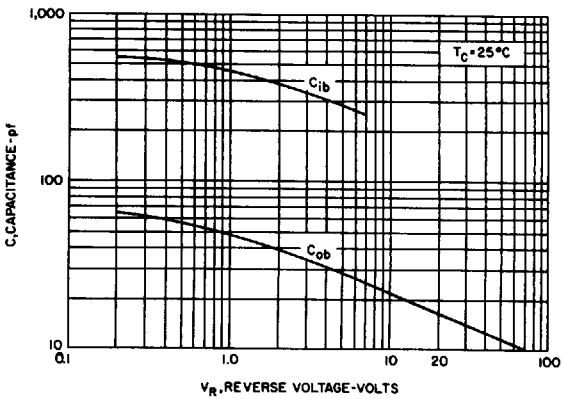


FIGURE 6. CAPACITANCE

POWER TRANSISTORS

D44TD Series

TYPICAL SWITCHING CHARACTERISTICS

T-35-19

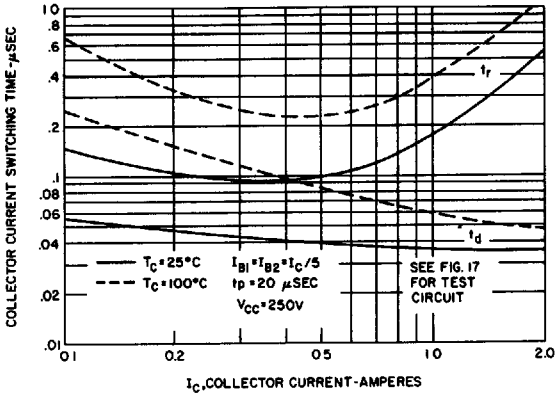


FIGURE 7. TURN-ON TIME RESISTIVE LOAD

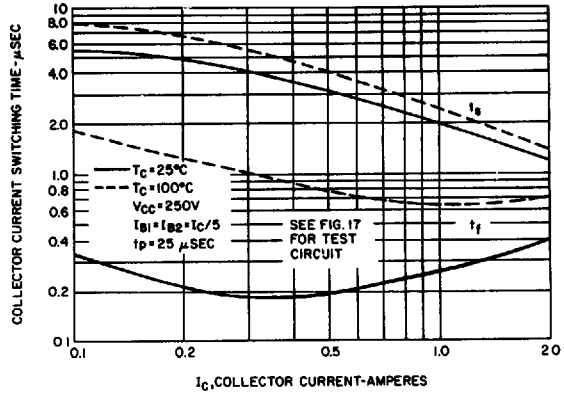


FIGURE 8. TURN-OFF TIME RESISTIVE LOAD

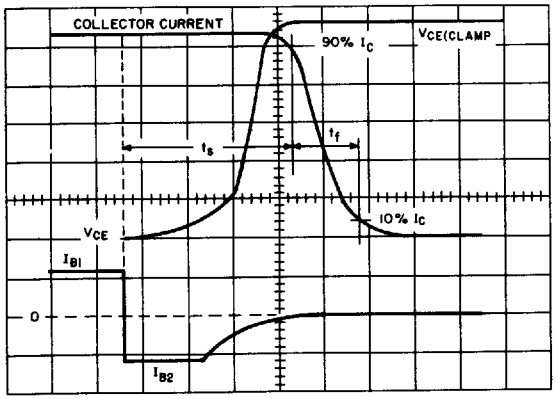


FIGURE 9. INDUCTIVE TURN-OFF WAVEFORMS

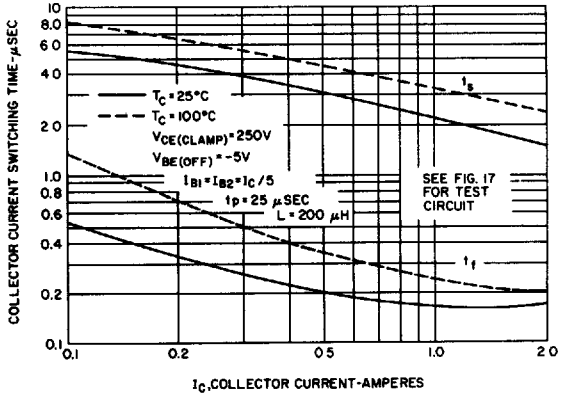


FIGURE 10. CLAMPED INDUCTIVE TURN-OFF TIME

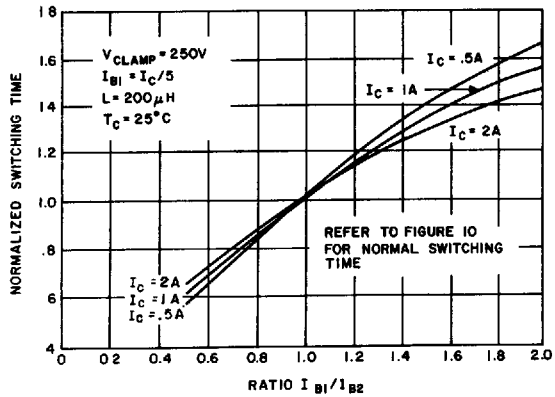


FIGURE 11. STORAGE TIME VARIATION WITH I_{B2}

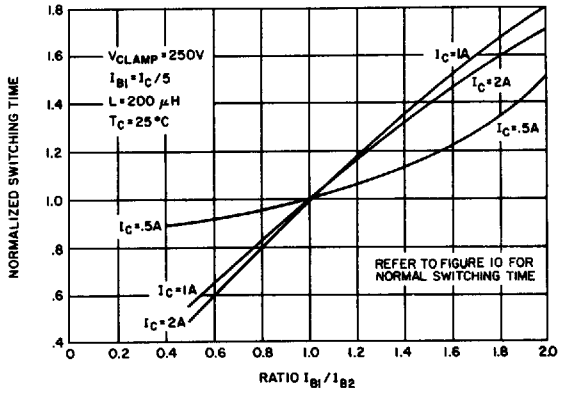


FIGURE 12. FALL TIME VARIATION WITH I_{B2}

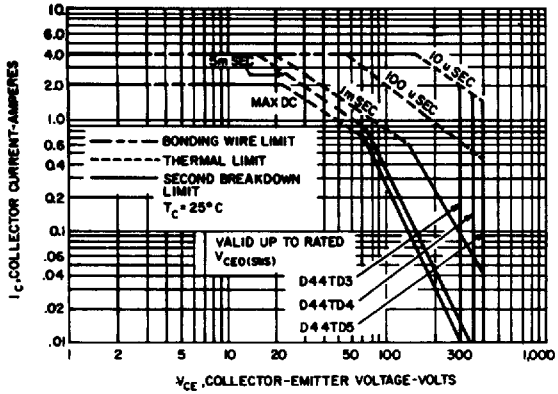


FIGURE 13. FORWARD BIAS SAFE OPERATING AREA

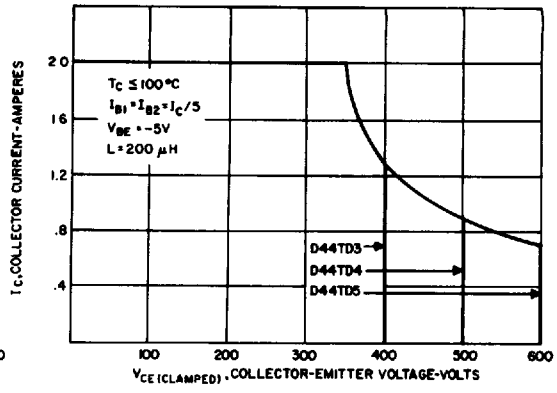


FIGURE 14. CLAMPED REVERSE BIAS SAFE OPERATING AREA

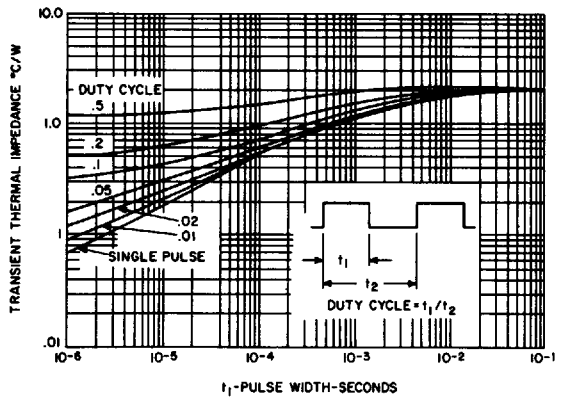


FIGURE 15. TRANSIENT THERMAL RESPONSE

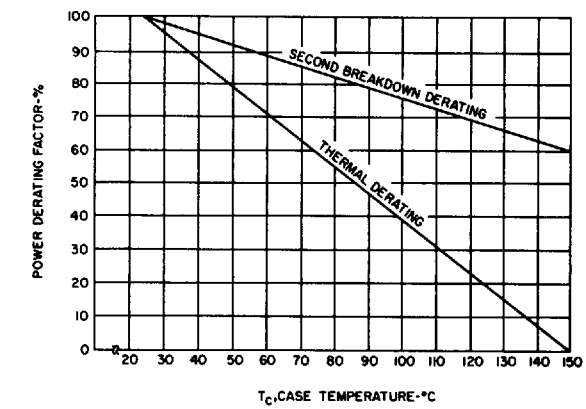


FIGURE 16. POWER DERATING CURVE

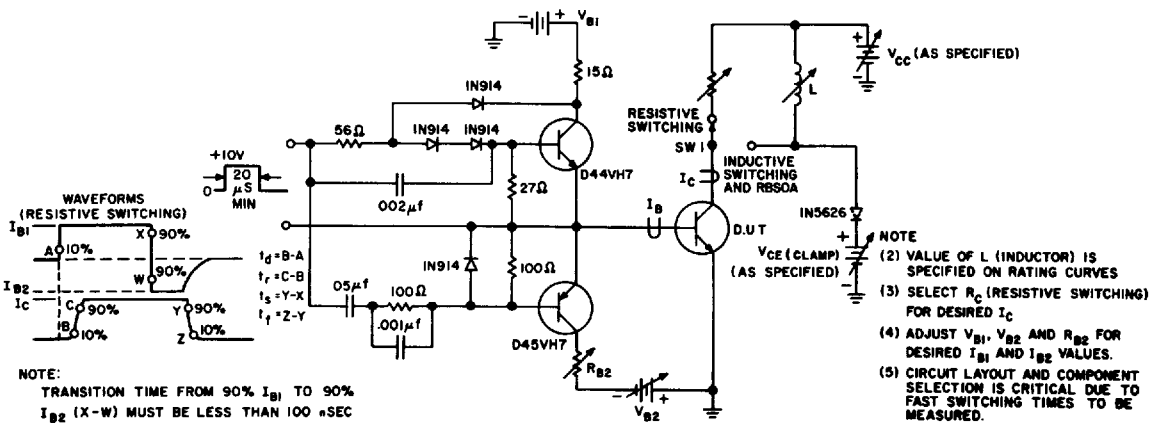


FIGURE 17. TEST CIRCUIT FOR SWITCHING TIMES AND RBSOA