HARRIS SEMICONDUCTOR

HFA3127/883

February 1995

Ultra High Frequency Transistor Array

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **NPN Transistor (f_T). . . . . .8GHz (Typ)**
- **NPN Current Gain . . . . . 40 (Min)**
- **NPN Early Voltage (VA) . . . . . 20 (Min)**
- **Noise Figure (50Ω) at 1.0GHz . . . . . 3.5dB (Typ)**
- **Collector-to-Collector Leakage. . . . . .<1pA (Typ)**
- **Complete Isolation Between Transistors**
- **Pin Compatible with Industry Standard 3XXX Series**

Applications

- **VHF/UHF Amplifiers**
- **VHF/UHF Mixers**
- **IF Converters**
- **Synchronous Detectors**

Description

The HFA3127/883 is an Ultra High Frequency Transistor Array fabricated on the Harris Semiconductor complementary bipolar UHF-1 process. This array consists of five dielectrically isolated transistors on a common monolithic substrate. The high f_T (8GHz) and low noise figure (3.5dB) of these transistors make them ideal for high frequency amplifier and mixer applications.

The HFA3127/883 is an all-NPN array. Access is provided to each of the terminals of the individual transistors for maximum application flexibility. The monolithic construction of the array provides close electrical and thermal matching of the five transistors.

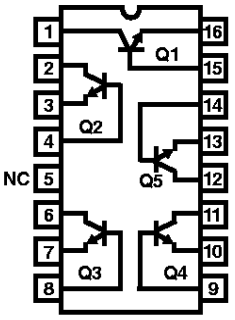
SMD 5962-9474901MEA version is also available from Harris Semiconductor.

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
HFA3127MJ/883	-55°C to +125°C	16 Lead CerDIP

Pinout

HFA3127/883
(CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3967**
Spec Number **511120**

Absolute Maximum Ratings

Collector to Emitter Voltage 8.0V
Collector to Base Voltage 12.0V
Emitter to Base Voltage 5.5V
Collector Current at 100% Duty Cycle, 175°C T_J 11.3mA
Storage Temperature Range . . . . . -65°C to 150°C
Junction Temperature (DIE) . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Rating . . . . . <2000V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	80°C/W	24°C/W

Maximum Package Power Dissipation at +75°
CerDIP Package 1.25W
Derating Factor Above +75°C
CerDIP Package . . . . . 12.5mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100µA, I_E = 0	1	+25°C	12	-	V
			2, 3	+125°C to -55°C	12	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 100µA, I_B = 0	1	+25°C	8	-	V
			2, 3	+125°C to -55°C	8	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CES}$	I_C = 100µA, Base Shorted tp Emitter	1	+25°C	10	-	V
			2, 3	+125°C to -55°C	10	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0	1	+25°C	5.5	-	V
			2, 3	+125°C to -55°C	5.5	-	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 6V, I_B = 0	1	+25°C	-	100	nA
			2, 3	+125°C to -55°C	-	100	nA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 8V, I_E = 0	1	+25°C	-	10	nA
			2, 3	+125°C to -55°C	-	10	nA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10mA, I_B = 1mA	1	+25°C	-	0.5	V
			2, 3	+125°C to -55°C	-	0.5	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10mA	1	+25°C	-	0.95	V
			2, 3	+125°C to -55°C	-	1.05	V
DC Forward Current Transfer Ratio	h_{FE}	I_C = 10mA, V_{CE} = 2V	1	+25°C	40	-	-
			2, 3	+125°C to -55°C	20	-	-
Early Voltage	V_A	I_C = 10mA, V_{CE} = 3.5V	1	+25°C	20	-	V
			2, 3	+125°C to -55°C	20	-	V

TABLE 2. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 3 Intentionally Left Blank.

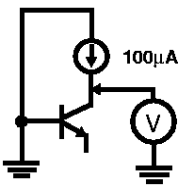
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

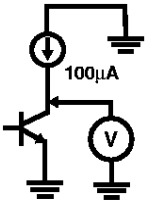
NOTE:

1. PDA applies to Subgroup 1 only.

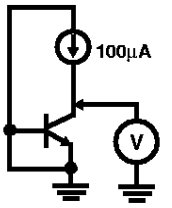
Test Circuits (Applies to Table 1)



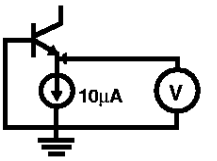
BVCBO



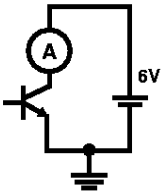
BVCEO



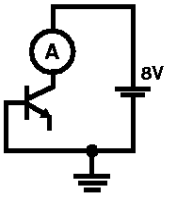
BVCES



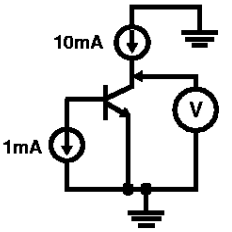
BVEBO



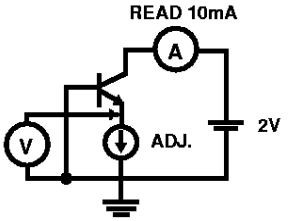
ICEO



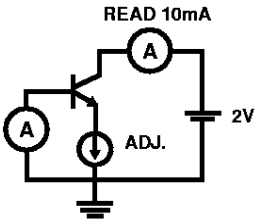
ICBO



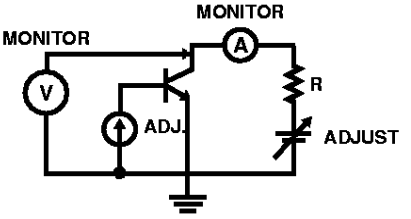
VCE(SAT)



VBE

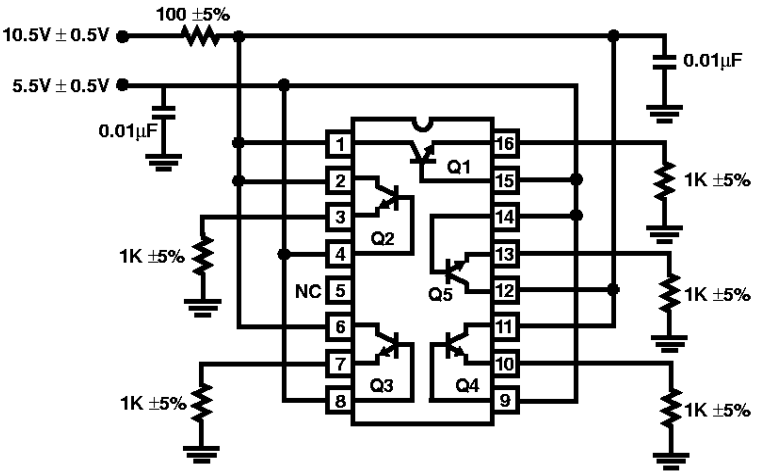


HFE



VA

Burn-In Circuit



Die Characteristics

DIE DIMENSIONS:
52 x 52.8 x 15 1mils
1320µm x 1340µm x 381µm ± 25.4µm

METALIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.5kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

WORST CASE CURRENT DENSITY:
3.04 x 10^5A/cm^2

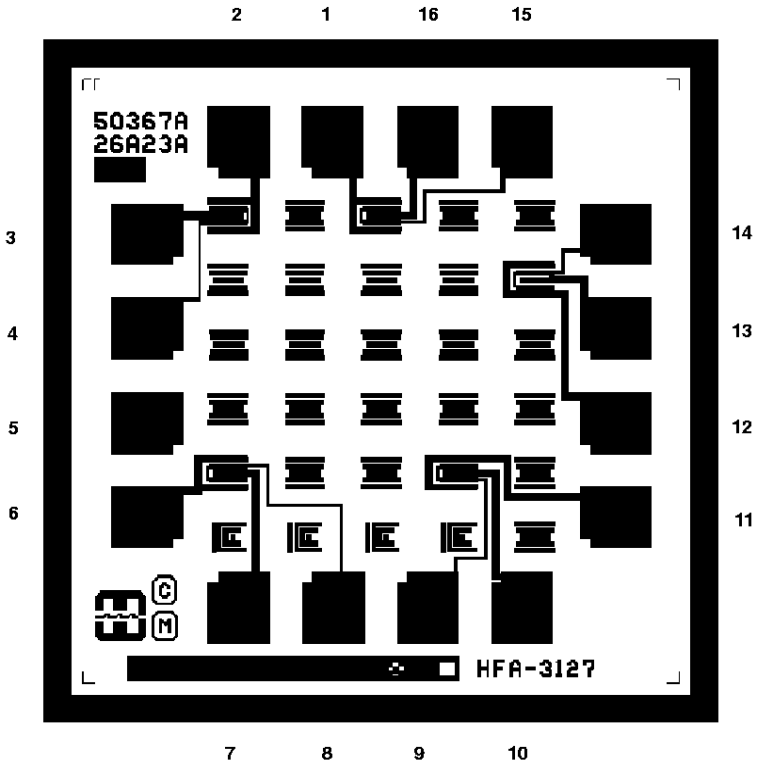
TRANSISTOR COUNT: 5

SUBSTRATE POTENTIAL: Floating

Metallization Mask Layout

Pad numbers correspond to the 16 pin DIP pinout.

HFA3127/883



DESIGN INFORMATION

February 1995

Ultra High Frequency Transistor Array

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Electrical Specifications at $T_A = +25^oC$

PARAMETERS	TEST CONDITIONS	TYP	UNITS
Noise Figure	f = 1.0GHz, V_{CE} = 5V, I_C = 5mA, Z_S = 50Ω	3.5	dB
f_T Current Gain-Bandwidth Product	I_C = 1mA, V_{CE} = 5V	5.5	GHz
	I_C = 10mA, V_{CE} = 5V	8	GHz
Power Gain-Bandwidth Product, f_{MAX}	I_C = 10mA, V_{CE} = 5V	2.5	GHz
Collector-to-Collector Leakage		1	pA
Collector-to-Base Capacitance	0V, 1MHz	1.6	pF
Base-to-Emitter Capacitance	0V, 1MHz	2.2	pF
Collector-to-Emitter Capacitance	0V, 1MHz	1.9	pF

NOTE: Package interlead capacitance is taken into account for all capacitance measurements.

Typical Performance Curves

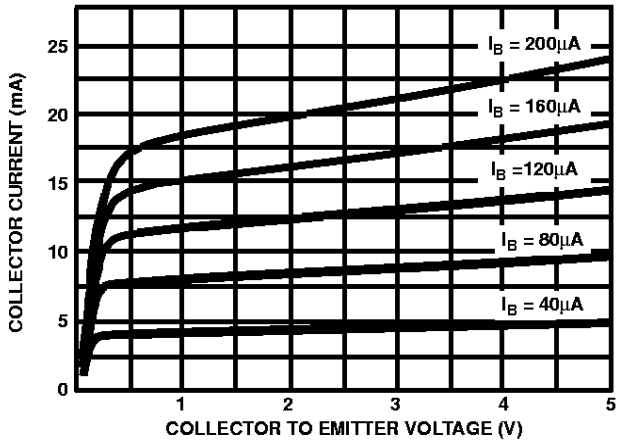


FIGURE 1. NPN COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

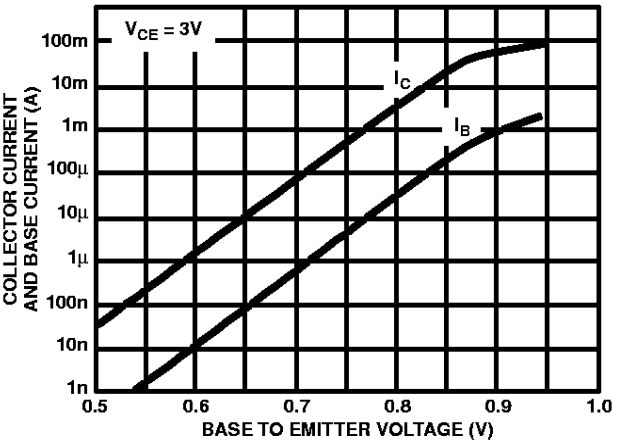


FIGURE 2. NPN COLLECTOR AND BASE CURRENTS vs BASE TO EMITTER VOLTAGE

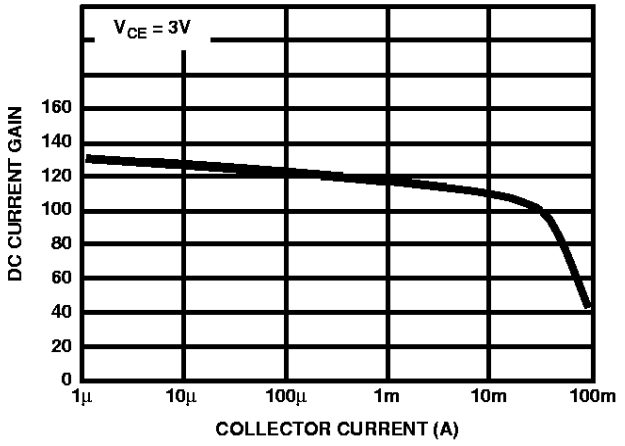


FIGURE 3. NPN DC CURRENT GAIN vs COLLECTOR CURRENT

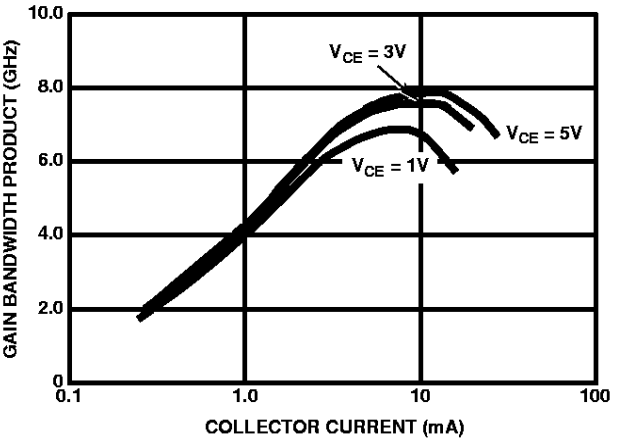
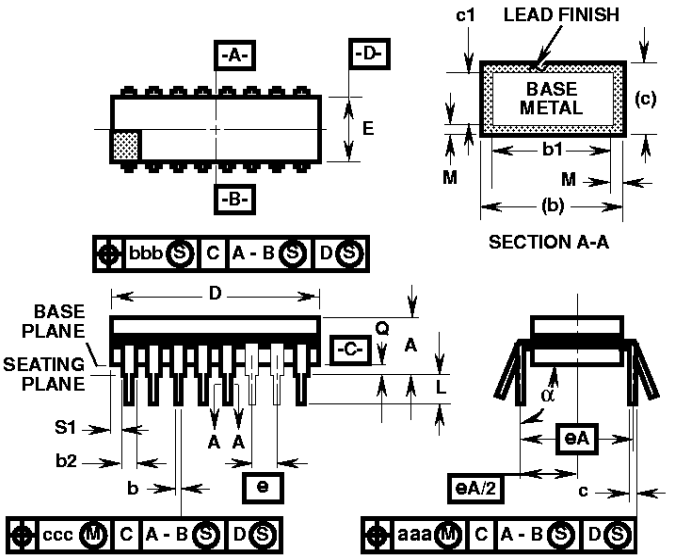


FIGURE 4. NPN GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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