MP2161A

2A, 6V, 1.5MHz, 17µA I_Q, COT Synchronous Step-Down Converter in 8-pin TSOT23

The Future of Analog IC Technology

DESCRIPTION

The MP2161A is a monolithic, step-down, switch-mode converter with built-in internal power MOSFETs. It achieves a 2A continuous output current from a 2.5V to 6V input voltage range with excellent load and line regulation. The output voltage is regulated as low as 0.6V.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2161A is available in a small TSOT23-8 package and requires a minimum number of readily available, standard, external components.

The MP2161A is ideal for a wide range of applications including high performance DSPs, FPGAs, PDAs, and portable instruments.

FEATURES

- Very Low I_Q: 17µA
- Default 1.5MHz Switching Frequency
- 1.5% V_{FB} Accuracy
- EN and Power Good for Power Sequencing
- Wide 2.5V to 6V Operating Input Range
- Output Adjustable from 0.6V
- Up to 2A Output Current
- 100% Duty Cycle in Dropout
- 110mΩ and 60mΩ Internal Power MOSFET Switches
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- Available in a TSOT23-8 Package

APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery Powered Devices
- Low Voltage I/O System Power

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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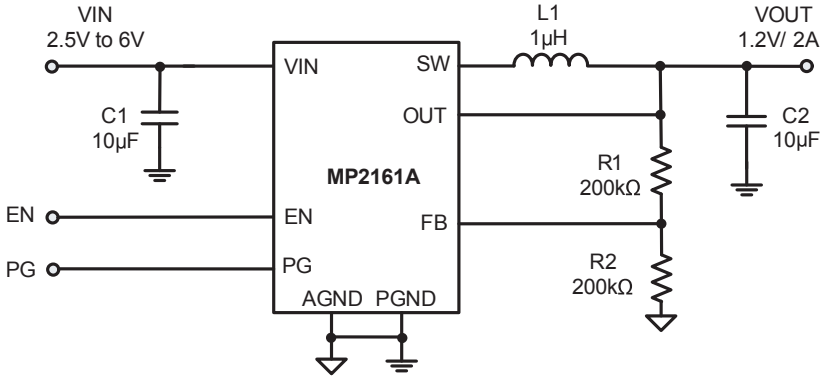
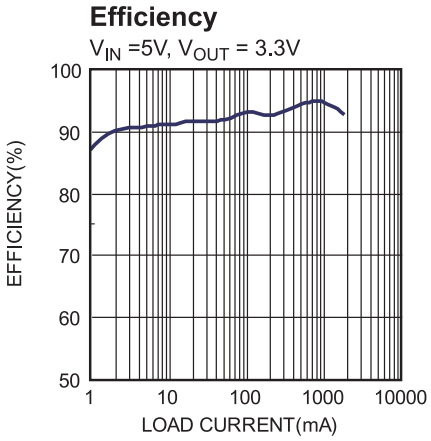
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2161AGJ	TSOT23-8	*See Below*

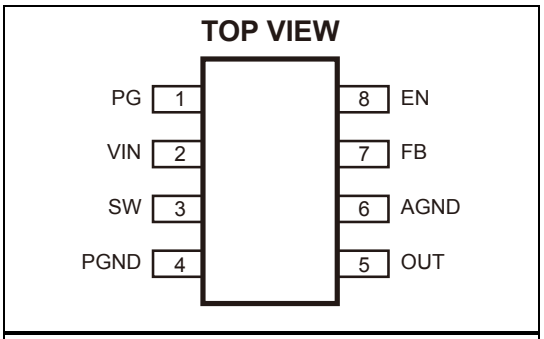
* For Tape & Reel, add suffix –Z (e.g. MP2161AGJ–Z)

TOP MARKING

|AKRY

AKR: Product code of MP2161AGJ
Y: Year code

PACKAGE REFERENCE



TSOT23-8

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} .....
-0.3V (-1.5V for <20ns&-4V for <8ns) to 6.5V (10V for <10ns)
All other pins ..... -0.3V to 6.5 V
Junction temperature ..... 150°C
Lead temperature..... 260°C
Continuous power dissipation (T_A = +25°C) **(2)**
……..... 1.25W
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.5V to 6V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-8	100	 55	... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	2.5V ⩽ V_{IN} ⩽ 6V, T_A = 25°C	-1.5	0.600	+1.5	V/%
		T_A = 0°C to +60°C	-2		+2	
		T_A = -40°C to +85°C (6)	-2.5		+2.5	
Feedback current	I_{FB}	V_{FB} = 0.6V		10	50	nA
PFET switch on resistance	R_{DSON_P}			110		mΩ
NFET switch on resistance	R_{DSON_N}			60		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V and 6V		0	1	μA
PFET current limit			2.6	3.2	4.0	A
On time	T_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		166		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		220		
Switching frequency	F_s	V_{OUT} = 1.2V, T_A = 25°C	-20	1500	+20	kHz/%
		T_A = -40°C to +85°C(6)	-25	1500	+25	kHz/%
Minimum off time(6)	$T_{MIN-OFF}$			60		ns
Soft-start time	T_{SS-ON}	V_{OUT} from 10% to 90%	0.6	1.15	1.7	ms
Power good upper trip threshold	PG_H	FB voltage respect to the regulation		+10		%
Power good lower trip threshold	PG_L			-10		%
Power good delay	PG_D			50		μs
Power good sink current capability	V_{PG-L}	Sink 1mA			0.4	V
Power good logic-high voltage	V_{PG-H}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
Power good internal pull-up resistor	R_{PG}			550		kΩ
Under-voltage lockout threshold—rising			2.15	2.3	2.45	V
Under-voltage lockout threshold—hysteresis				260		mV
EN input logic-low voltage					0.4	V
EN input logic-high voltage			1.2			V
EN input current		V_{EN} = 2V		1.5		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, V_{IN} = 3V		20	100	nA
Supply current (quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 5V		17	20	μA
Thermal shutdown(5)				150		°C
Thermal hysteresis(5)				30		°C

NOTES:

5) Guaranteed by design.
6) Guaranteed by characterization test.

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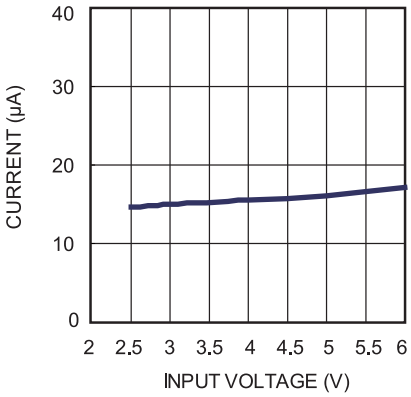
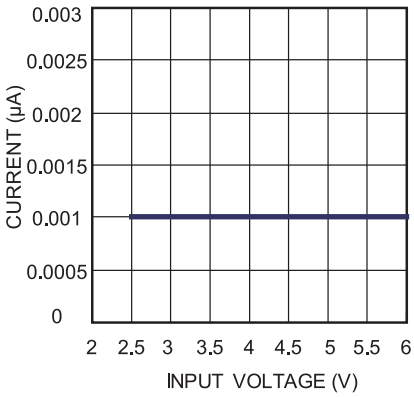
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25ºC, unless otherwise noted.

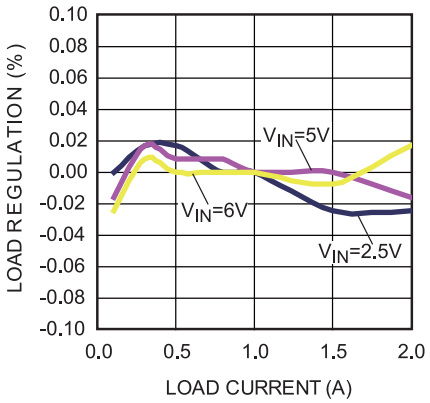
Quiescent Current vs. Input Voltage



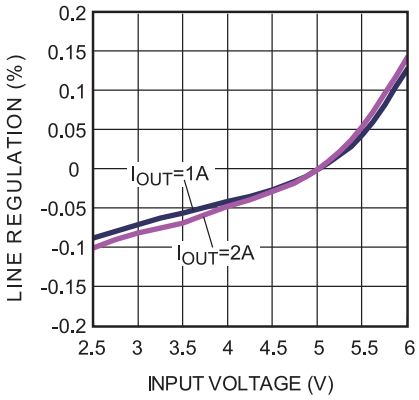
Shutdown Current vs. Input Voltage



Load Regulation

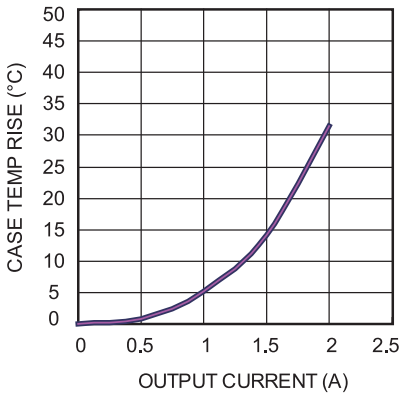


Line Regulation



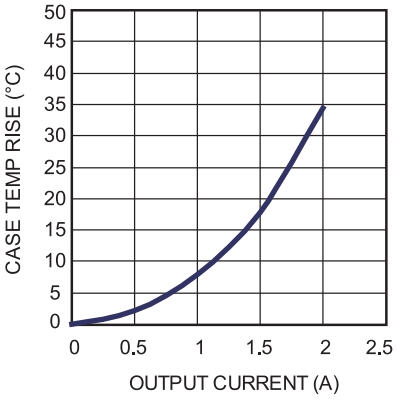
Case Temperature Rise

V_{IN}=3V, V_{OUT}=1.2V

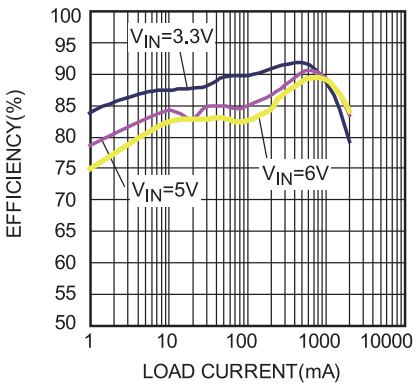


Case Temperature Rise

V_{IN}=5V, V_{OUT}=3.3V

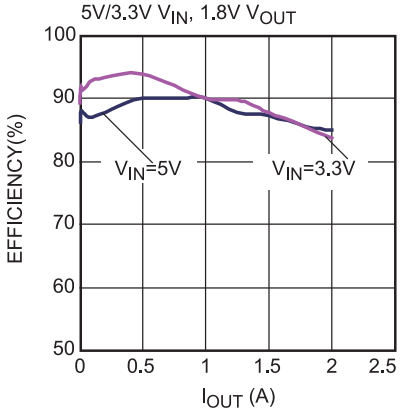


Efficiency



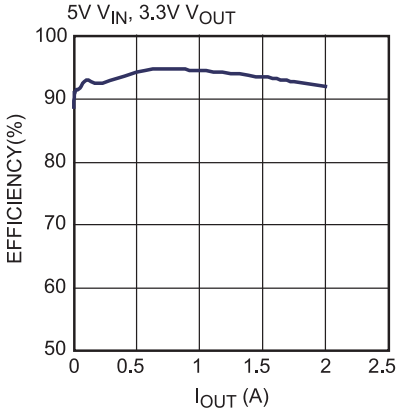
Efficiency

5V/3.3V V_{IN}, 1.8V V_{OUT}



Efficiency

5V V_{IN}, 3.3V V_{OUT}



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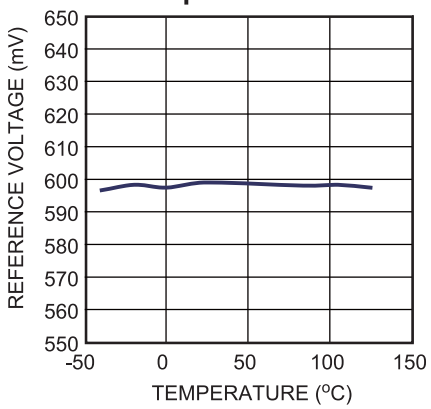
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

Reference Voltage vs. Temperature



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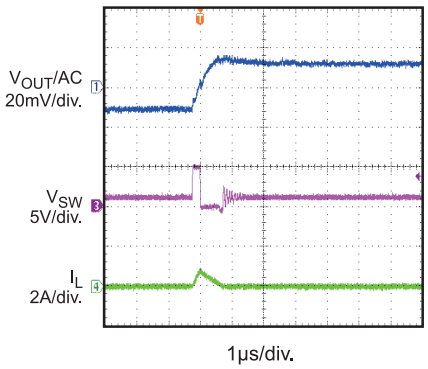
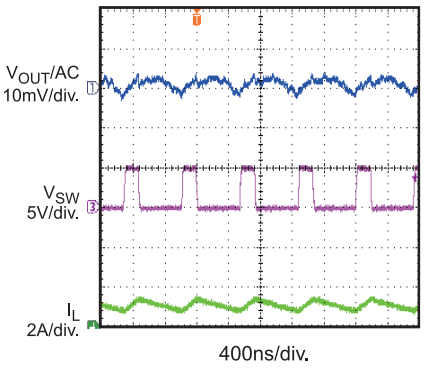
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

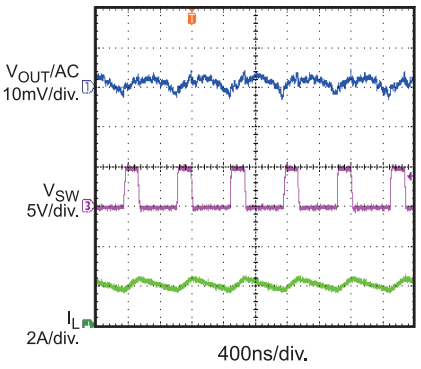
Output Ripple
I_{OUT}=0A



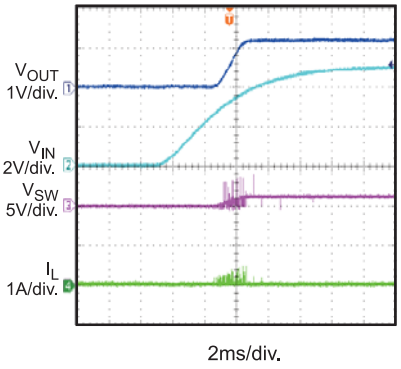
Output Ripple
I_{OUT}=1A



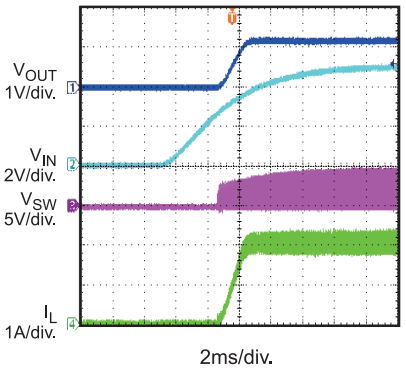
Output Ripple
I_{OUT}=2A



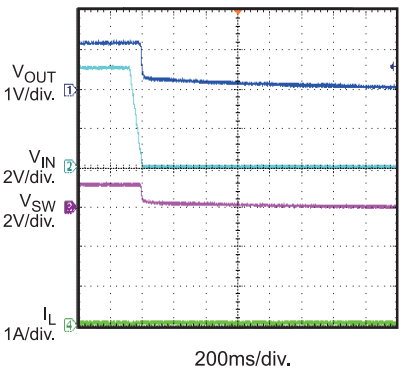
VIN Power-Up without Load



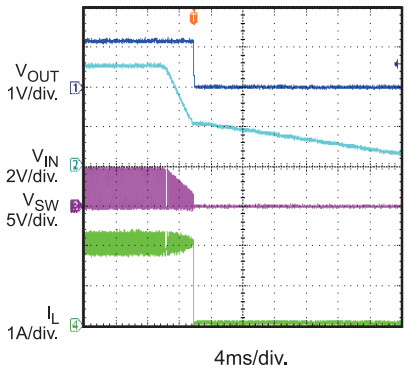
VIN Power-Up with 2A Load



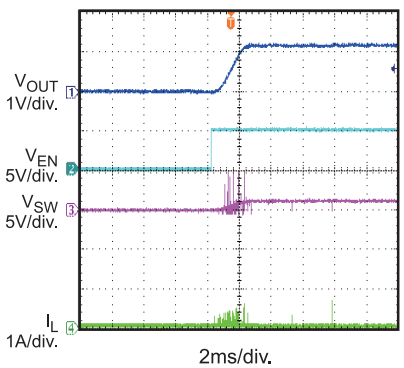
VIN Shutdown without Load



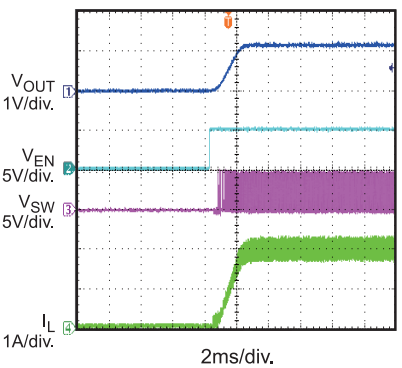
VIN Shutdown with 2A Load



EN Start-Up without Load



EN Start-Up with 2A Load



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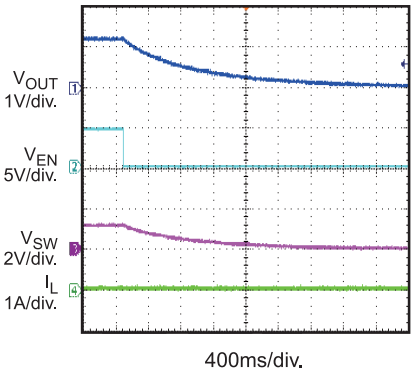
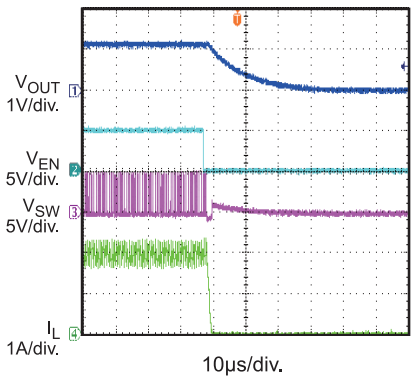
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted

EN Shutdown without Load



EN Shutdown with 2A Load



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PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** The output of PG is an open drain with an internal pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within ±10% of the regulation level. If FB voltage is out of that regulation range, it is low.
2	VIN	**Supply voltage.** The MP2161A operates from a +2.5V to +6V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
3	SW	**Switch output.**
4	PGND	**Power ground.**
5	OUT	**Input sense for output voltage.**
6	AGND	**Analogy ground for internal control circuit.**
7	FB	**Feedback.** An external resistor divider from the output to AGND (tapped to FB) sets the output voltage.
8	EN	**On/off control.**

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FUNCTIONAL BLOCK DIAGRAM

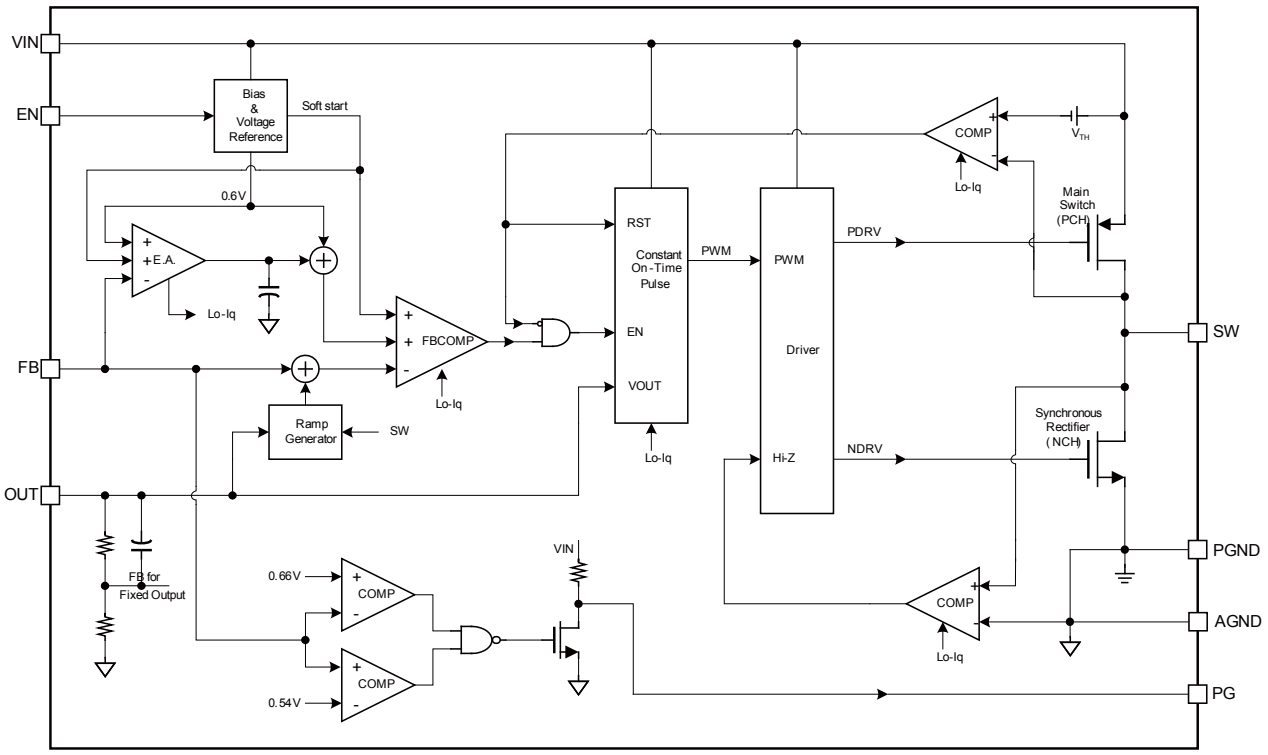

Figure 1: MP2161A Block Diagram

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OPERATION

The MP2161A uses constant-on-time (COT) control with input voltage feed forward to stabilize the switching frequency over the full input range. At light load, the MP2161A employs a proprietary control of the low-side switch and inductor current to eliminate ringing on the switching node and improve efficiency.

Constant-On-time (COT) Control

Compared to fixed frequency PWM control, constant-on-time (COT) control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed forward, the MP2161A maintains a nearly constant switching frequency across the input and output voltage range. The on time of the switching pulse is estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.667\mu s \quad (1)$$

To prevent inductor current runaway during load transient, the MP2161A fixes the minimum off time at 60ns. However, this minimum off time limit will not affect operation of the MP2161A in steady state.

Light-Load Operation

In a light-load condition, the MP2161A uses a proprietary control scheme to save power and improve efficiency. The MP2161A turns off the low-side switch when the inductor current starts to reverse. Then the MP2161A works in discontinuous conduction mode (DCM) operation.

There is a zero current cross circuit to detect if the inductor current starts to reverse. Considering the internal circuit propagation time, the typical delay is 50ns. This means that with this delay the inductor current will still fall after the ZCD is triggered. If the inductor current falling slew rate is fast (Vo voltage is high or close to Vin), the low-side MOSFET (LS-FET) is turned off, and the inductor current may be negative. This phenomenon prevents the MP2161A from entering DCM operation, even with no load. If DCM mode is required, the off time of the LS-FET in CCM should be longer than 100ns (2 times the propagation delay). For example, if Vin is 3.6V and Vo is 3.3V, the off time in CCM is 55ns. It is difficult to enter DCM at light load. Using a smaller inductor can improve this condition and make it easier to enter DCM.

Enable (EN)

When the input voltage is greater than the under-voltage lockout threshold (UVLO), typically 2.3V, the MP2161A is enabled by pulling EN higher than 1.2V. Floating or pulling EN down to ground disables the MP2161A. There is an internal 1MΩ resistor from EN to ground.

Soft Start (SS)

MP2161A has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at start-up. The soft-start time is about 1.15ms typically.

Power GOOD Indicator

MP2161A has an open drain with a 550kΩ pull-up resistor pin for a power good indicator (PG). When FB is within +/-10% of the regulation voltage (e.g., 0.6V), PG is pulled up to VIN by the internal resistor. If the FB voltage is out of the +/-10% window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum R_{dson} of less than 400Ω.

Current Limit

MP2161A has a typical 3.2A current limit for the high-side switch. When the high-side switch hits the current limit, the MP2161A reaches the hiccup threshold until the current decreases. This prevents the inductor current from continuing to build up, which results in damage to the components.

Short Circuit and Recovery

The MP2161A enters short-circuit protection mode when the current limit is reached. It tries to recover from the short circuit with hiccup mode. In short-circuit protection, the MP2161A disables the output power stage, discharges a soft-start capacitor, and then automatically tries to soft start again. If the short-circuit condition remains after the soft start ends, the MP2161A repeats this operation cycle until the short circuit disappears, and the output rises back to regulation level.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

An external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 cannot be too large or too small considering the trade-off between a dynamic circuit and stability in the circuit. Choose R1 around 120kΩ to 200kΩ. R2 is then given using Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 2.

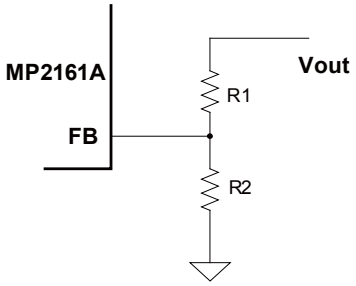

Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

A 0.68μH to 2.2μH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is calculated using Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For a higher output voltage, a 47μF capacitor may be needed for a more stable system.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5) and Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g., 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

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Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for proper IC function. A poor layout design can result in poor line or load regulation and stability issues. For best results, please refer to Figure 3 and follow the guidelines below:

1. Place the high current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the VIN and GND pins.
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short and away from the feedback network.

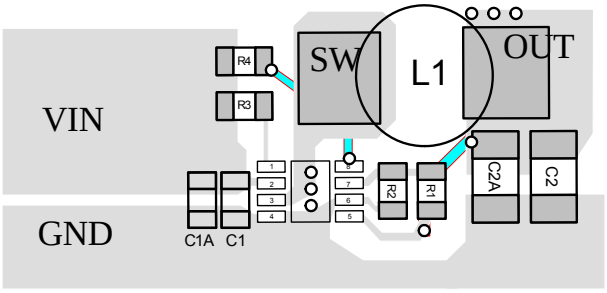

Figure 3: Recommended PCB Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	5V
V_{OUT}	1.2V
f_{SW}	1500kHz

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

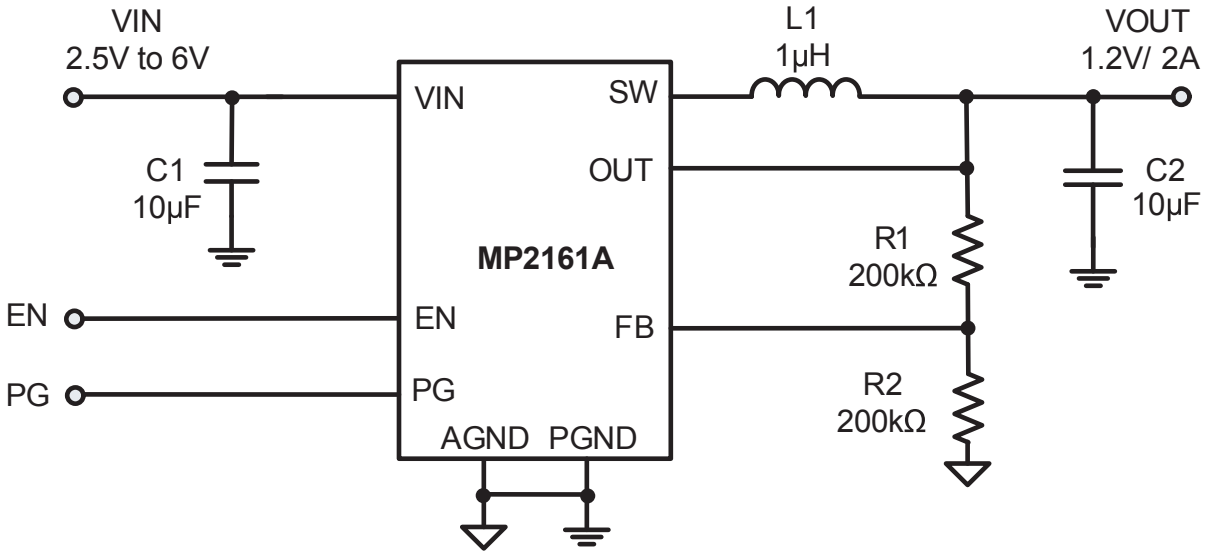

Figure 4: Typical Application Circuit

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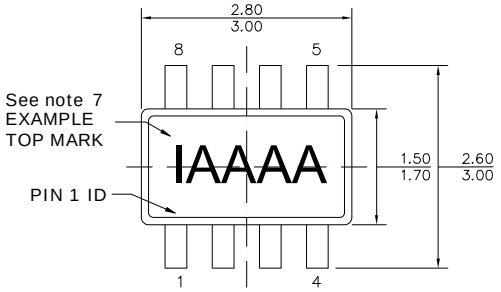
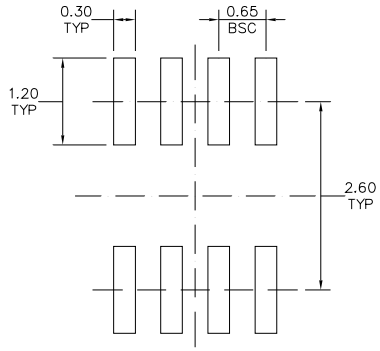
PACKAGE INFORMATION

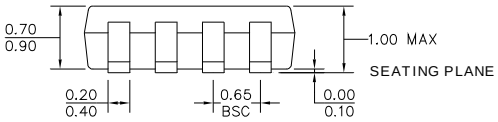
TSOT23-8



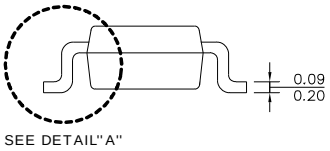
TOP VIEW



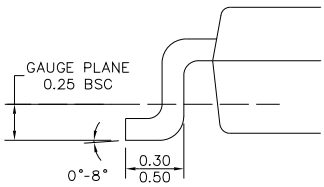
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) JEDEC REFERENCE IS MO-193, VARIATION BA
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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