

DESCRIPTION

The MP2122A is an internally compensated, 1MHz, fixed-frequency, dual, PWM, synchronous, step-down regulator with advanced light-load mode. The MP2122A operates from a 2.7V to 6V input, generates an output voltage as low as 0.608V, and has a 45µA quiescent current, making it ideal for powering portable equipment that run on a single-cell lithium-ion (Li+) battery.

The MP2122A integrates dual, 80mΩ, high-side switches and 35mΩ, synchronous rectifiers for high efficiency without an external Schottky diode. Peak-current mode control and internal compensation limits the minimum number of readily available external components.

Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MP2122A is available in an 8-pin TSOT23 package.

FEATURES

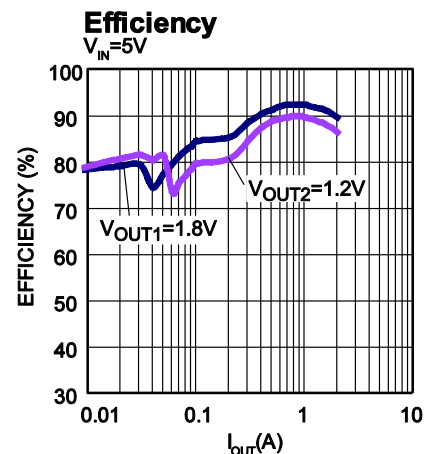
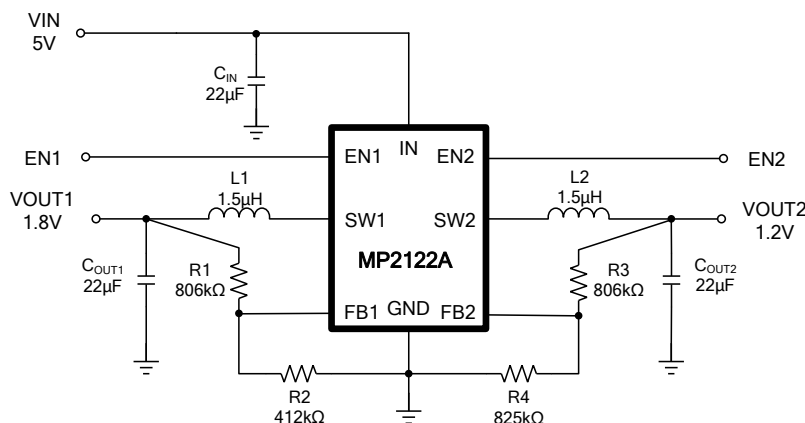
- Dual 2A Output Current
- >93% Peak Efficiency
- >80% Light-Load Efficiency
- Advanced Light-Load Mode
- Wide 2.7V to 6V Operating Input Range
- 80mΩ and 35mΩ Internal Power MOSFET
- 1MHz Fixed Switching Frequency
- Adjustable Output from 0.608V to VIN
- 180° Phase-Shifted Operation
- 100% Duty Cycle Operation
- 45µA Quiescent Current
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Thermal Shutdown
- Available in a TSOT23-8 Package

APPLICATIONS

- Small/Handheld Devices
- DVD Drivers
- Portable Instruments
- Smart Phones and Feature Phones
- Battery-Powered Devices

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TYPICAL APPLICATION



ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|--------------|----------|-------------|
| MP2122AGJ | TSOT23-8 | See Below |

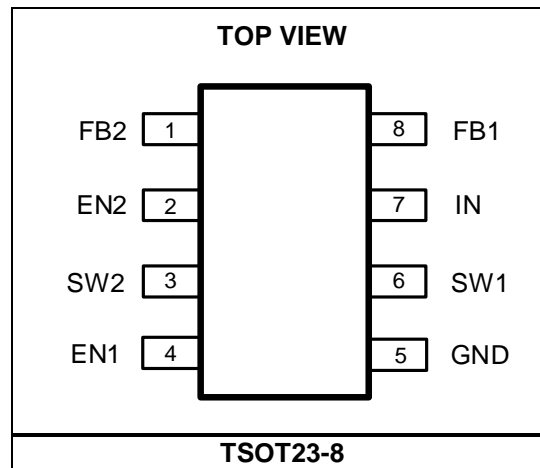
* For Tape & Reel, add suffix -Z (e.g. MP2122AGJ-Z)

TOP MARKING

| AKXY

AKX: Product code of MP2122AGJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN})6.5V
V_{sw}-0.3V (-3V for <10ns) to
6.5V (7.5V for <10ns)
All other pins -0.3V to +6.5V
Junction temperature 150°C
Lead temperature 260°C
Continuous power dissipation (T_A = +25°C) ⁽²⁾
..... 1.25W

Recommended Operating Conditions

Supply voltage (V_{IN}) 2.7V to 6V
Output voltage (V_{OUT}) 0.608V to 5.5V
Operating junction temp..... -40°C to +125°C

Thermal Resistance ⁽³⁾ **θ_{JA}** **θ_{JC}**
TSOT23-8 100..... 55 ... °C/W

NOTES:

- 1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (4)
V_{IN} = V_{EN} = 3.6V, T_A = +25°C, unless otherwise noted.

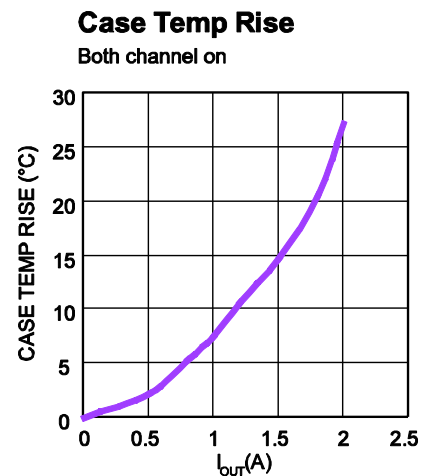
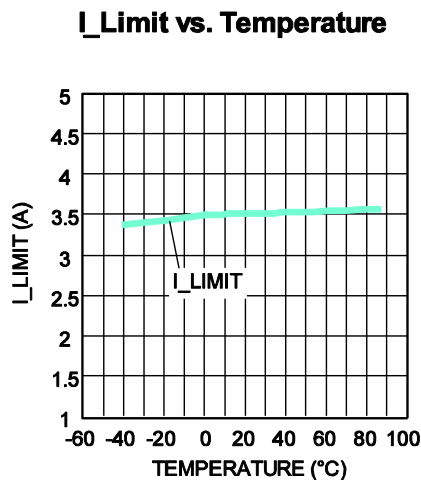
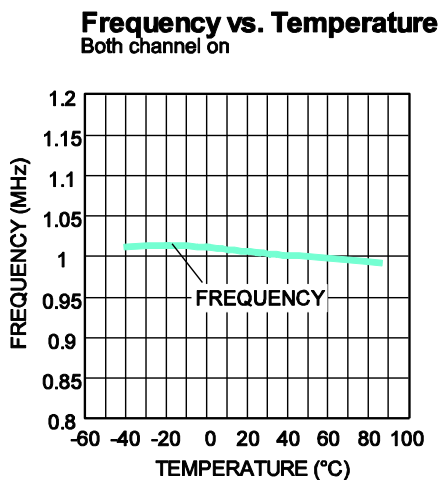
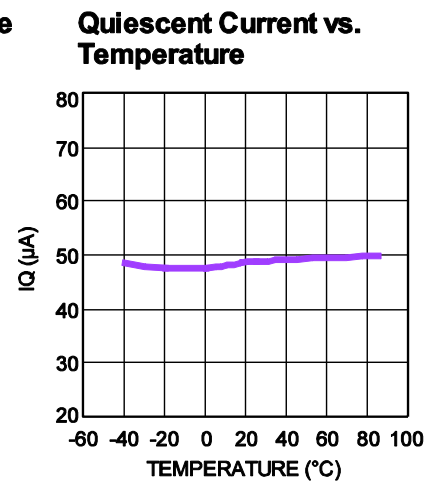
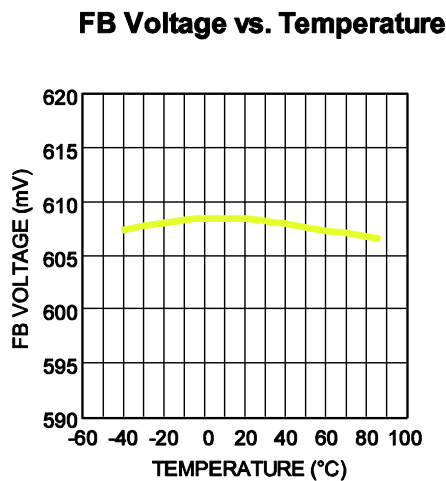
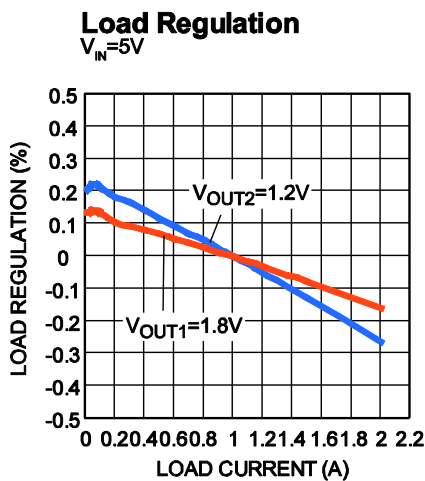
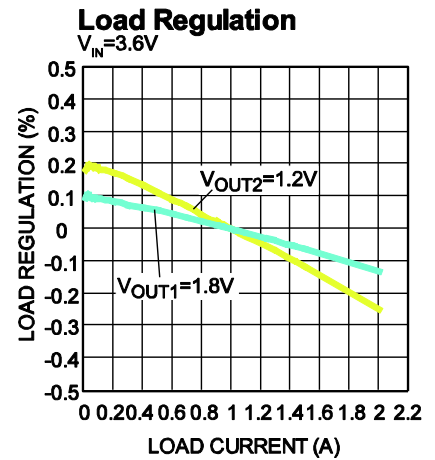
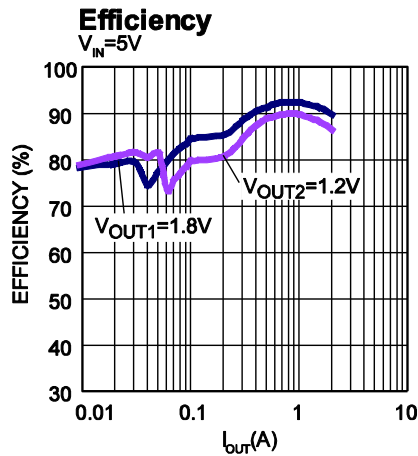
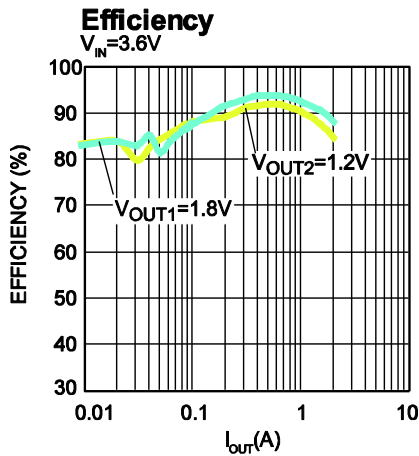
| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|-----------------------|--|-------|-------|-------|--------|
| Supply current (quiescent) | I _Q | V _{IN} = 3.6V, V _{EN} = 2V, V _{FB} = 0.65V | 35 | 45 | 55 | μA |
| Shutdown current | | V _{EN} = 0V | | 0 | 1 | μA |
| IN under-voltage lockout threshold | | Rising edge | 2.4 | 2.5 | 2.6 | V |
| IN under-voltage lockout hysteresis | | | | 300 | | mV |
| Regulated FB voltage | V _{FB} | T _A = +25°C | 0.596 | 0.608 | 0.620 | V |
| FB input current | | V _{FB} = 0.608V | | ±10 | 50 | nA |
| EN high threshold | | -40°C ≤ T _A ≤ +85°C | 1.2 | | | V |
| EN low threshold | | -40°C ≤ T _A ≤ +85°C | | | 0.4 | V |
| Internal soft-start time | τ _{SS} | | | 0.5 | | ms |
| High-side switch on resistance | R _{DS(on)_P} | V _{IN} = 5V | | 80 | | mΩ |
| Low-side switch on resistance | R _{DS(on)_N} | V _{IN} = 5V | | 35 | | mΩ |
| SW leakage current | | V _{EN} = 0V, V _{IN} = 6V, V _{SW} = 0V and 6V | -1 | 0 | 1 | μA |
| High-side switch current limit | | Sourcing, D = 40% | 2.8 | 3.5 | 4.5 | A |
| Oscillator frequency | | Both channels work in CCM | 0.8 | 1 | 1.2 | MHz |
| Phase shift | | | | 180 | | degree |
| Minimum on time ⁽⁵⁾ | τ _{ON_MIN} | | | 90 | | ns |
| Minimum off time | τ _{OFF_MIN} | | | 100 | | ns |
| Maximum duty cycle | | | | 100 | | % |
| Thermal shutdown threshold ⁽⁵⁾ | | Hysteresis = 30°C | | 160 | | °C |

NOTES:

- 4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
 5) Guaranteed by design.

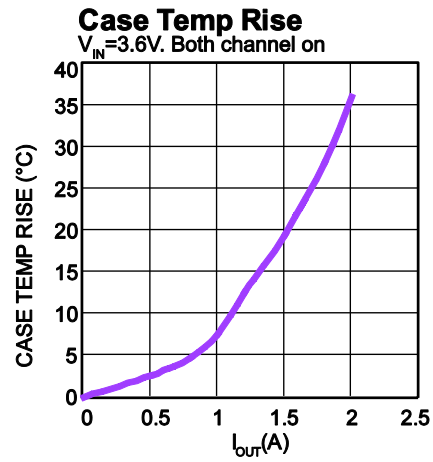
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5μH, C_{OUT1} = C_{OUT2} = 22μF, T_A = 25°C, unless otherwise noted.

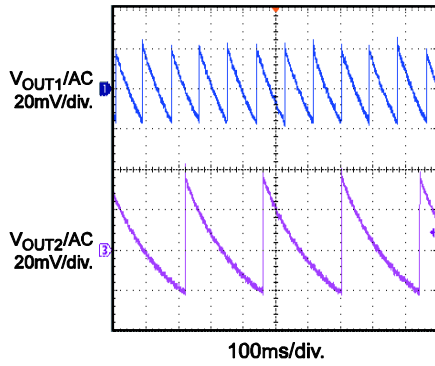
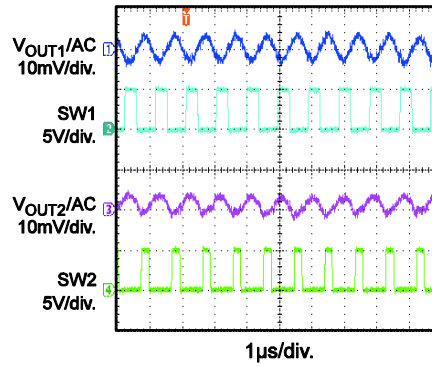
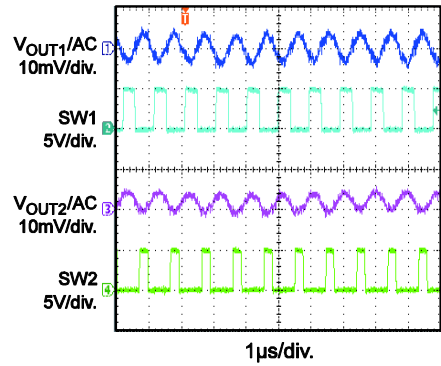
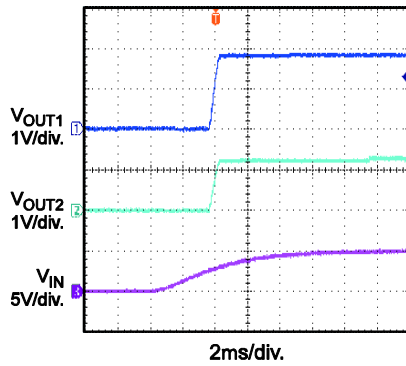
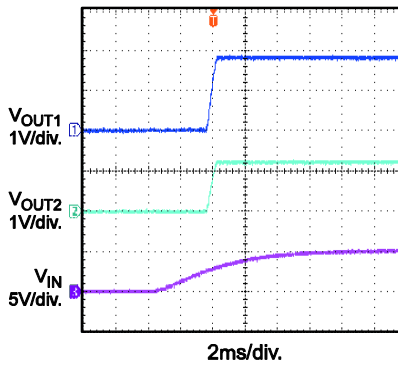
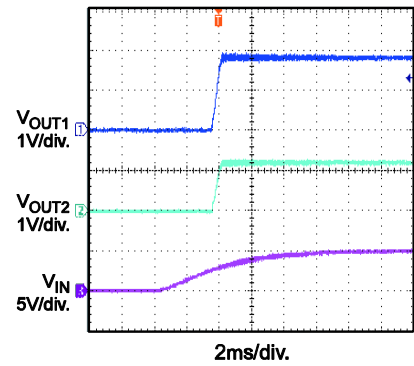
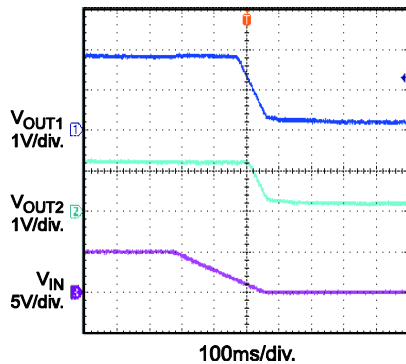
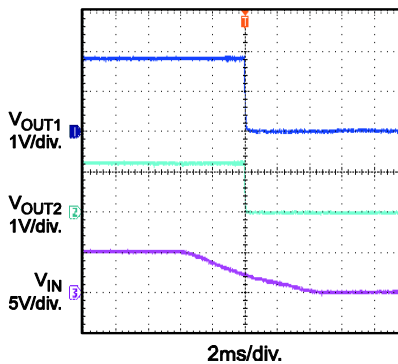
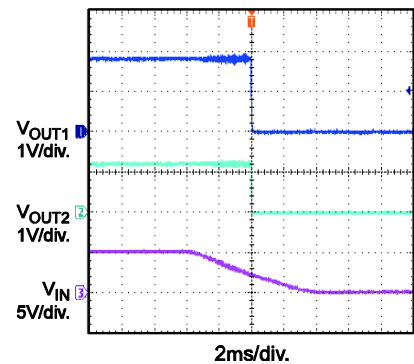


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 1.2V$, $L = 1.5\mu H$, $C_{OUT1} = C_{OUT2} = 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.



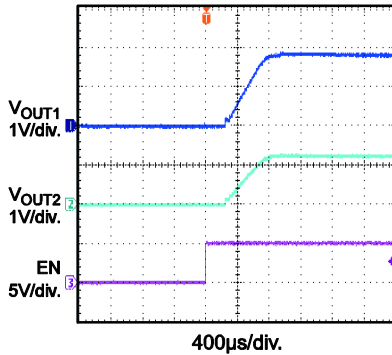
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*
 $V_{IN} = 5V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 1.2V$, $L = 1.5\mu H$, $C_{OUT1} = C_{OUT2} = 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

Output Ripple
 $I_{OUT1} = I_{OUT2} = 0A$

Output Ripple
 $I_{OUT1} = I_{OUT2} = 1A$

Output Ripple
 $I_{OUT1} = I_{OUT2} = 2A$

 V_{IN} Power-Up without Load
 $I_{OUT1} = I_{OUT2} = 0A$

 V_{IN} Power-Up Half Load
 $I_{OUT1} = I_{OUT2} = 1A$

 V_{IN} Power-Up Full Load
 $I_{OUT1} = I_{OUT2} = 2A$

 V_{IN} Power-Down without Load
 $I_{OUT1} = I_{OUT2} = 0A$

 V_{IN} Power-Down Half Load
 $I_{OUT1} = I_{OUT2} = 1A$

 V_{IN} Power-Down Full Load
 $I_{OUT1} = I_{OUT2} = 2A$


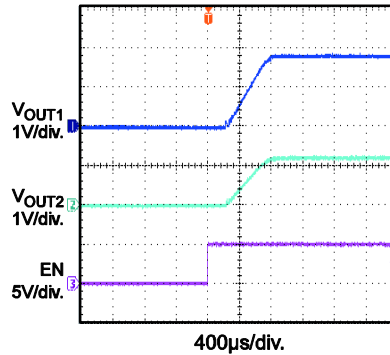
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5μH, C_{OUT1} = C_{OUT2} = 22μF, T_A = 25°C, unless otherwise noted.

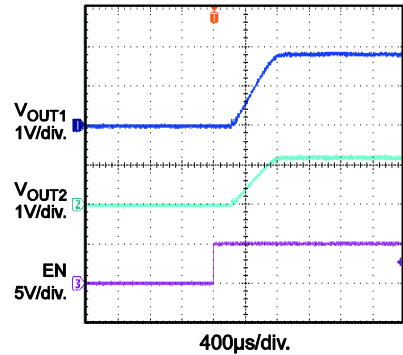
EN On without Load
I_{OUT1} = I_{OUT2} = 0A



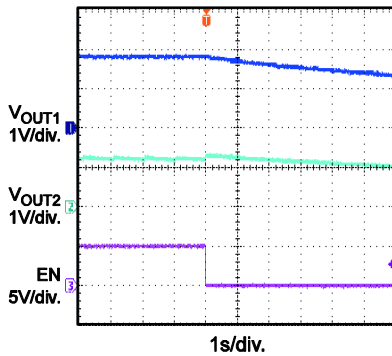
EN On with Half Load
I_{OUT1} = I_{OUT2} = 1A



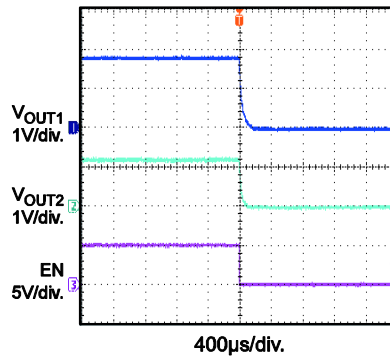
EN On with Full Load
I_{OUT1} = I_{OUT2} = 2A



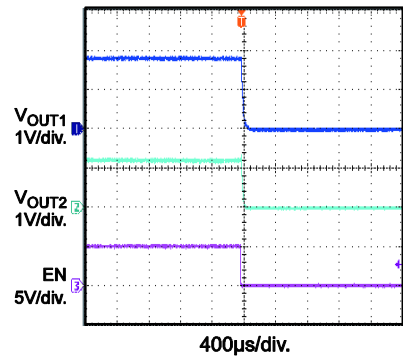
EN Down without Load
I_{OUT1} = I_{OUT2} = 0A



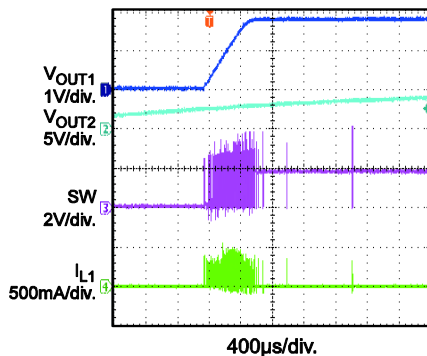
EN Down with Half Load
I_{OUT1} = I_{OUT2} = 1A



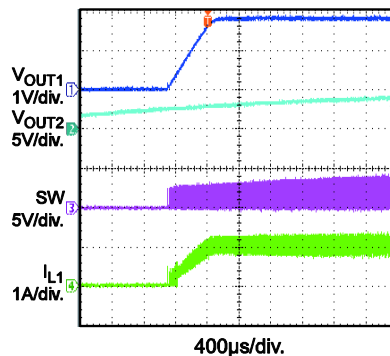
EN Down with Full Load
I_{OUT1} = I_{OUT2} = 2A



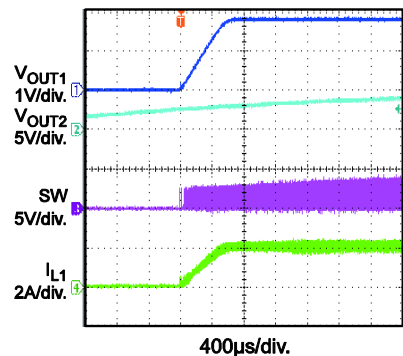
V_{IN} Power-On without Load
I_{OUT1} = I_{OUT2} = 0A



V_{IN} Power-On
I_{OUT1} = 1A, I_{OUT2} = 0A

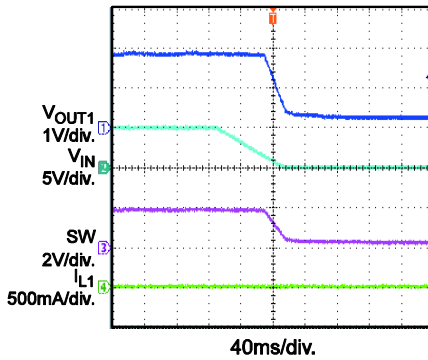
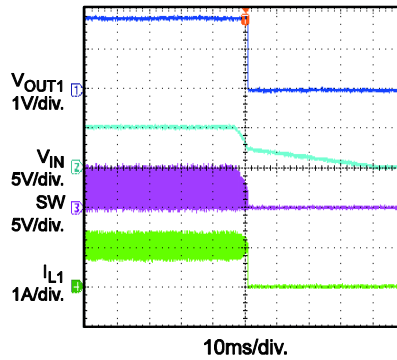
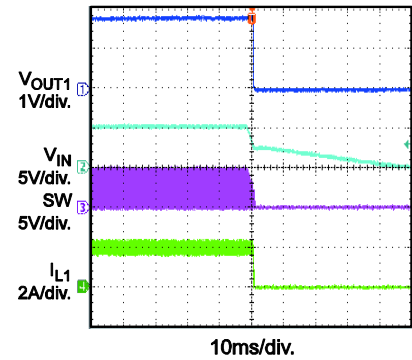
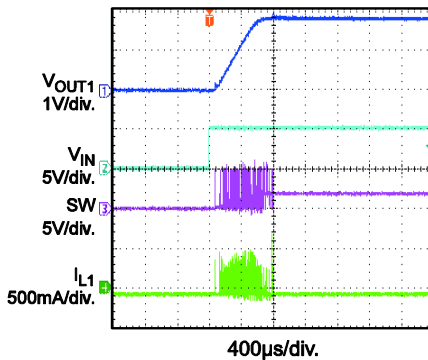
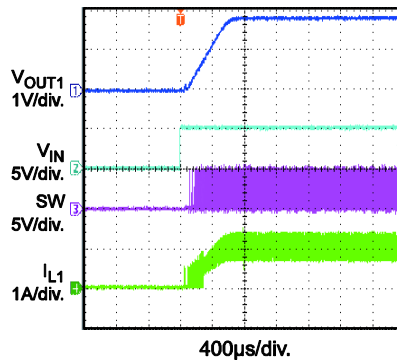
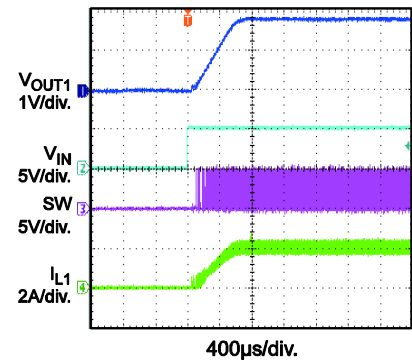
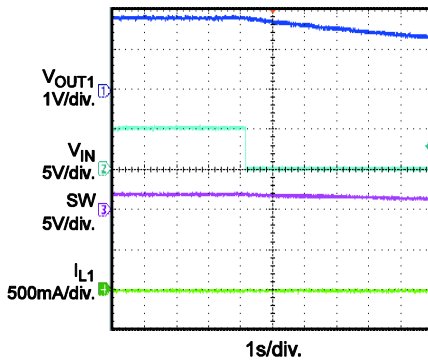
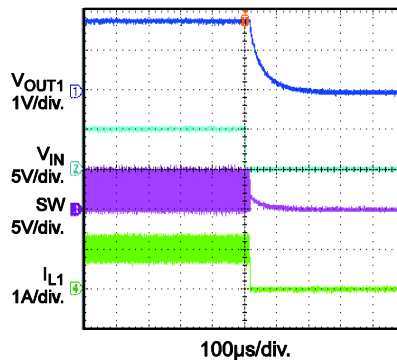
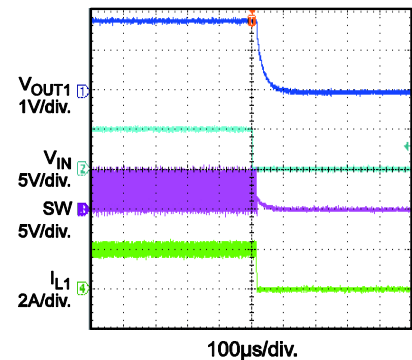


V_{IN} Power-On
I_{OUT1} = 2A, I_{OUT2} = 0A



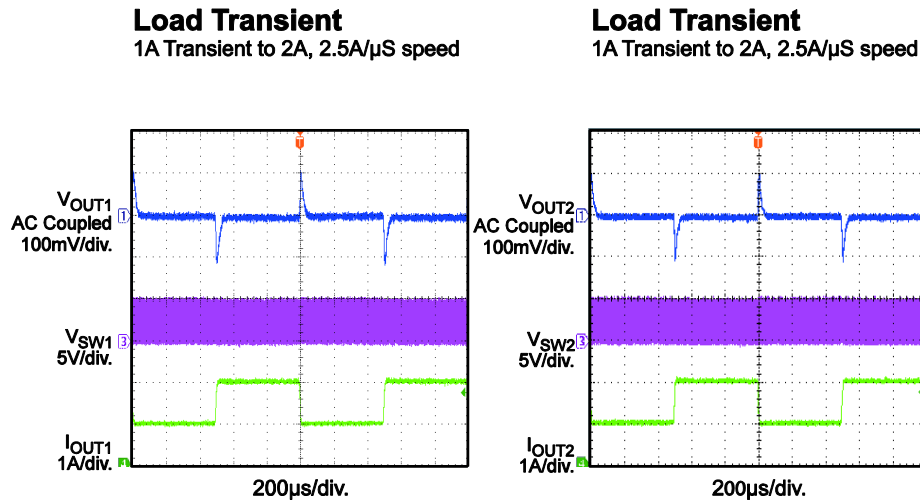
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5μH, C_{OUT1} = C_{OUT2} = 22μF, T_A = 25°C, unless otherwise noted.

V_{IN} Power-Down
 I_{OUT1} = I_{OUT2} = 0A

V_{IN} Power-Down
 I_{OUT1} = 1A, I_{OUT2} = 0A

V_{IN} Power-Down
 I_{OUT1} = 2A, I_{OUT2} = 0A

Enable On
 I_{OUT1} = I_{OUT2} = 0A

Enable On
 I_{OUT1} = 1A, I_{OUT2} = 0A

Enable On
 I_{OUT1} = 2A, I_{OUT2} = 0A

Enable Down
 I_{OUT1} = I_{OUT2} = 0A

Enable Down
 I_{OUT1} = 1A, I_{OUT2} = 0A

Enable Down
 I_{OUT1} = 2A, I_{OUT2} = 0A


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5μH, C_{OUT1} = C_{OUT2} = 22μF, T_A = 25°C, unless otherwise noted.



PIN FUNCTIONS

| Package Pin # | Name | Description |
|---------------|------|---|
| 1 | FB2 | Feedback 2. FB2 is an error amplifier input. Connect FB2 to the tap of an external resistor divider between the output and GND. FB2 sets the regulation voltage. |
| 2 | EN2 | Channel 2 enable. Enable for buck 2. |
| 3 | SW2 | Switch node. SW2 connects to the channel 2 internal high-side and low-side power MOSFETs. SW2 connects to the inductor. |
| 4 | EN1 | Channel 1 enable. Enable for buck 1. |
| 5 | GND | Ground. |
| 6 | SW1 | Switch node. SW1 connects to the channel 1 internal high-side and low-side power MOSFETs. SW1 connects to the inductor. |
| 7 | IN | Input supply. IN requires a decoupling capacitor to ground to reduce switching spikes. |
| 8 | FB1 | Feedback 1. FB1 is an error amplifier input. Connect FB1 to the tap of an external resistor divider between the output and GND. FB1 sets the regulation voltage. |

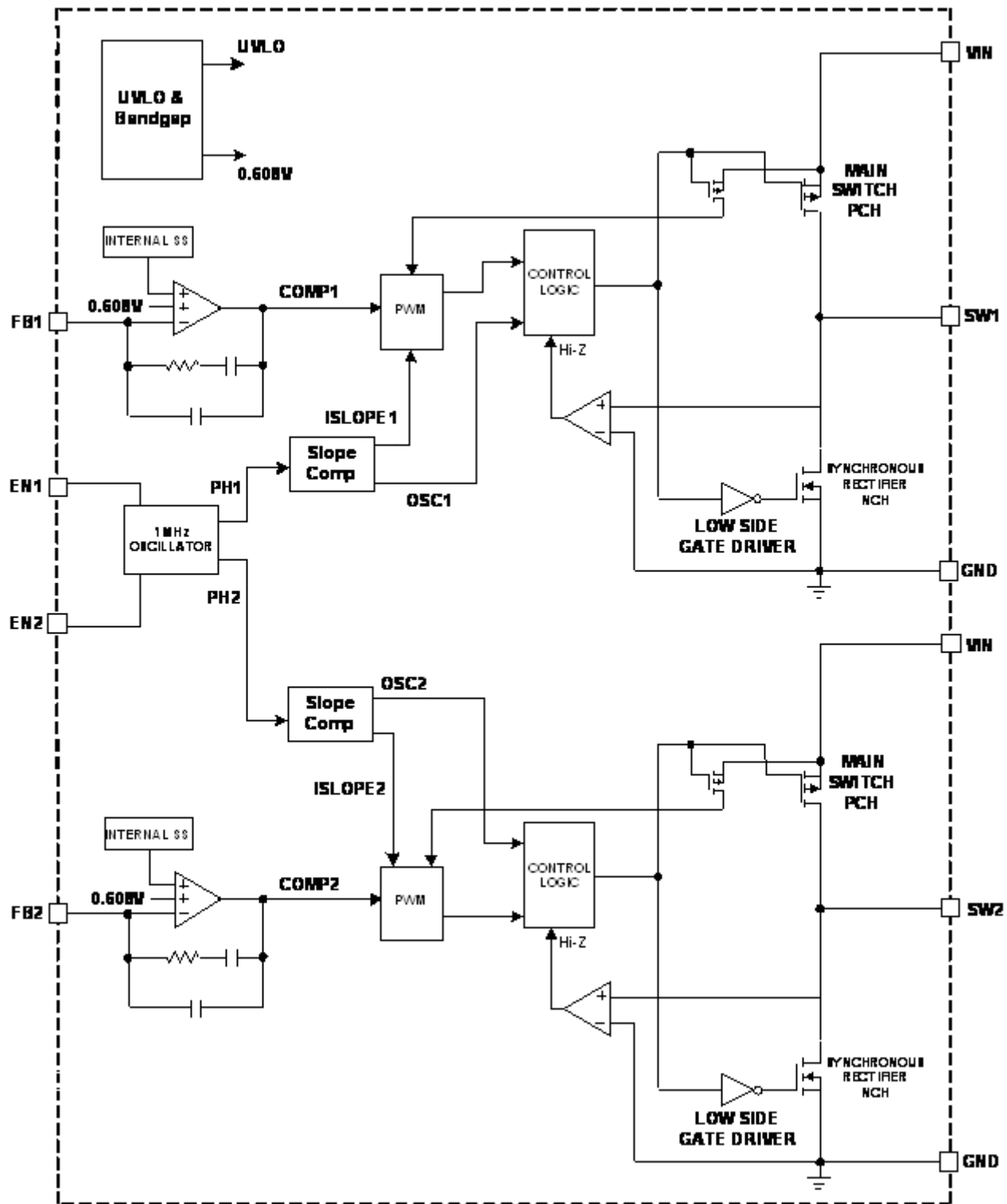
BLOCK DIAGRAM


Figure 1: Functional Block Diagram

OPERATION

The MP2122A is a fully integrated, dual-channel, synchronous, step-down converter. Both channels have peak-current modes with internal compensation for faster transient responses and cycle-by-cycle current limits.

The MP2122A is optimized for low-voltage, portable applications where efficiency and small size are critical.

180° Phase Shift

By default, the MP2122A's two channels operate at a 180° phase shift to reduce input current ripple. The smaller current ripple allows for a smaller input bypass capacitor. In continuous conduction mode (CCM), two internal clocks control the switching. The high-side MOSFET (HS-FET) turns on at the corresponding CLK's rising edge.

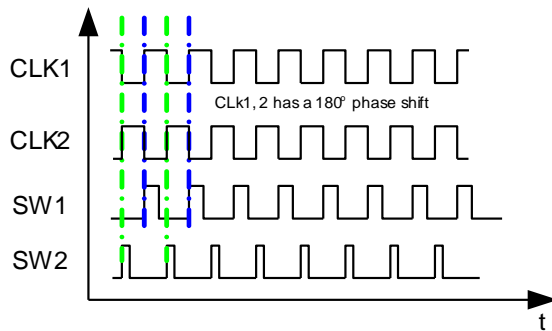


Figure 2: Clock/Switching Timing

The switching frequency for each channel falls when operating at a low dropout, so the MP2122A operates at a default switching frequency of 1MHz with a fixed off time. After the input voltage recovers, switching for pulse-width modulation (PWM) mode resumes normally and synchronizes with the master oscillator for phase-shifted operation.

Advanced Light-Load Mode

The MP2122A has an advanced light-load mode, which can help the MP2122A achieve better light-load performance. In light loads, the MP2122A uses a proprietary control scheme to save power and improve efficiency. The MP2122A turns off the low-side switch when the inductor current starts to reverse. Then the MP2122A works in discontinuous conduction mode (DCM) operation.

When either channel enters DCM or low-dropout operation, that channel is not controlled by the internal 1MHz oscillator (see Table 1).

Table 1: Light-Load Modes

| | Condition | | Mode | |
|---|-------------|-------------|----------------|--------------------|
| | CH1 | CH2 | CH1 | CH2 |
| 1 | Heavy load | | 1MHz CCM | 1MHz CCM, 0° phase |
| 2 | Light load | | DCM | DCM |
| 3 | Low dropout | | Fixed off time | Fixed off time |
| 4 | Heavy load | Light load | 0.95MHz CCM | DCM |
| 5 | Light load | Heavy load | DCM | 0.95MHz CCM |
| 6 | Heavy load | Low dropout | 0.95MHz CCM | Fixed off time |
| 7 | Low dropout | Heavy load | Fixed off time | 0.95MHz CCM |
| 8 | Light load | Low dropout | DCM | Fixed off time |
| 9 | Low dropout | Light load | Fixed off time | DCM |

Soft Start

The MP2122A has a built-in soft start that ramps up the output voltage at a controlled slew rate to minimize overshoot at start-up. The soft-start time is ~0.5ms.

Current Limit and Short-Circuit Recovery

Each channel's high-side switch has a typical 3.5A current limit. The MP2122A treats any current-limit condition that remains for 400µs as a short and enters hiccup mode.

The MP2122A disables its output power stage in hiccup mode and slowly discharges the soft-start capacitor before initiating soft start. If the short-circuit condition still remains, the MP2122A repeats this operation until the short circuit is removed and the output returns to the regulation level.

APPLICATION INFORMATION

Output Voltage

External resistor dividers connected to FB1/2 set the output voltages. The feedback resistor connected to FB1 (R1) also sets the feedback loop bandwidth (f_c). f_c does not exceed 0.1 times f_{SW} . When using a ceramic output capacitor (C_O), set the range to 50kHz and 100kHz for optimal transient performance and phase margin. When using an electrolytic capacitor, set the loop bandwidth no higher than 1/4 the ESR zero frequency (f_{ESR}). f_{ESR} can be calculated with Equation (1):

$$f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_O} \quad (1)$$

It is recommended to use a 600k Ω to 800k Ω resistor for R1 when $C_O = 22\mu\text{F}$. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.608V} - 1} \quad (2)$$

Table 2 lists recommended resistor values for different output voltages.

Table 2: Resistor Values vs. Output Voltage

| V _{OUT} (V) | R1 (Ω) | R2 (Ω) | L (μH) | C _{OUT} (μF) (Ceramic) |
|----------------------|-----------------|-----------------|---------------------|--|
| 1.2 | 806k | 825k | 0.47 - 2.2 | 22 |
| 1.5 | 806k | 549k | 0.47 - 2.2 | 22 |
| 1.8 | 806k | 412k | 0.47 - 2.2 | 22 |
| 2.5 | 806k | 261k | 1 - 4.7 | 22 |
| 3.3 | 806k | 182k | 1 - 4.7 | 22 |

Inductor Selection

For most applications, use a 1.5 μH to 2.2 μH inductor with a DC current rating at least 1.25 times the maximum load current. For the best efficiency, select an inductor with a DC resistance <20m Ω (see Table 3). For most designs, the inductance value can be estimated with Equation (3):

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current. Select the inductor ripple current to be approximately 30% of the maximum load current (2A).

The maximum inductor peak current is determined with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Table 3: Suggested Surface-Mount Inductors

| Vendor | Part Number | L (μH) | DCR (m Ω) | SC (A) | LxWxH (mm ³) |
|--------|--------------------|---------------------|-------------------|--------|--------------------------|
| Wurth | 744777002 | 2.2 | 13 | 6 | 7.3x7.3x4.5 |
| | 744310200 | 2 | 14.2 | 6.5 | 7x6.9x3 |
| TDK | RLF7030T-1R5N6R1-T | 1.5 | 8 | 6.5 | 7.8x6.8x3.2 |

Input Capacitor

The input capacitor reduces surge current drawn from the input and switching noise from the device. Select an input capacitor with a switching frequency impedance less than the input source impedance to prevent high-frequency switching current from passing to the input source. Use low ESR ceramic capacitors with X5R or X7R dielectrics with small temperature coefficients. For most applications, a 22 μF capacitor is sufficient.

Output Capacitor

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. Using an electrolytic capacitor may result in additional output voltage ripple, thermal issues, and requires additional care in selecting the feedback resistor (R1) due to the large ESR. The output ripple (ΔV_{OUT}) can be approximated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_O} \right) \quad (5)$$

Power Dissipation

IC power dissipation is important to the circuit design because of efficiency concerns and the chip's thermal requirements. Several parameters influence power dissipation, such as conduction loss (Cond), dead time (DT), switching loss (SW), MOSFET driver current (DR), and supply current (S).

Based on these parameters, the power loss can be estimated with Equation (6):

$$P_{LOSS} = P_{Cond} + P_{DT} + P_{SW} + P_{DR} + P_S \quad (6)$$

Thermal Regulation

Changes in IC temperature change electrical characteristics, especially when the temperature exceeds the IC's recommended operating range. Managing the IC's temperature requires additional considerations to ensure that the IC runs below the maximum allowable temperature. While operating the IC within the recommended electrical limits is a major component to maintaining proper thermal regulation, specific layout designs can also improve the thermal profile while limiting costs to either efficiency or the operating range.

For the MP2122A, connect the GND on the package to a GND plane on top of the PCB to use this plane as a heat sink. Connect this GND plane to the GND planes beneath the IC using vias to further improve heat dissipation. Given that these GND planes can introduce unwanted EMI noise and occupy valuable PCB space, design the size and shape of these planes to match the thermal resistance requirement using Equation (7):

$$\theta_{SA} = \theta_{JA} - \theta_{JC} \quad (7)$$

Connecting GND to a heat sink cannot guarantee that the IC will not exceed its recommended temperature limits. If the ambient air temperature approaches the IC's temperature limit, the IC can be de-rated so it operates using less power. This helps prevent thermal damage and unwanted electrical characteristics.

PCB Layout Guidelines

Proper layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to IN and GND.
3. Place the external feedback resistors next to FB.
4. Keep the switching node SW short and away from the feedback network.

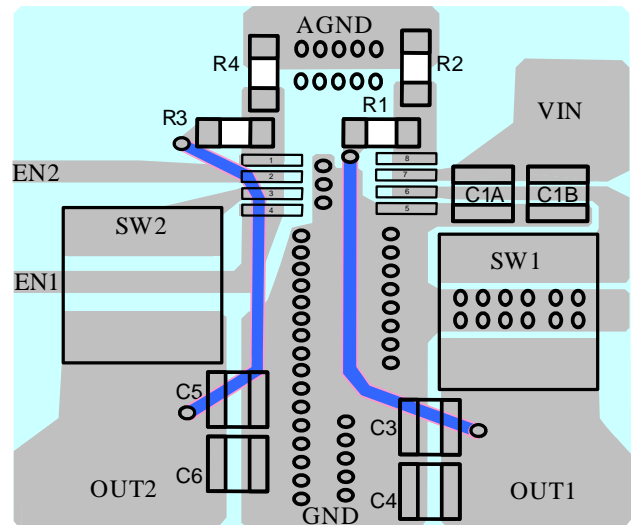


Figure 3: Recommended PCB Layout

Design Example

Table 4 is a design example following the application guidelines for the specifications below.

Table 4: Design Example

| | |
|--------------|------|
| VIN | 5V |
| VOUT1 | 1.8V |
| VOUT2 | 1.2V |

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUIT

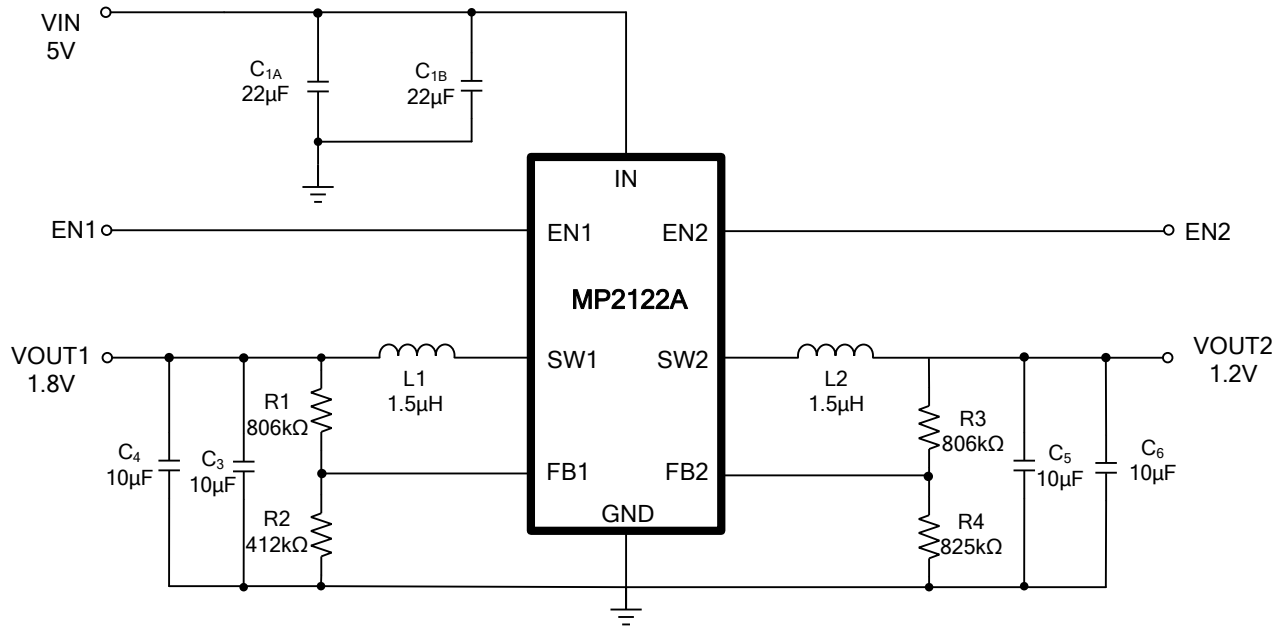
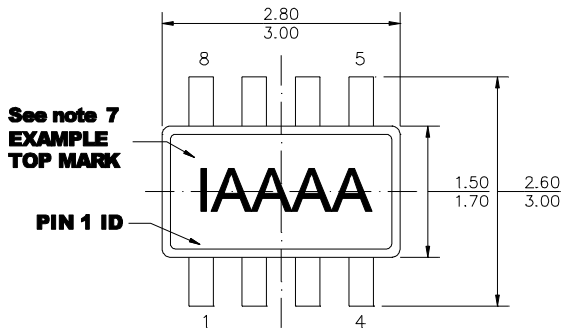


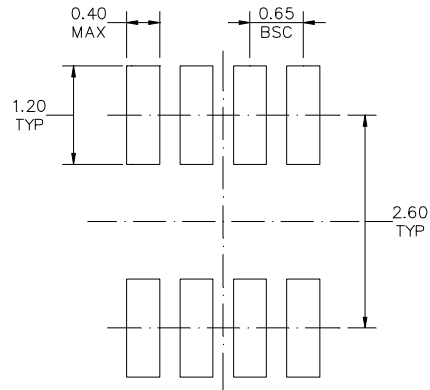
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

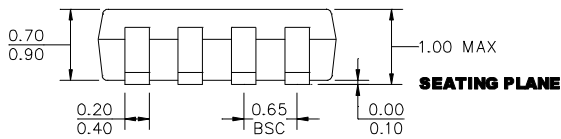
TSOT23-8



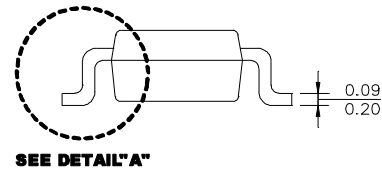
TOP VIEW



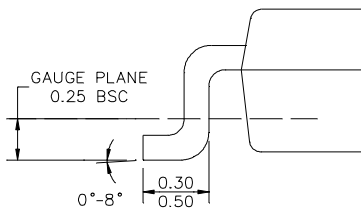
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO193, VARIATION BA
- 6) DRAWING IS NOT TO SCALE
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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