HGTG20N60C3R, HGTP20N60C3R, HGT1S20N60C3R, HGT1S20N60C3RS

HARRIS SEMICONDUCTOR

January 1997

40A, 600V, Rugged UFS Series N-Channel IGBTs

Features

- **40A, 600V T_J = 25°C**
- **600V Switching SOA Capability**
- **Typical Fall Time at T_J = 150°C 330ns**
- **Short Circuit Rating at T_J = 150°C............. 10µs**
- **Low Conduction Loss**

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP20N60C3R	TO-220AB	20N60C3R
HGTG20N60C3R	TO-247	20N60C3R
HGT1S20N60C3R	TO-262AA	20N60C3R
HGT1S20N60C3RS	TO-263AB	20N60C3R

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., HGT1S20N60C3RS9A.

Description

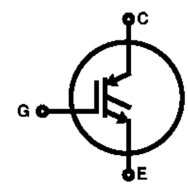
This family of IGBTs was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. These devices demonstrate RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the Turn-On ratings include the effect of the diode in the test circuit (Figure 16). The data was obtained with the diode at the same T_J as the IGBT under test.

Formerly Developmental Type TA49047.

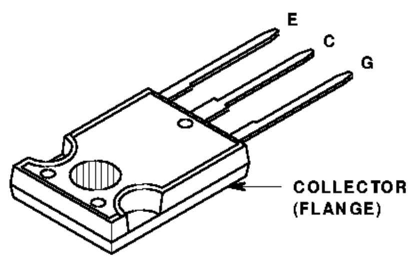
Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

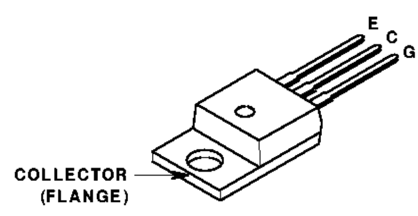


Packaging

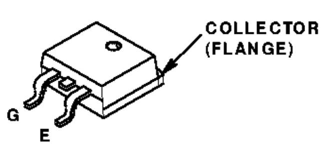
JEDEC STYLE TO-247



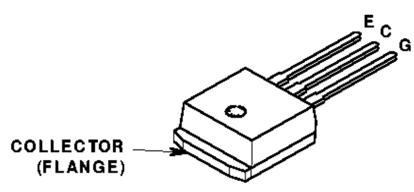
JEDEC TO-220AB (ALTERNATE VERSION)



JEDEC TO-263AB



JEDEC TO-262AA



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		ALL TYPES	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	40	A
At $T_C = 110^oC$	I_{C110}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	80	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Fig. 12	SSOA	80A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	164	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/^{o}C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	10	µs

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 440V$, $T_J = 150^oC$, $R_{GE} = 10\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.2	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.5	6.3	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA (See Figure 12)	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$	$V_{CE(PK)} = 600V$, L = 1mH	80	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	9.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$	$V_{GE} = 15V$	-	87	110	nC
			$V_{GE} = 20V$	-	116	150	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 10\Omega$, L = 1mH; Diode used in test circuit RURP1560 at 150^oC		-	34	-	ns
Current Rise Time	t_{RI}			-	40	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	390	500	ns
Current Fall Time	t_{FI}			-	330	400	ns
Turn-Off Voltage dv/dt (Note 3)	dV_{CE}/dt			-	1.3	-	V/ns
Turn-On Voltage dv/dt (Note 3)	dV_{CE}/dt			-	7.0	-	V/ns
Turn-On Energy (Note 4)	E_{ON}			-	2.3	-	mJ
Turn-Off Energy (Note 5)	E_{OFF}			-	3.0	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	-	0.76	^{o}C/W

NOTES:

3. dV_{CE}/dt depends on the diode used and the temperature of the diode.
4. Turn-On Energy Loss (E_{ON}) includes diode losses and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals $V_{CE(ON)}$. This value of E_{ON} was obtained with a RURP1560 diode at $T_J = 150^oC$. A different diode or temperature will result in a different E_{ON}. For example with diode at $T_J = 25^oC$ E_{ON} is about one half the value at 150^oC.
5. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

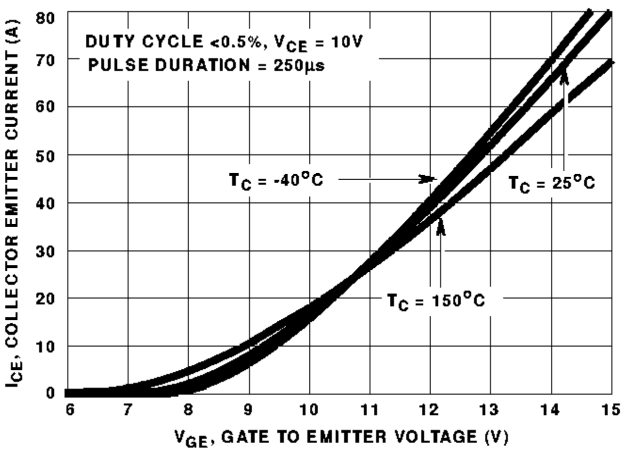


FIGURE 1. TRANSFER CHARACTERISTICS

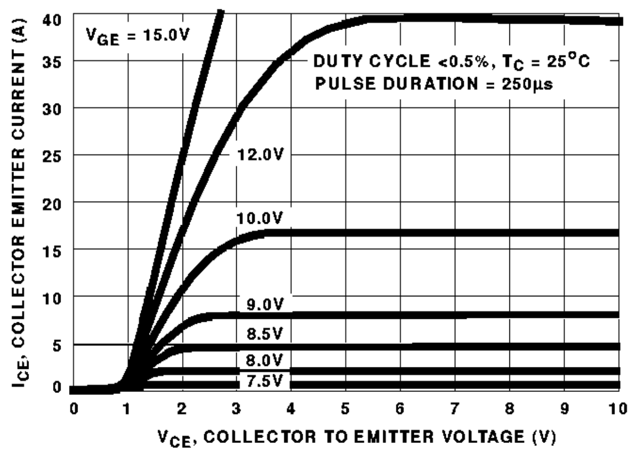


FIGURE 2. SATURATION CHARACTERISTICS

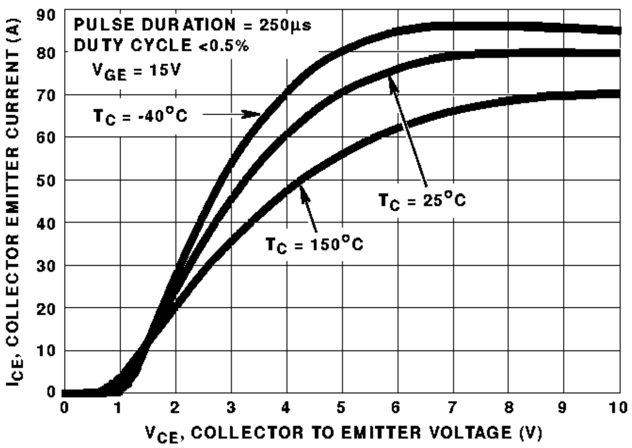


FIGURE 3. COLLECTOR EMITTER ON STATE VOLTAGE

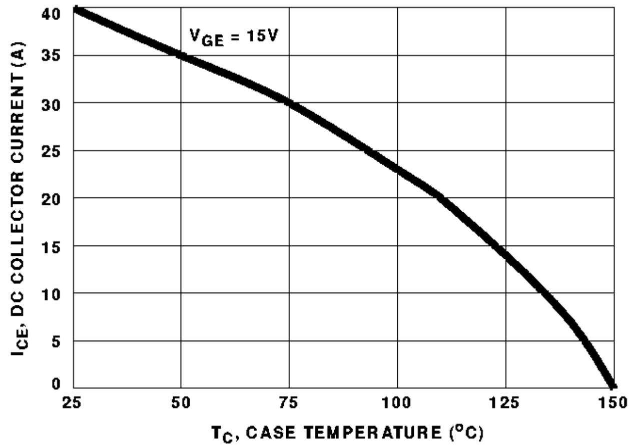


FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

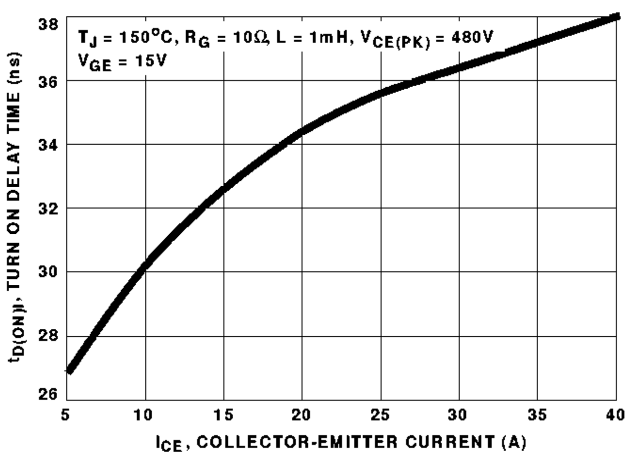


FIGURE 5. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

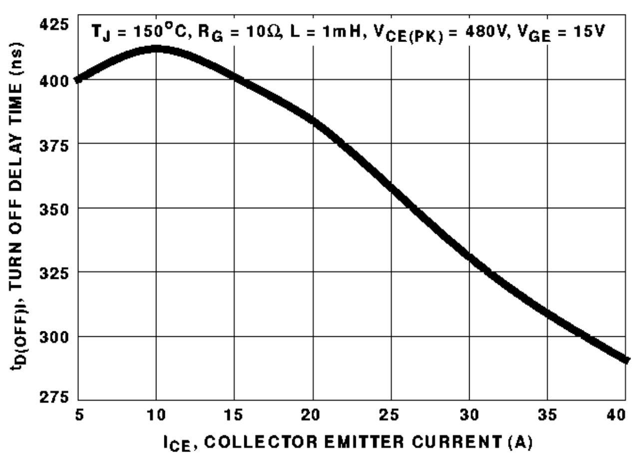


FIGURE 6. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

Typical Performance Curves (Continued)

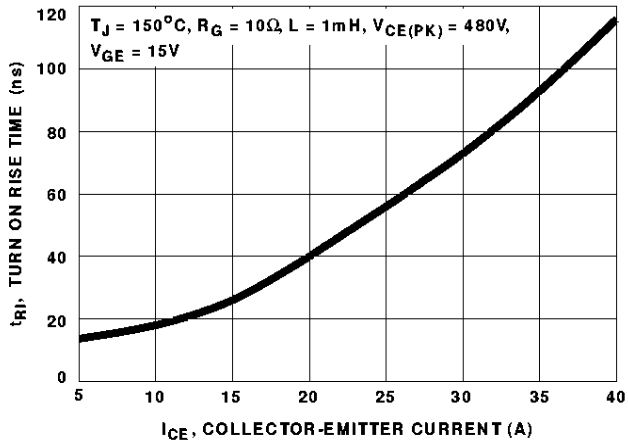


FIGURE 7. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

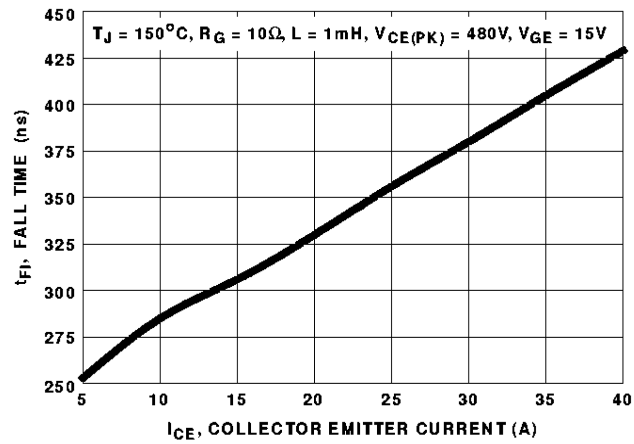


FIGURE 8. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

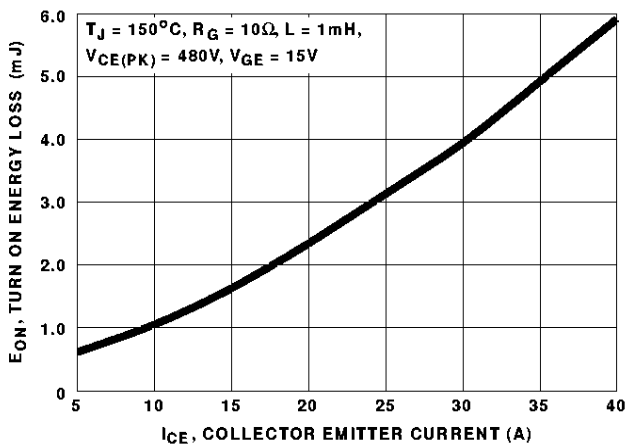


FIGURE 9. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

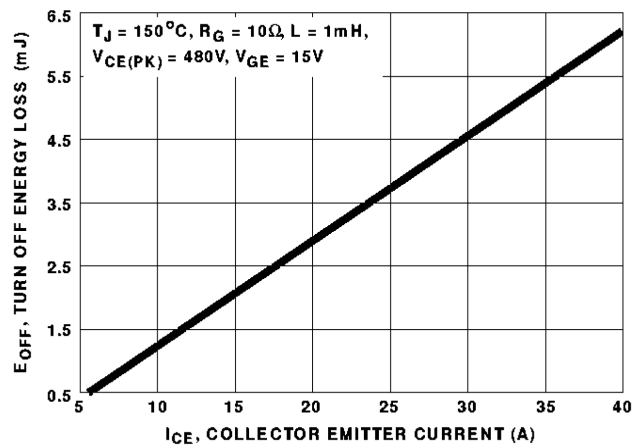


FIGURE 10. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

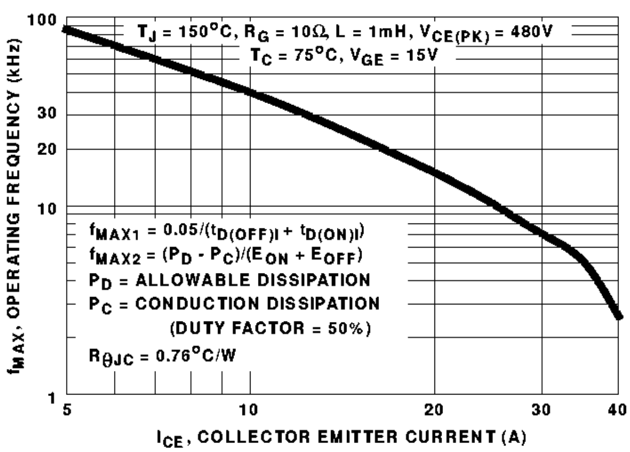


FIGURE 11. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR EMITTER CURRENT

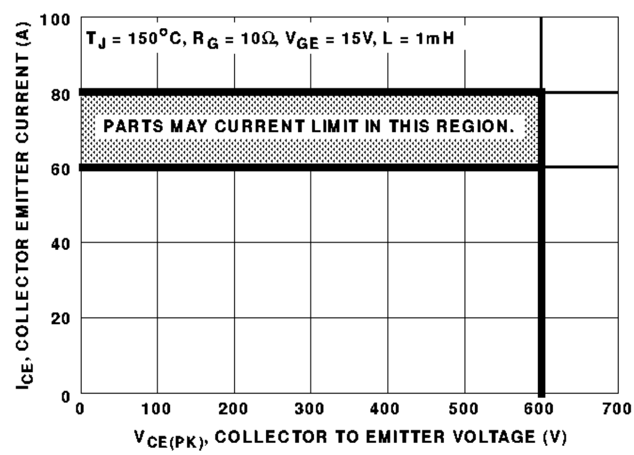


FIGURE 12. SWITCHING SAFE OPERATING AREA

Typical Performance Curves (Continued)

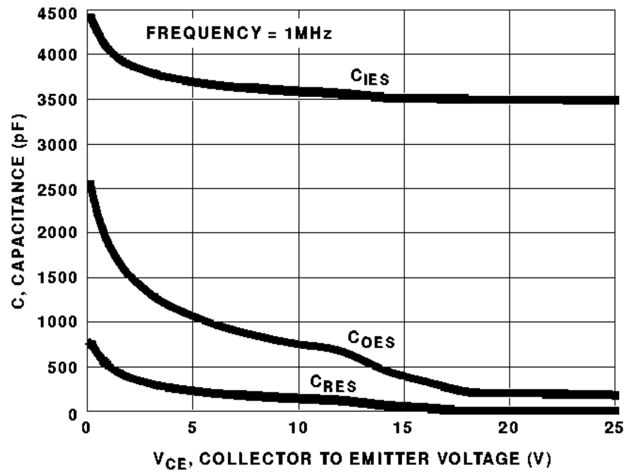


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

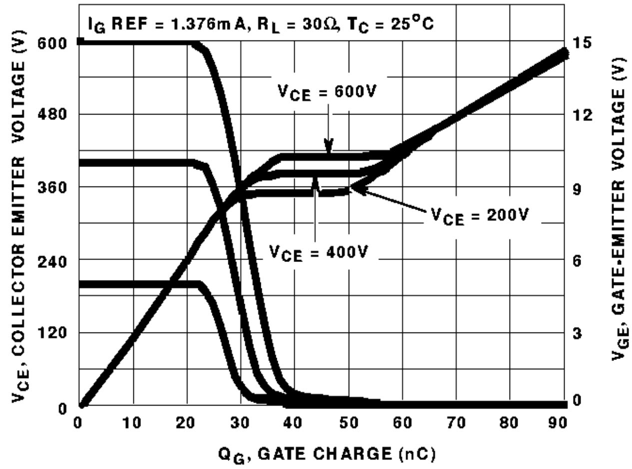


FIGURE 14. GATE CHARGE WAVEFORMS

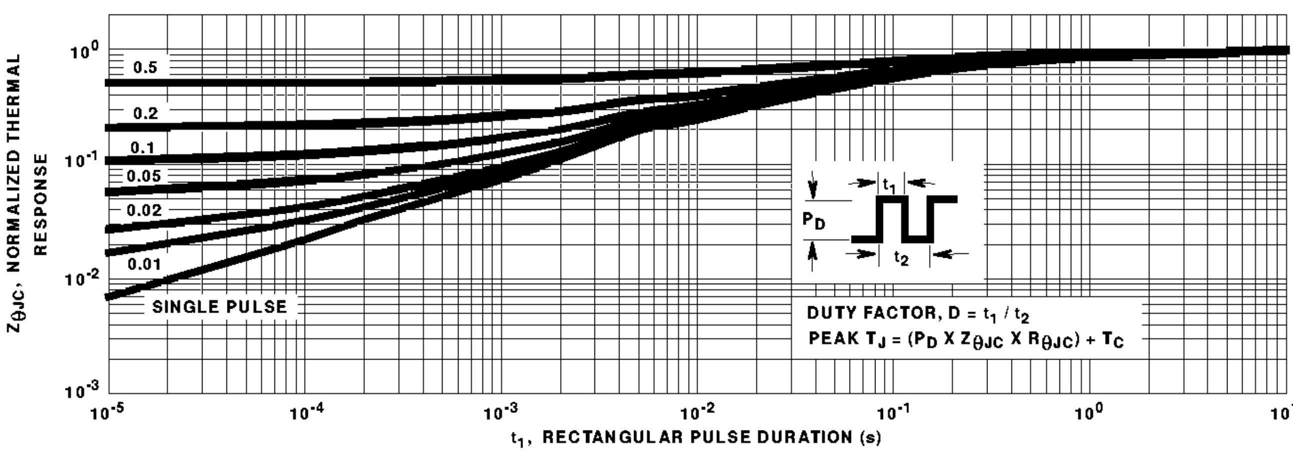


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Test Circuit and Waveform

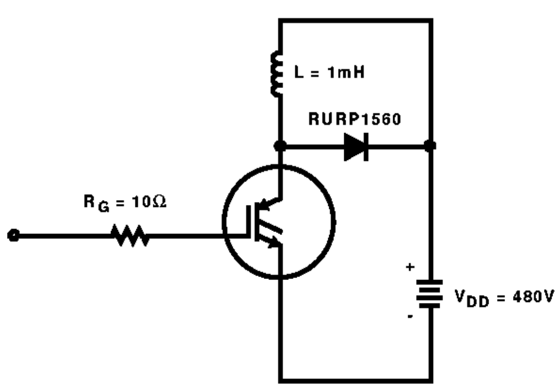


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

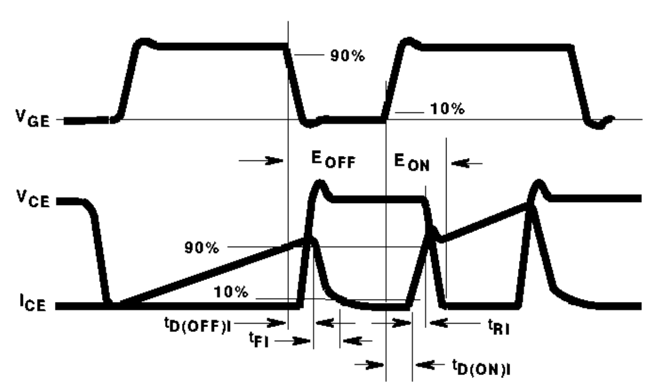


FIGURE 17. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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Operating Frequency Information

Operating frequency information for a typical device (Figure 11) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (ICE) plots are possible using the information shown for a typical unit in Figures 3, 5, 6, 9 and 10. The operating frequency plot (Figure 11) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 17. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 11) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 17. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

NORTH AMERICA
Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

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