

CMOS BCD-to-7-Segment Latch Decoder Drivers

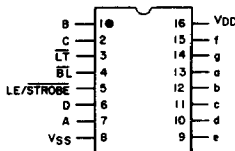
High-Voltage Types (20-Volt Rating)



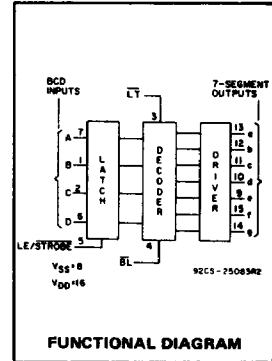
The CD4511B types are BCD-to-7-segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA CMOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test (\overline{LT}), Blanking (\overline{BL}), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used. The CD4511B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

These devices are similar to the type MC14511.



TOP VIEW
92CS-25084RM
CD4511B
TERMINAL ASSIGNMENT



Features:

- High-output-sourcing capability up to 25 mA
- Input latches for BCD Code storage
- Lamp Test and Blanking capability
- 7-segment outputs blanked for BCD input codes > 1001
- 100% tested for quiescent current at 20 V
- Max. input current of 1 μ A at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Driving common-cathode LED displays
- Multiplexing with common-cathode LED displays
- Driving incandescent displays
- Driving low-voltage fluorescent displays

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	\pm 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A): (Full Package-Temperature Range)	—	3	18	V
Set-Up Time (t_s)	5	150	—	ns
	10	70	—	ns
	15	40	—	ns
Hold Time (t_H)	5	0	—	ns
	10	0	—	ns
	15	0	—	ns
Strobe Pulse Width (t_W)	5	400	—	ns
	10	160	—	ns
	15	100	—	ns

CD4511B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				Limits at Indicated Temperatures (°C)							Units
	I_{OH} (mA)	V_o (V)	V_{IN} (V)	V_{DD} (V)	Values at -55, +25, +125 for D, F, K, H, Packages Values at -40, +25, +85 for E Packages				+25			
					-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current: I_{DD} Max.	-	-	-	5	5	5	150	150	-	0.04	5	μA
	-	-	-	10	10	10	300	300	-	0.04	10	
	-	-	-	15	20	20	600	600	-	0.04	20	
	-	-	-	20	100	100	3000	3000	-	0.08	100	
Output Voltage:	-	-	0.5	5	0.05				-	0	0.05	V
Low Level V_{OL} Max.	-	-	0.10	10	0.05				-	0	0.05	
	-	-	0.15	15	0.05				-	0	0.05	
High Level V_{OH} Min.	-	-	0.5	5	4	4	4.2	4.2	4.1	4.55	-	
	-	-	0.10	10	9	9	9.2	9.2	9.1	9.55	-	
	-	-	0.15	15	14	14	14.2	14.2	14.1	14.55	-	
Input Low Voltage, V_{IL} Max.	-	0.5, 3.8	-	5	1.5				-	-	1.5	V
	-	1.8, 8	-	10	3				-	-	3	
	-	1.5, 13.8	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	-	0.5, 3.8	-	5	3.5				3.5	-	-	V
	-	1.8, 8	-	10	7				7	-	-	
	-	1.5, 13.8	-	15	11				11	-	-	
Output Drive Voltage: High Level V_{OH} Min.	0	-	-	5	4.0	4.0	4.20	4.20	4.10	4.55	-	V
	5	-	-		-	-	-	-	-	-	4.25	-
	10	-	-		3.80	3.80	3.90	3.90	3.90	3.90	4.10	-
	15	-	-		-	-	3.50	3.50	-	-	3.95	-
	20	-	-		3.55	3.55	3.30	-	-	3.40	3.75	-
	25	-	-	3.40	3.40	-	-	-	3.10	3.55	-	
	0	-	-	10	9.0	9.0	9.20	9.20	9.10	9.55	-	V
	5	-	-		-	-	-	-	-	-	9.25	-
	10	-	-		8.85	8.85	9.00	9.00	9.00	9.00	9.15	-
	15	-	-		-	-	-	-	-	-	9.05	-
	20	-	-		8.70	8.70	8.40	8.40	8.60	8.60	8.90	-
	25	-	-	8.60	8.60	-	-	-	8.30	8.75	-	
0	-	-	15	14.0	14.0	14.20	14.20	14.10	14.55	-	V	
5	-	-		-	-	-	-	-	-	14.30	-	
10	-	-		13.90	13.90	14.0	14.0	14.0	14.0	14.20	-	
15	-	-		-	-	-	-	-	-	14.10	-	
20	-	-		13.75	13.75	13.50	13.50	13.70	13.95	-	-	
25	-	-	13.65	13.65	-	-	-	13.50	13.80	-		
Output Low (Sink) Current, I_{OL} Min.	-	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	-	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	-	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Input Current, I_{IN} Max.	-	0.18	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA

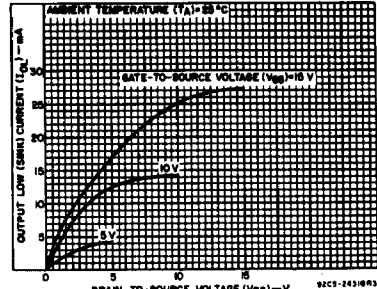


Fig. 1 - Typical output low (sink) current characteristics.

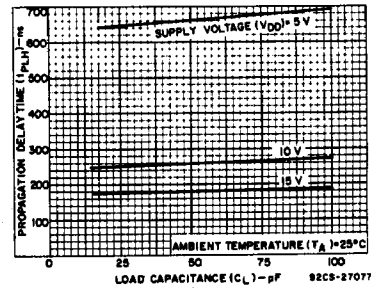


Fig. 2 - Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

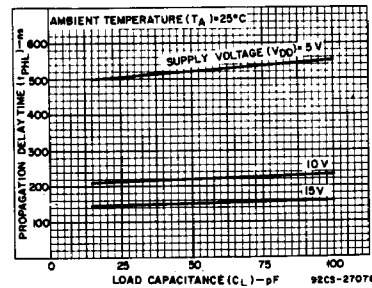


Fig. 3 - Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

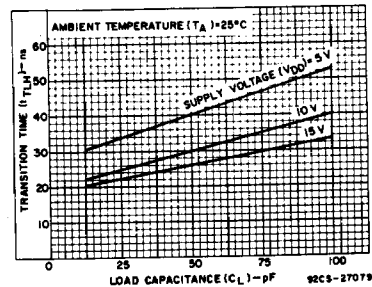


Fig. 4 - Typical low-to-high-level transition time as a function of load capacitance.

CD4511B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	Test Conditions	LIMITS All Packages			UNITS
		V_{DD} Volts	Min.	Typ.	
Propagation Delay Time: (Data) High-to-Low Level, t_{pHL}	5	—	520	1040	ns
	10	—	210	420	
	15	—	150	300	
Low-to-High Level, t_{pLH}	5	—	660	1320	ns
	10	—	260	520	
	15	—	180	360	
Propagation Delay Time: (BL) High-to-Low Level, t_{pHL}	5	—	350	700	ns
	10	—	175	350	
	15	—	125	250	
Low-to-High Level, t_{pLH}	5	—	400	800	ns
	10	—	175	350	
	15	—	150	300	
Propagation Delay Time: (LT) High-to-Low Level, t_{pHL}	5	—	250	500	ns
	10	—	125	250	
	15	—	85	170	
Low-to-High Level, t_{pLH}	5	—	150	300	ns
	10	—	75	150	
	15	—	50	100	
Transition Time: Low-to-High Level, t_{TLH}	5	—	40	80	ns
	10	—	30	60	
	15	—	25	50	
High-to-Low Level, t_{THL}	5	—	125	310	ns
	10	—	75	185	
	15	—	65	160	
Minimum Set-Up Time, t_S	5	150	75	—	ns
	10	70	35	—	
	15	40	20	—	
Minimum Hold Time, t_H	5	0	-75	—	ns
	10	0	-35	—	
	15	0	-20	—	
Strobe Pulse Width, t_W	5	400	200	—	ns
	10	160	80	—	
	15	100	50	—	
Input Capacitance, C_{iN}			5	7.5	pF

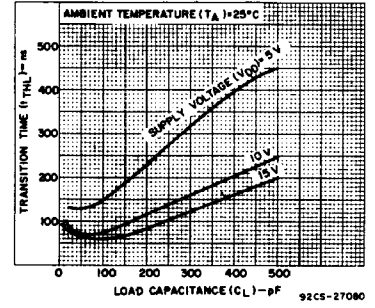


Fig. 5 - Typical high-to-low transition time as a function of load capacitance.

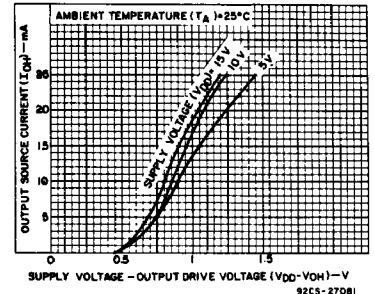


Fig. 6 - Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.

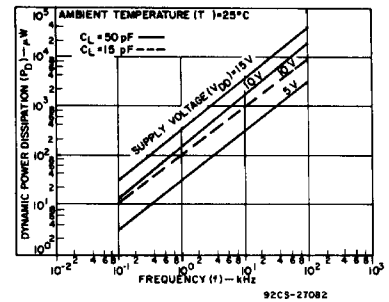


Fig. 7 - Typical dynamic power dissipation characteristics

CD4511B Types

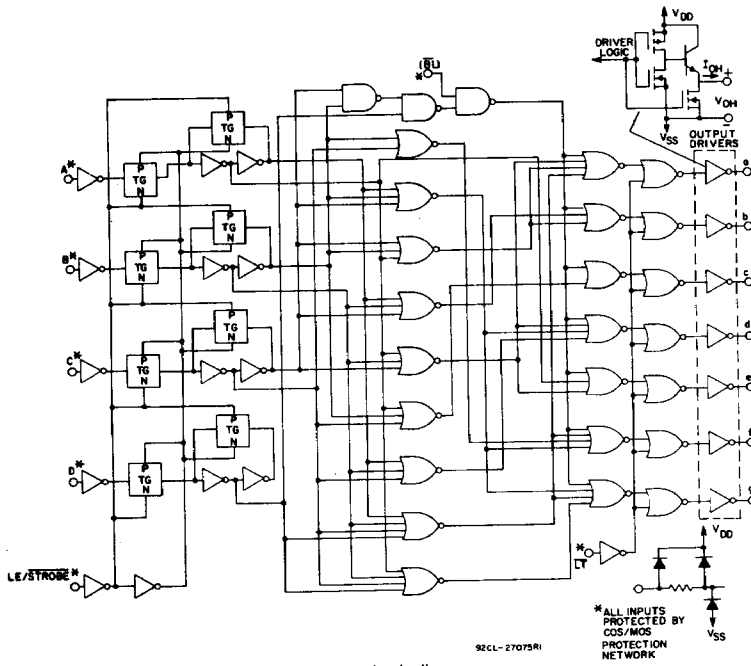


Fig. 8 - Logic diagram.

TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	0	2
0	1	1	0	0	1	1	1	1	1	0	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*	*	*	*	*	*	*	*

X ≡ Don't Care * Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

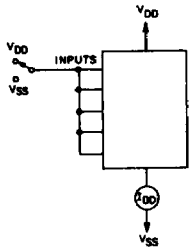


Fig. 9 - Quiescent device current.

TEST CIRCUITS

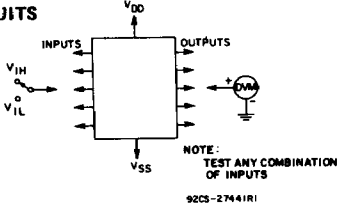


Fig. 10 - Input voltage.

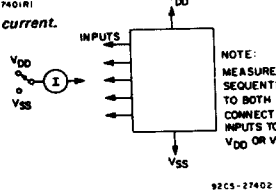
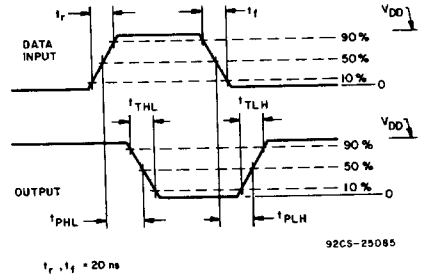


Fig. 11 - Input current.



$t_r, t_f = 20 \text{ ns}$

92CS-25085

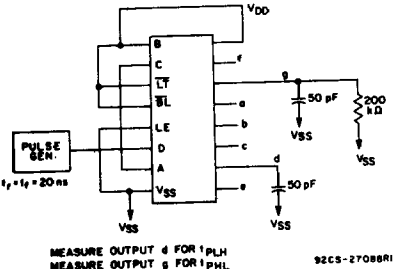


Fig. 12 - Data propagation delay.

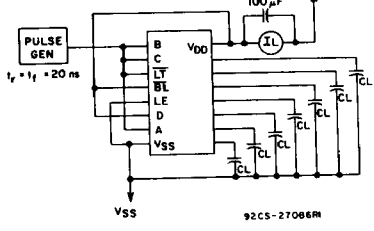
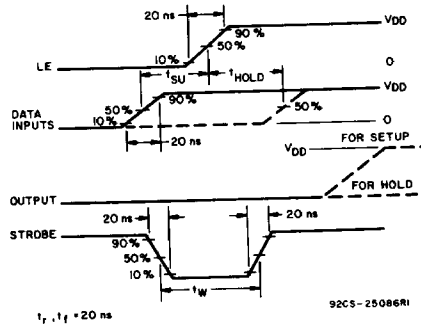


Fig. 13 - Dynamic power dissipation.

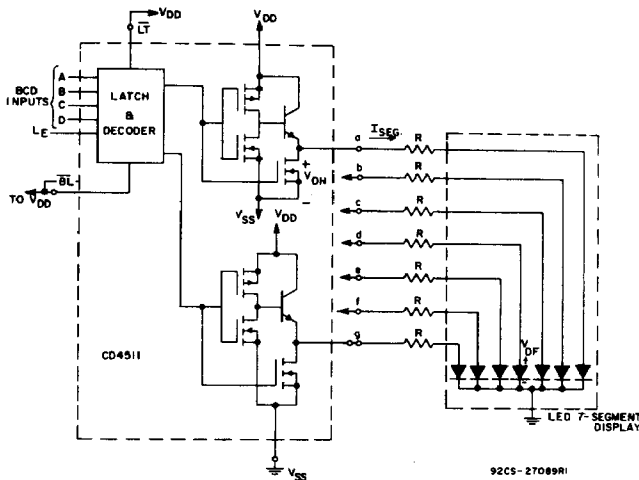


$t_r, t_f = 20 \text{ ns}$

92CS-25086R1

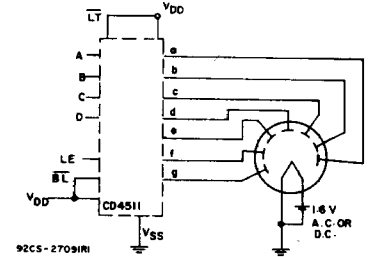
Fig. 14 - Dynamic waveforms.

APPLICATIONS Interfacing with Various Displays



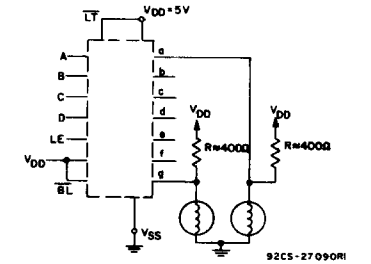
Duty Cycle = 100%
 $I_{SEG} = I_{DIODE\ AVG.} = 20\text{ mA at Luminous Intensity/Segment} = 250\text{ microcandles}$
 $R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$

Fig. 15 - Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).



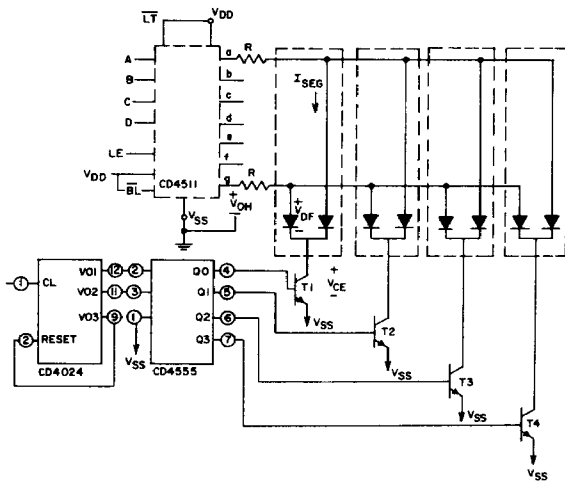
A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.
 Fig. 16 - Driving low-voltage fluorescent displays.



2 of 7 Segments Shown Connected
 Resistors R from VDD to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

Fig. 17 - Driving incandescent displays (RCA Numitron DR2000 series displays).

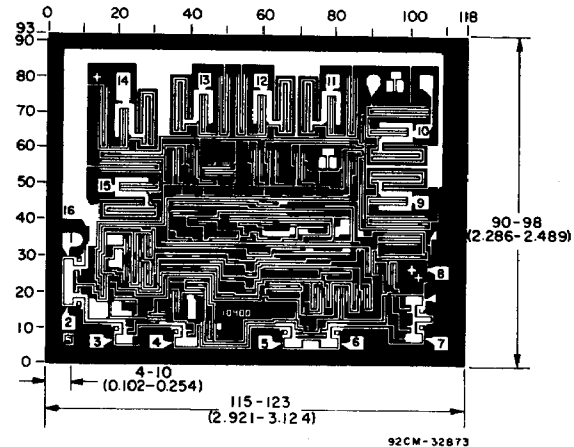


Multiplexing Scheme Showing 2 of 7 Segments Connected
 Transistors T₁-T₄ (RCA-2N3053 or 2N2102) have I_C Max. rating > 7x I_{SEG}

Duty Cycle = 25%
 $I_{SEG} = |I_{DIODE\ AVG.}| \times 4$
 $R = \frac{V_{OH} - V_{DF} - V_{CE}}{I_{SEG}}$

All unused inputs on CD4555 are connected to VDD or VSS.

Fig. 18 - Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).



Dimensions and pad layout for CD4511B chip.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).