67413A/67413

First-In First-Out (FIFO)
64 x 5 Memory

Advanced Micro Devices

Features/Benefits

- **High-speed 35 MHz shift-in/shift-out rates**
- **High-drive capability**
- **Three-state outputs**
- **Half-full and Almost-full/Empty status flags**
- **Structured pinouts. Output pins directly opposite corresponding input pins.**
- **Asynchronous operation**
- **TTL-compatible inputs and outputs**

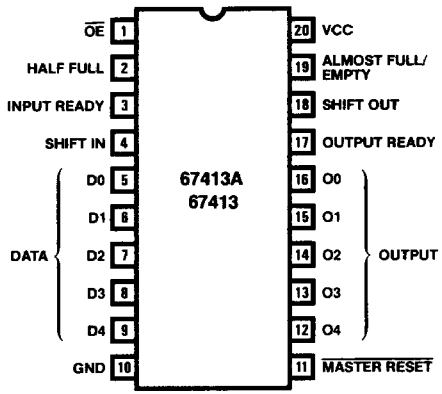
Description

The 67413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 35-MHz input/output rates (67413 operates at 25-MHz in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be connected in parallel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

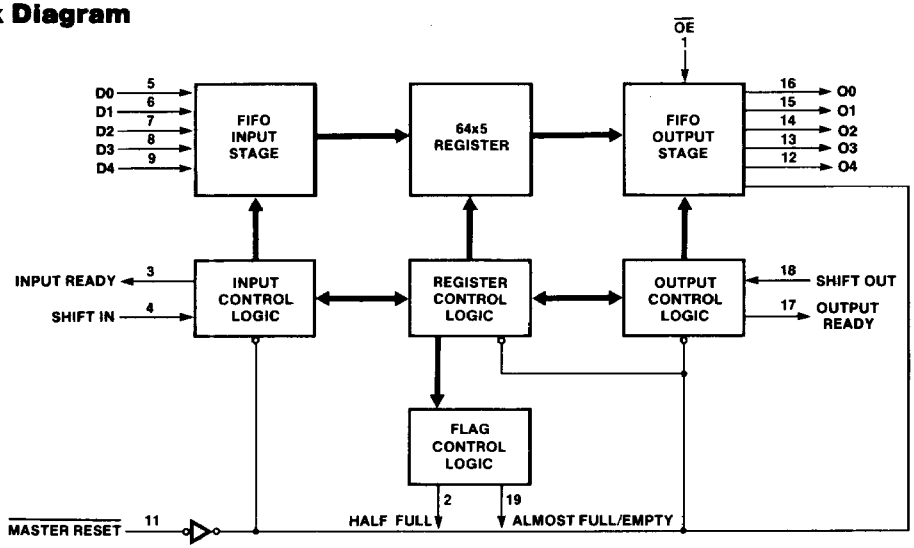
Ordering Information

Part Number	Package	Temp	Description
67413A	CD 020	Com	35 MHz in/out
67413	CD 020	Com	25 MHz in/out

Pin Configuration



Block Diagram



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Publication # 10678 Rev. A Amendment /0
Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 to 7 V
Input voltage ..... -1.5 to 7 V
Off-state output voltage ..... -0.5 to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	67413A MIN	67413A TYP	67413A MAX	67413 MIN	67413 TYP	67413 MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
T_A	Operating free-air temperatue		0		75	0		75	°C
t_{SIH}†	Shift in HIGH time	1	9			16			ns
t_{SIL}†	Shift in LOW time	1	17			20			ns
t_{IDS}	Input data setup	1	2			3			ns
t_{IDH}	Input data hold time	1	15			25			ns
t_{SOH}†	Shift Out HIGH time	5	9			16			ns
t_{SOL}	Shift Out LOW time	5	17			20			ns
t_{MRW}†	Master Reset pulse	10	30			35			ns
t_{MRS}	Master Reset to SI	10	35			35			ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67413A MIN	67413A TYP	67413A MAX	67413 MIN	67413 TYP	67413 MAX	UNIT
f_{IN}	Shift in rate	1	DC DC		††30 †††35	DC		25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	18		12	28	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	20		14	25	ns
f_{OUT}	Shift Out rate	5	DC DC		††30 †††35	DC		25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	18		12	28	ns
t_{ORH}†	Shift Out † to Output Ready HIGH	5		14	20		14	25	ns
t_{ODH}†	Output Data Hold (previous word)	5	12				10		ns
t_{ODS}	Output Data Shift (next word)	5			34			40	ns
t_{PT}	Data throughput or "fall through"	4, 8		510	650		510	750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	28		18	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	28		21	30	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	28		18	30	ns
t_{MRO}*	Master Reset ↓ to Outputs LOW	10		32	45		32	55	ns

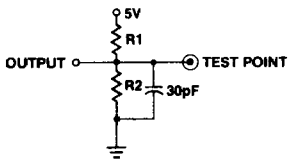
Note: Typicals at 5 V V_{CC} and 25°C T_A.
* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.
†† Tested
††† Guaranteed by design. (see test load).

Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	67413A MIN	67413A TYP	67413A MAX	67413 MIN	67413 TYP	67413 MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			18			20	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	135		100	145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	600		450	650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	600		450	650	ns
t_{AFH}*	Shift In ↑ AF/E HIGH	12		100	135		100	145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	360		280	380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	360		280	380	ns
t_{PHZ}	Output Disable Delay	A		14	25		14	30	ns
t_{PLZ}		A		14	25		14	30	
t_{PZL}	Output Enable Delay	A		14	25		14	30	ns
t_{PZH}		A		24	38		24	50	

Note: Input rise and fall time (10%-90%) = 2.5 ns. * See timing diagram for explanation of parameters.

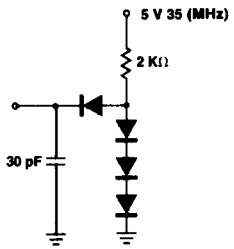
Standard Test Load



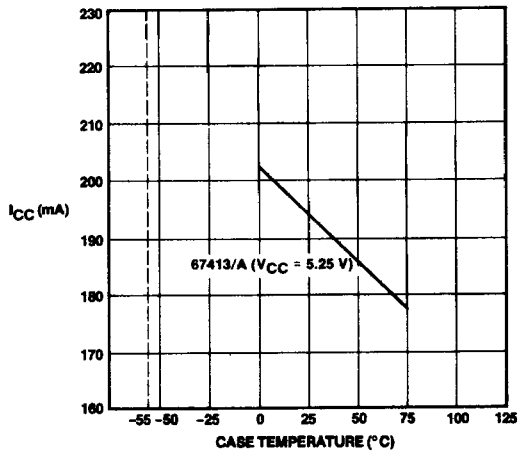
I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V

Design Test Load



Typical I_{CC} vs Temperature (V_{CC} = MAX)



67413 Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL			UNIT
			MIN	TYP	MAX	
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			20	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	650	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		100	145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	380	ns
t_{PHZ}	Output Disable Delay	A		14	30	ns
t_{PLZ}		A		14	30	ns
t_{PZL}	Output Enable Delay	A		14	30	ns
t_{PZH}		A		24	50	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns.

* See timing diagram for explanation of parameters.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

67413 Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	16			ns
t_{SIL}†	Shift in LOW time	1	20			ns
t_{IDS}	Input data set up	1	3			ns
t_{IDH}	Input data hold time	1	25			ns
t_{SOH}†	Shift Out HIGH time	5	16			ns
t_{SOL}	Shift Out LOW time	5	20			ns
t_{MRW}	Master Reset pulse †	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

67413 Switching Characteristics Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	DC		25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	28	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	25	ns
f_{OUT}	Shift Out rate	5	DC		25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	28	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	25	ns
t_{ODH}†	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			40	ns
t_{PT}	Data throughput or "fall through"	4,8		510	750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	30	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	30	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	55	ns

Note: Typicals at 5 V V_{CC} and 25°C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8†	V
V_{IH}	High-level input voltage					2†			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V					−250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data outputs)	67413A 67413	24 mA			0.5	V
			I_{OL} (IR, OR)	67413A 67413	8 mA††				
			I_{OL} (Flag outputs)	67413A 67413	8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data outputs)	67413A 67413	−3.0 mA	2.4			V
			I_{OH} (IR,OR)		−0.9 mA				
			I_{OH} (Flag outputs)		−0.9 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{HZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V					+20	μA
I_{LZ}		V_{CC} = MAX	V_O = 0.4 V					−20	μA
I_{CC}	Supply current	V_{CC} = MAX. All inputs low. All outputs open. (67413A/67413)						**240	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** See curve for I_{CC} vs. temp.

† There are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition,

care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a funcitonal standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-ingoing HIGH. This same type of problem is also related to T_{IRH}, T_{ORL} and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

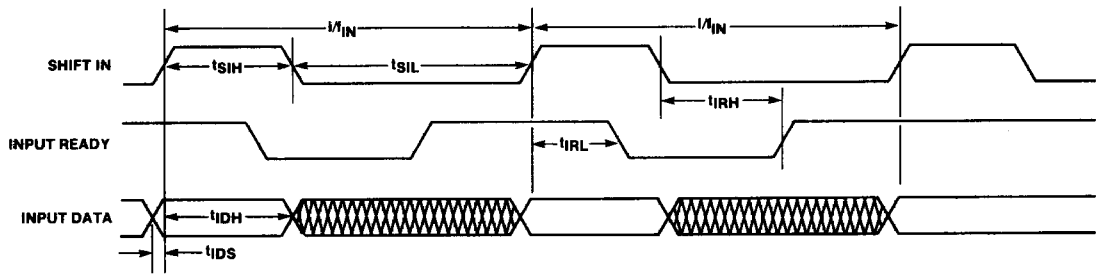


Figure 1. Input Timing

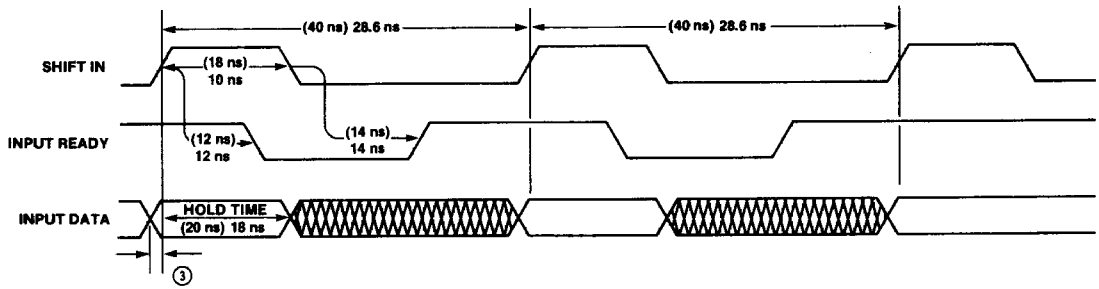


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate (67413A)

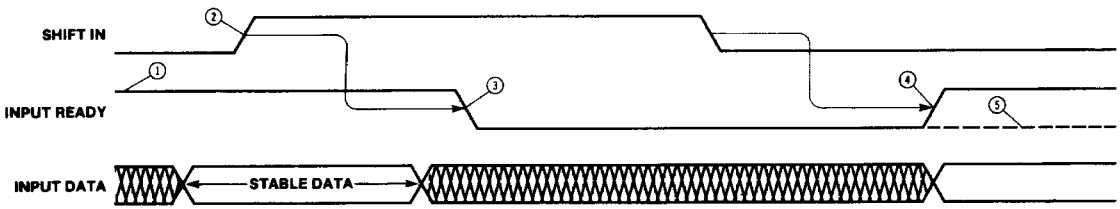


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
5. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

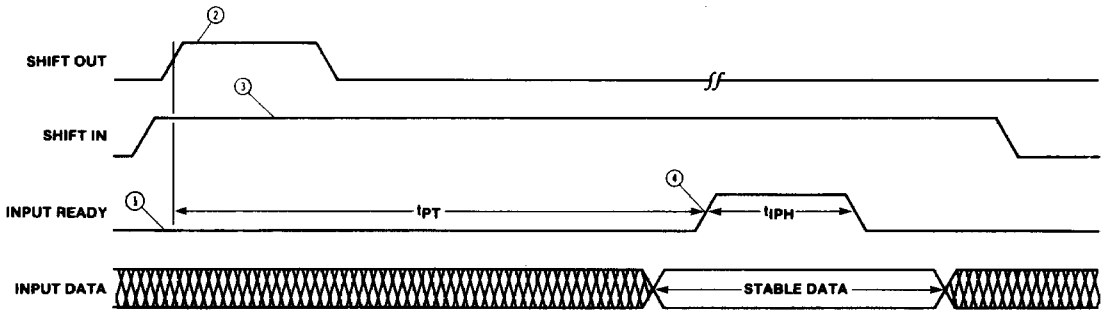


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

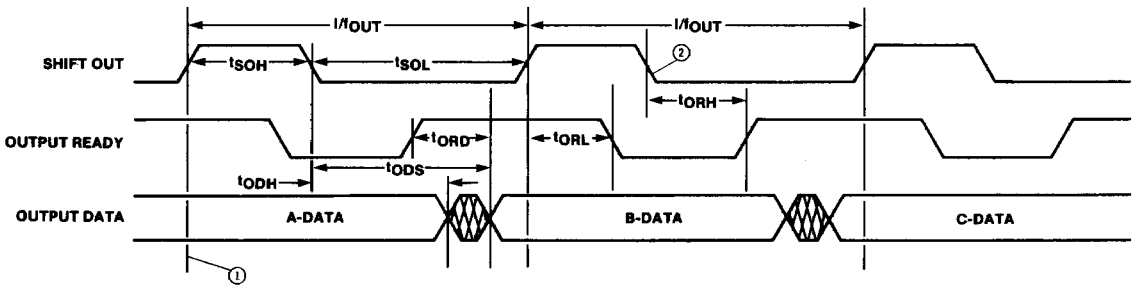


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

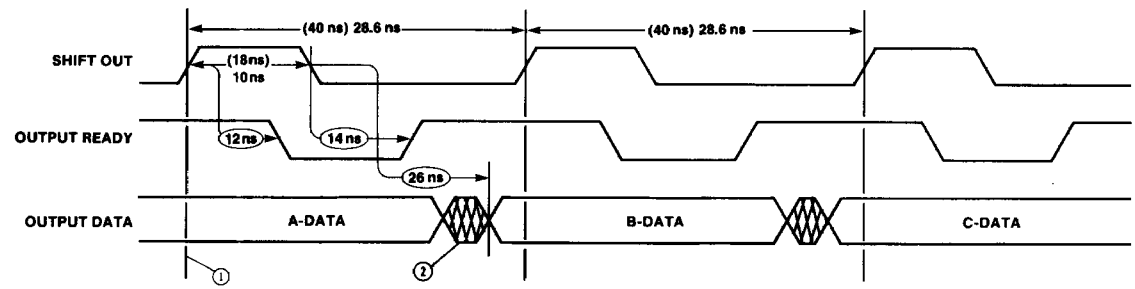


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate (67413A)

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

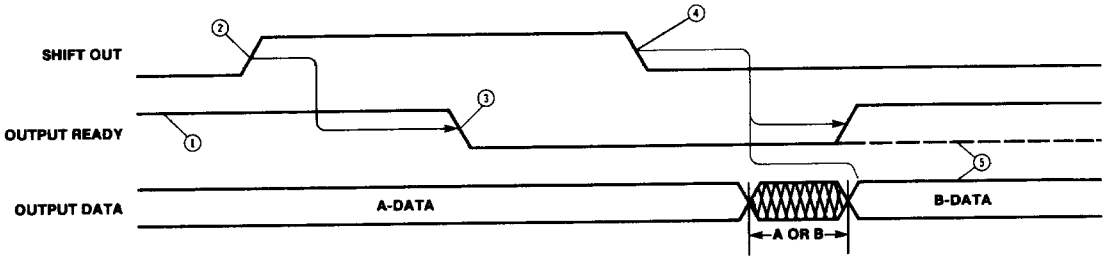


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

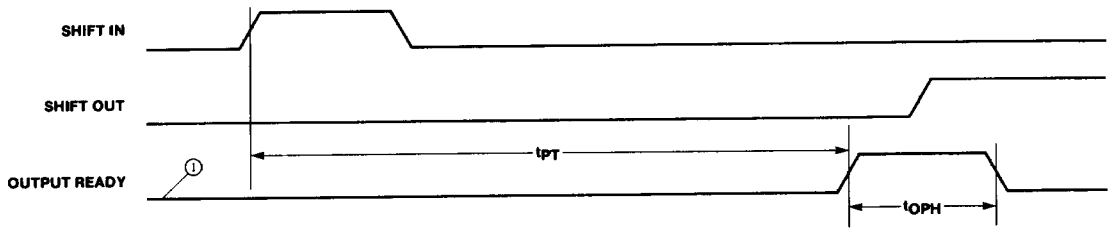


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

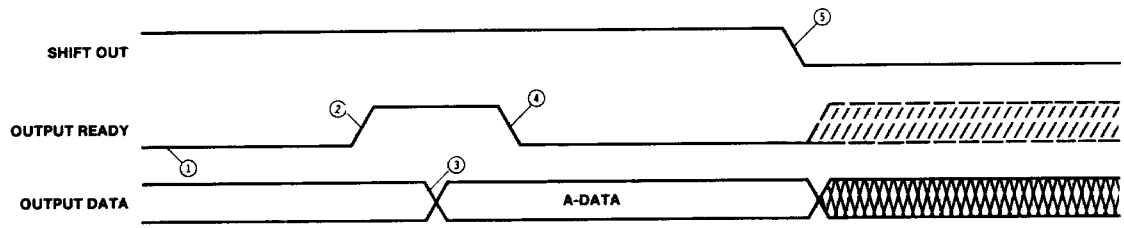


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

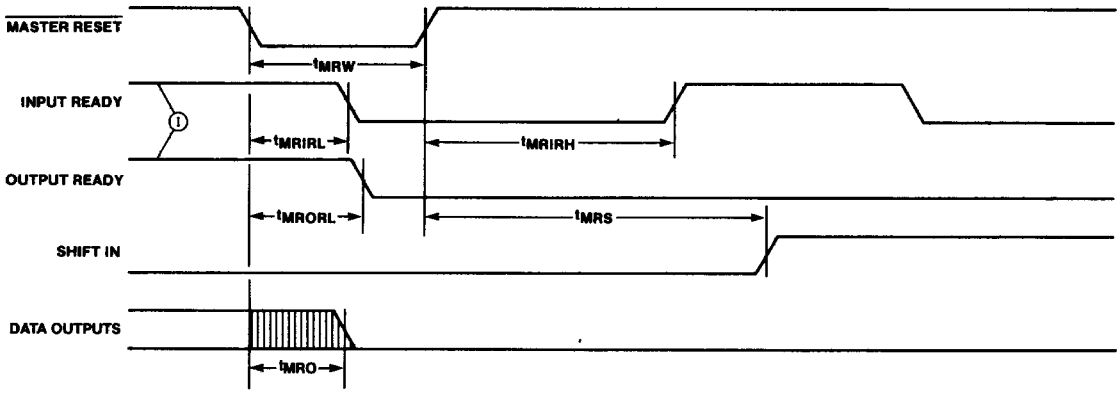


Figure 10. Master Reset Timing

① FIFO is partially full.

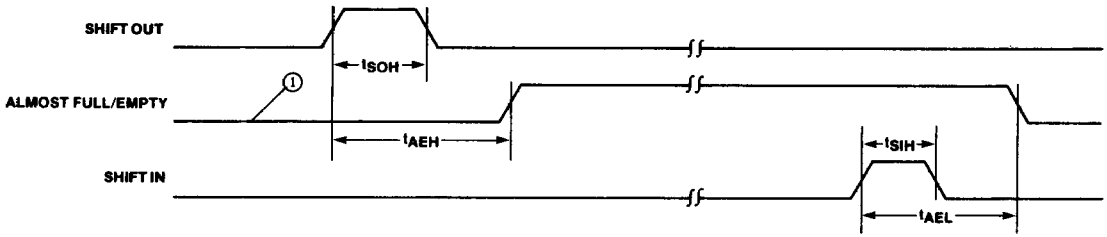


Figure 11. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

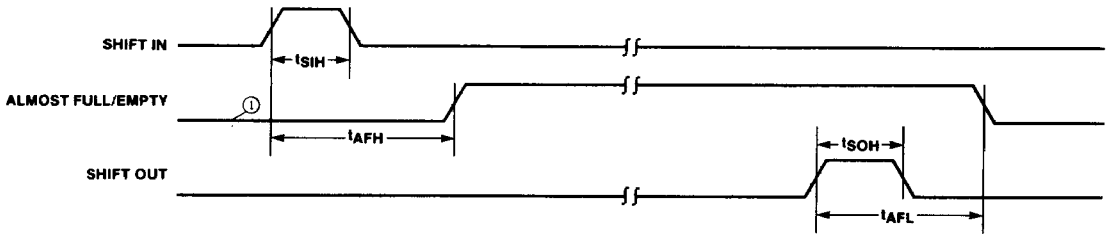


Figure 12. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full)

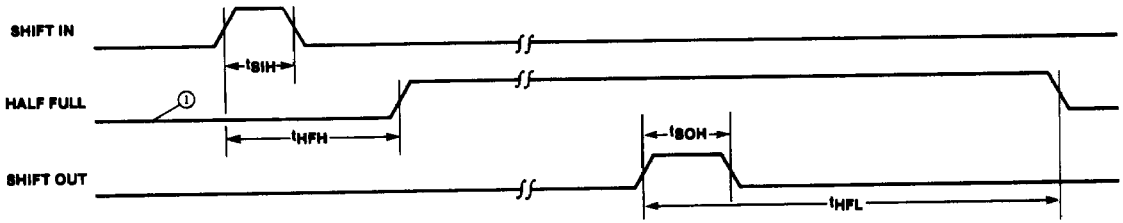


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).

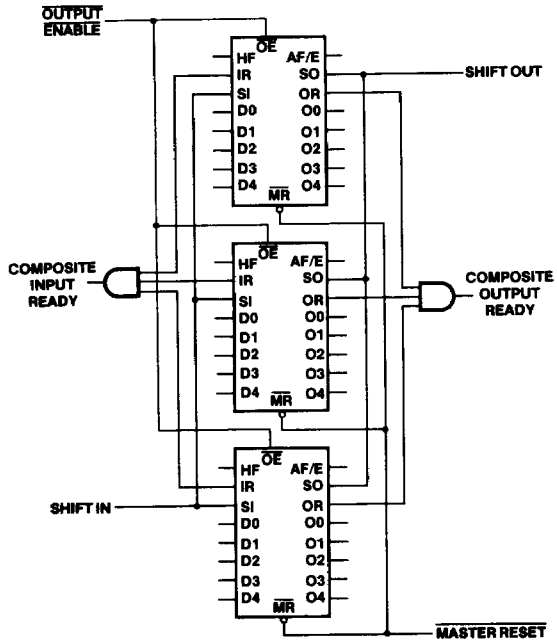


Figure 14. 64x15 FIFO with 67413A/67413

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.

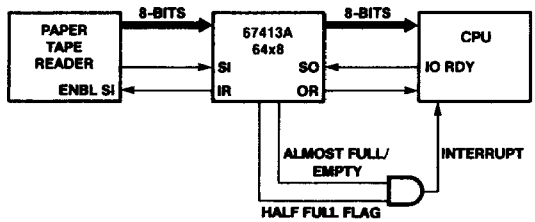
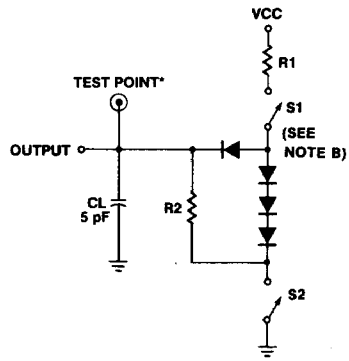


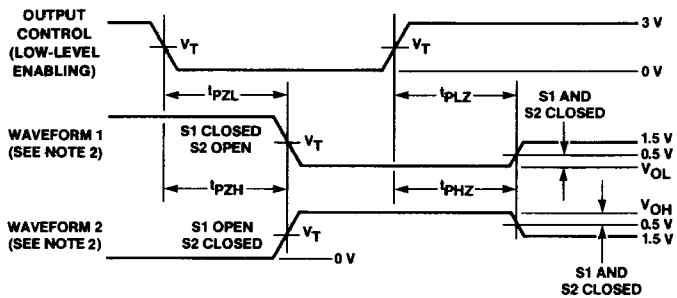
Figure 15. Application for 67413A "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

Three-State Test Load



Design Test Load



Enable and Disable

Notes: A. All diodes are 1N916 or 1N3064.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

D. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.