67401 67401A 67402 67402A

First-In First-Out (FIFO)
64x4   64x5 Standalone Memory

DISTINCTIVE CHARACTERISTICS

- **Choice of 15 and 10 MHz shift-out/shift-in rates**
- **Choice of 4-bit or 5-bit data width**
- **TTL inputs and outputs**
- **Readily expandable in word dimension only**
- **Structured pinouts. Output pins directly opposite corresponding input pins**
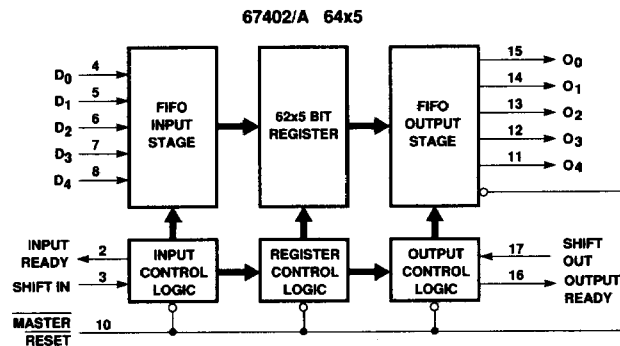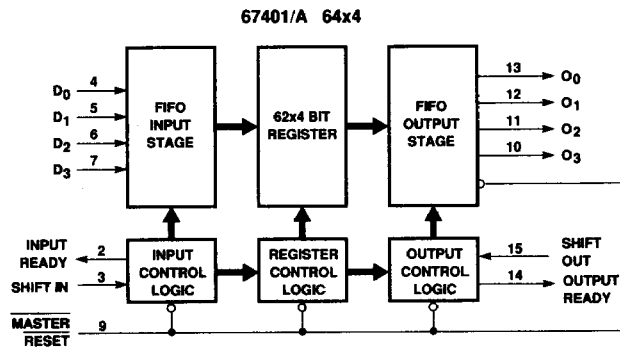- **Asynchronous operation**

ORDERING INFORMATION

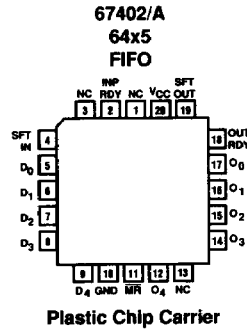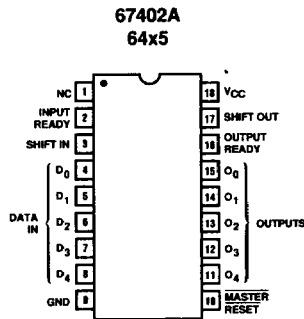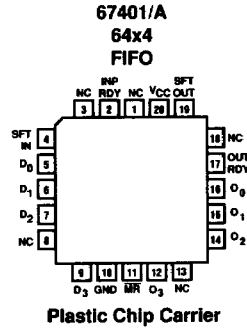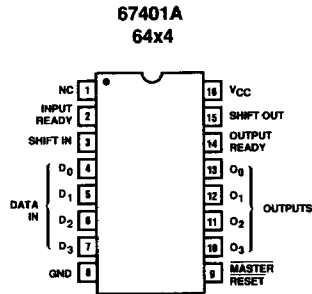| Part Number	Package	Temp	Description
67401	CD 016,PD 016,PL 020	Com	10 MHz 64x4 FIFO
67402	CD 018,PD 018,PL 020	Com	10 MHz 64x5 FIFO
67401A	CD 016,PD 016,PL 020	Com	15 MHz 64x4 FIFO
67402A	CD 018,PD 018,PL 020	Com	15MHz 64x5 FIFO

GENERAL DESCRIPTION

The 67401/1A/2/2A are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. A 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.
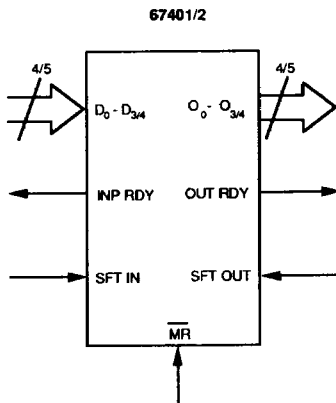
BLOCK DIAGRAMS

67401/A 64x4

67402/A 64x5

CONNECTION DIAGRAMS

67401A
64x4

NC	1	16	V_{CC}
INPUT READY	2	15	SHIFT OUT
SHIFT IN	3	14	OUTPUT READY
DATA IN D_0	4	13	O_0
D_1	5	12	O_1 OUTPUTS
D_2	6	11	O_2
D_3	7	10	O_3
GND	8	9	$\overline{\text{MASTER RESET}}$

67401/A
64x4
FIFO

Pins top: NC 3, INP RDY 2, NC 1, V_{CC} 20, SFT OUT 19

SFT IN 4 — 18 NC
D_0 5 — 17 OUT RDY
D_1 6 — 16 O_0
D_2 7 — 15 O_1
NC 8 — 14 O_2

Pins bottom: D_3 9, GND 10, $\overline{MR}$ 11, O_3 12, NC 13

Plastic Chip Carrier

67402A
64x5

NC	1	18	V_{CC}
INPUT READY	2	17	SHIFT OUT
SHIFT IN	3	16	OUTPUT READY
DATA IN D_0	4	15	O_0
D_1	5	14	O_1
D_2	6	13	O_2 OUTPUTS
D_3	7	12	O_3
D_4	8	11	O_4
GND	9	10	$\overline{\text{MASTER RESET}}$

67402/A
64x5
FIFO

Pins top: NC 3, INP RDY 2, NC 1, V_{CC} 20, SFT OUT 19

SFT IN 4 — 18 OUT RDY
D_0 5 — 17 O_0
D_1 6 — 16 O_1
D_2 7 — 15 O_2
D_3 8 — 14 O_3

Pins bottom: D_4 9, GND 10, $\overline{MR}$ 11, O_4 12, NC 13

Plastic Chip Carrier

LOGIC SYMBOL

67401/2

4/5 → D_0 - $D_{3/4}$ O_0 - $O_{3/4}$ → 4/5

INP RDY   OUT RDY

SFT IN   SFT OUT

$\overline{MR}$

10676-001A

PIN DESCRIPTION

D_0 - $D_{3/4}$	=	Data Input
O_0 - $O_{3/4}$	=	Data Output
INP RDY	=	Input Ready
OUT RDY	=	Output Ready
SFT IN	=	Shift In
SFT OUT	=	Shift Out
$\overline{MR}$	=	Master Reset
V_{CC}	=	5 V Power Supply
GND	=	Ground

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} .... -1.5 V to +7.0 V
Input voltage .... -1.5 V to +7.0 V
Off-state output voltage .... -0.5 V to +5.5 V
Storage temperature .... -65°C to +150°C

OPERATING CONDITIONS

Symbol	Parameter	Figure	67401A/2A			67401/2			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		0		75	0		75	°C
t_{SIH}†	Shift-In HIGH Time	1	23		28†	35			ns
t_{SIL}	Shift-In LOW Time	1	25			35			ns
t_{IDS}	Input Data Setup	1	5			5			ns
t_{IDH}	Input Data Hold Time	1	40			45			ns
t_{SOH}†	Shift-Out HIGH Time	5	23			35			ns
t_{SOL}	Shift-Out LOW Time	5	25			35			ns
t_{MRW}	Master Reset Pulse	10	35			35			ns
t_{MRS}	Master Reset to SI	10	35			35			ns

SWITCHING CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Figure	67401A/2A			67401/2			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{IN}	Shift-In Rate	1	15			10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			40			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			40			45	ns
f_{OUT}†	Shift-Out Rate	5	15			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			45			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			50			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			45			55	ns
t_{PT}	Data Throughput or "Fall Through"	4, 8			1.6			3	μs
t_{MRORL}	Master Reset to OR LOW	10			60			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			60			60	ns
t_{IPH}*	Input Ready Pulse HIGH	4	23			23			ns
t_{OPH}*	Output Ready Pulse HIGH	8	23			23			ns

† See AC test and high speed application note.

TEST LOAD

* The "TEST POINT" is driven by the output under test and observed by instrumentation.

5 V

560 Ω

TEST POINT*

1.1 KΩ   30 pF
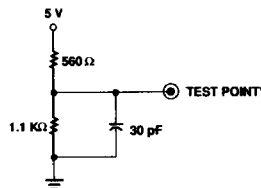
Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

DC CHARACTERISTICS Over Operating Conditions

Symbol	Parameter		Test Conditions		Min Typ Max	Unit
V_{IL}	Low-level input voltage				0.8†	V
V_{IH}	High-level input voltage				2†	V
V_{IC}	Input Clamp Voltage		V_{CC} = MIN	I_I = −18 mA	−1.5	V
$I_{IL}1$	Low-Level Input Current	D_0–D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45 V	−0.8	mA
$I_{IL}2$		SI, SO			−1.6	mA
I_{IH}	High-Level Input Current		V_{CC} = MAX	V_I = 2.4 V	50	µA
I_I	Maximum Input Current		V_{CC} = MAX	V_I = 5.5 V	1	mA
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN	I_{OL} = 8 mA	0.5	V
V_{OH}	High-Level Output Voltage		V_{CC} = MIN	I_{OH} = −0.9 mA	2.4	V
I_{OS}	Output Short-Circuit Current		V_{CC} = MAX	V_O = 0 V	−20 −90	mA
I_{CC}	Supply Current		V_{CC} = MAX All inputs low. All outputs open.	67401	160	
				67402	180	
				67401A	170	
				67402A	190	

*   No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

†   These are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to system or tester noise.

FUNCTIONAL DESCRIPTION
Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH, the location is ready to accept data from the D_n inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_x outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_x remains as before (i.e., data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC TEST AND HIGH SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized withing the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

SWITCHING WAVEFORMS
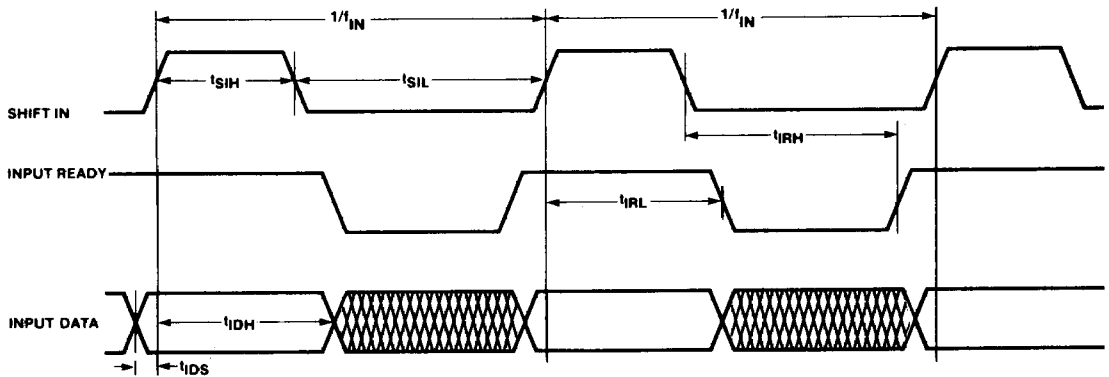
SWITCHING WAVEFORMS

Figure 1.   Input Timing

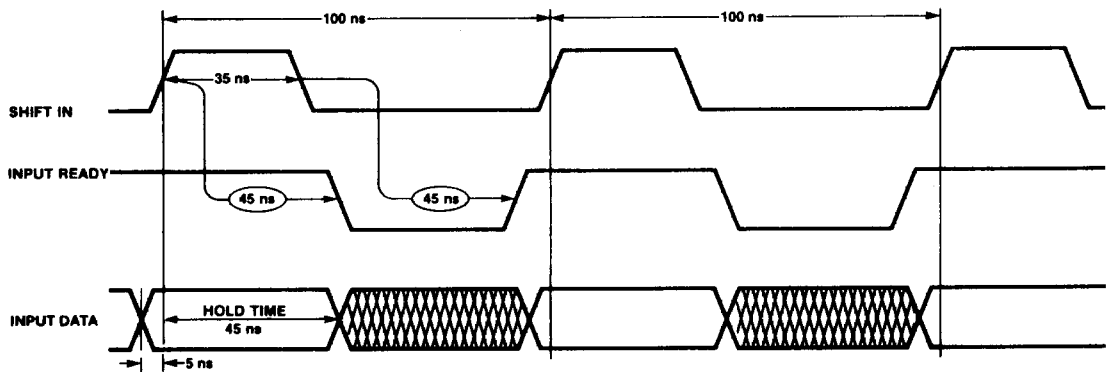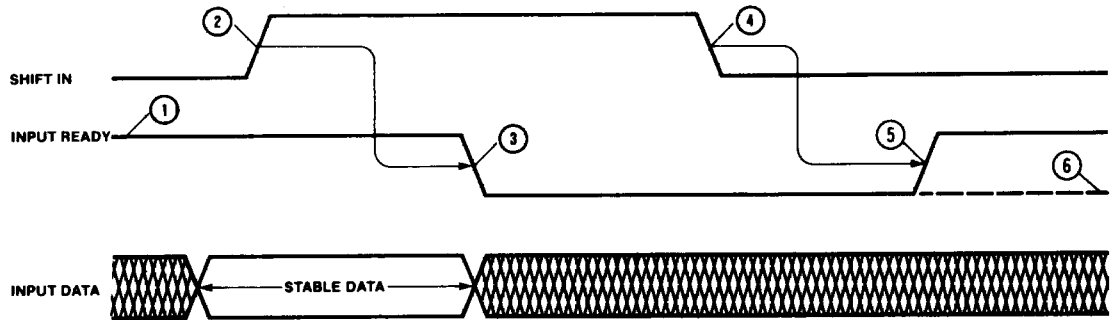Figure 2.   Typical Waveforms for 10-MHz Shift In Data Rate (67401/2)

SWITCHING WAVEFORMS

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.

② Input Data is loaded into the first word.

③ Input Ready goes LOW indicating the first word is full.

④ The Data from the first word is released for "fall-through" to second word.

⑤ The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

⑥ If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains low.

NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 3).

Figure 3. The Mechanism of Shifting Data Into the FIFO
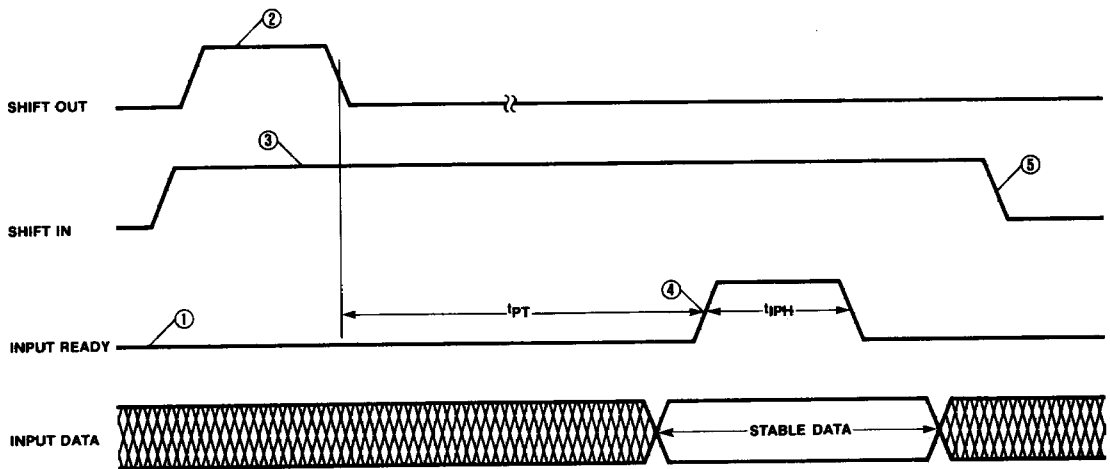
① FIFO is initially full.

② Shift Out pulse is applied. An empty location sarts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

⑤ The Data from the first word is released for "fall through" to second word.

Figure 4. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH
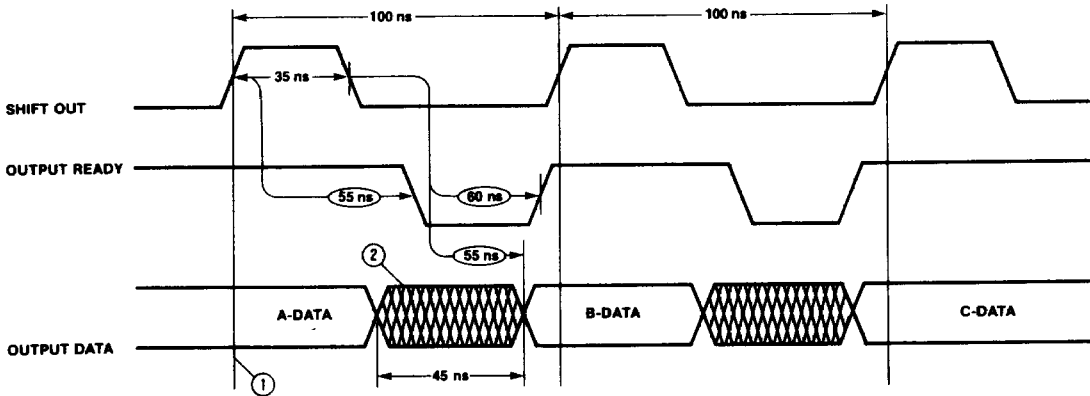
SWITCHING WAVEFORMS
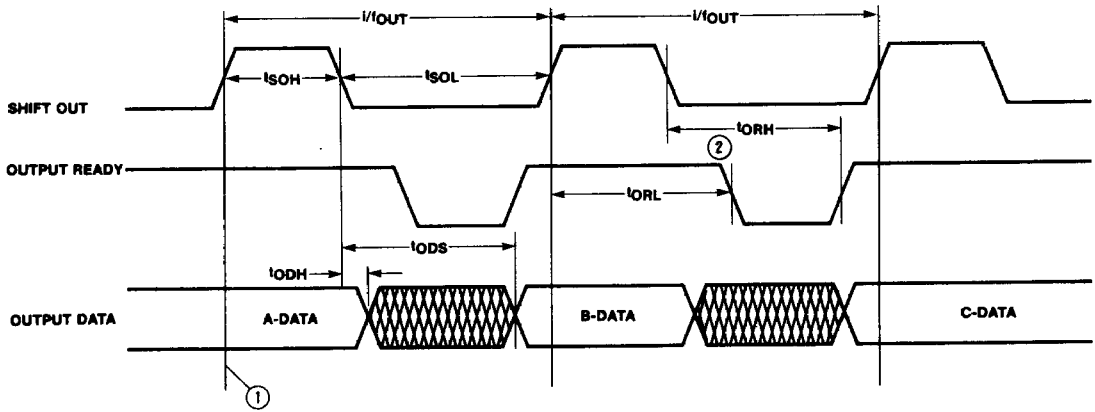
① The diagram assumes that at this time, words 63, 62, and 61 are loaded with A, B, and C Data, respectively.

② Data is shifted out when Shift Out makes a HIGH-to-LOW transition.
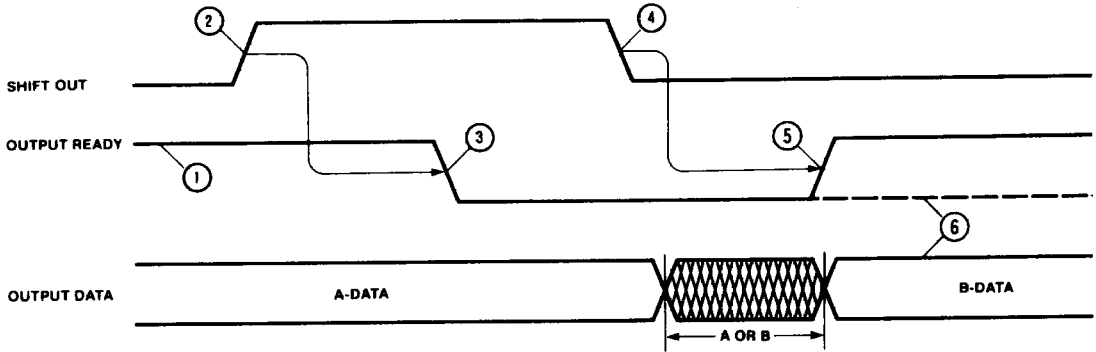
Figure 5.   Ouput Timing

2

① The diagram assumes that at this time words 63, 62, and 61 are loaded with A, B, and C Data respectively.

② Data in the crosshatched region may be A or B Data.

**Figure 6.   Typical Waveforms for 10-MHz Shift Out Data Rate (67401/2)**

SWITCHING WAVEFORMS

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the next step.

③ Output Ready goes LOW.

④ Contents of word 62 (B-DATA) to be released for "fall-through" to word 63.

⑤ Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

⑥ If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Reasdy is LOW will be ignored.

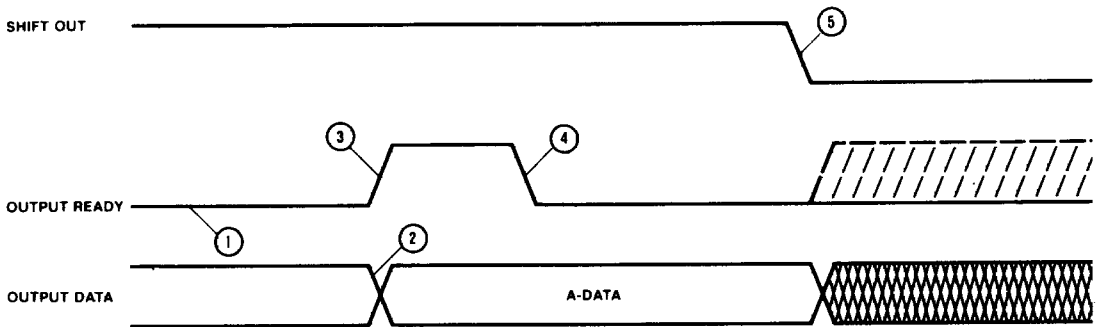**Figure 7. The Mechanism of Shifting Data Out of the FIFO**
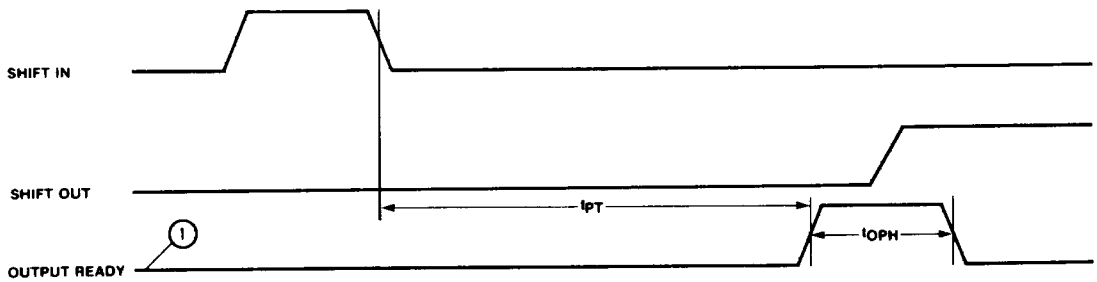
① FIFO is initially empty.

② Shift Out held HIGH.

Figure 8. t_{PT} and t_{OPH} Specification

SWITCHING WAVEFORMS

① Word 63 is empty.

② New data (A) arrives at the outputs (word 63).

③ Output Ready goes HIGH indicating arrival of the new data.

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

Figure 9.   Data Is Shifted Out Whenever Shift Out and Output ready Are Both HIGH
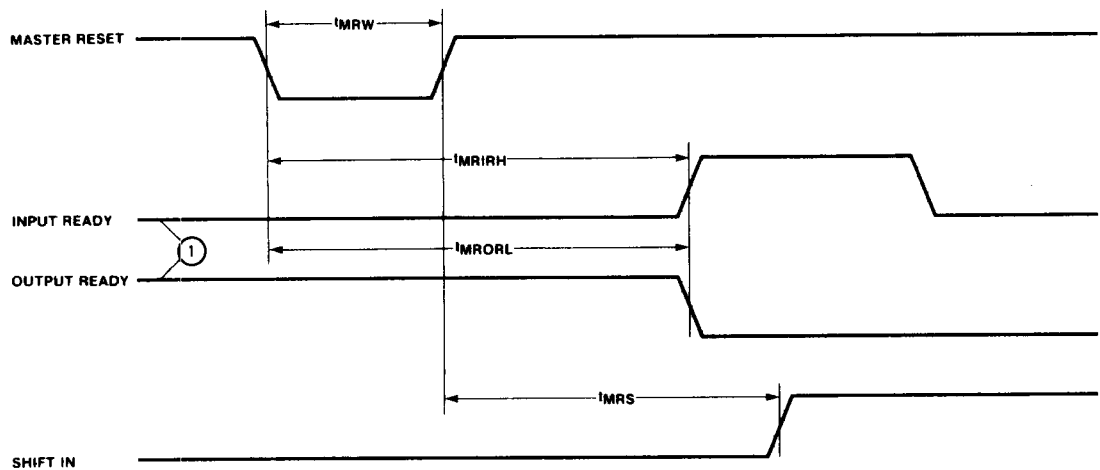
① FIFO is initially full.

Figure 10.   Master Reset Timing