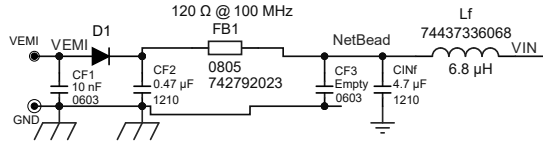


APM80951 Evaluation Board Low-EMI 1.5 A PWM Dimmable SR Buck LED Module

EMC filter configuration



Schematic for APM80951

RFPWM = 0 Ω, Rdrb = 0 Ω, Rdrf = Empty

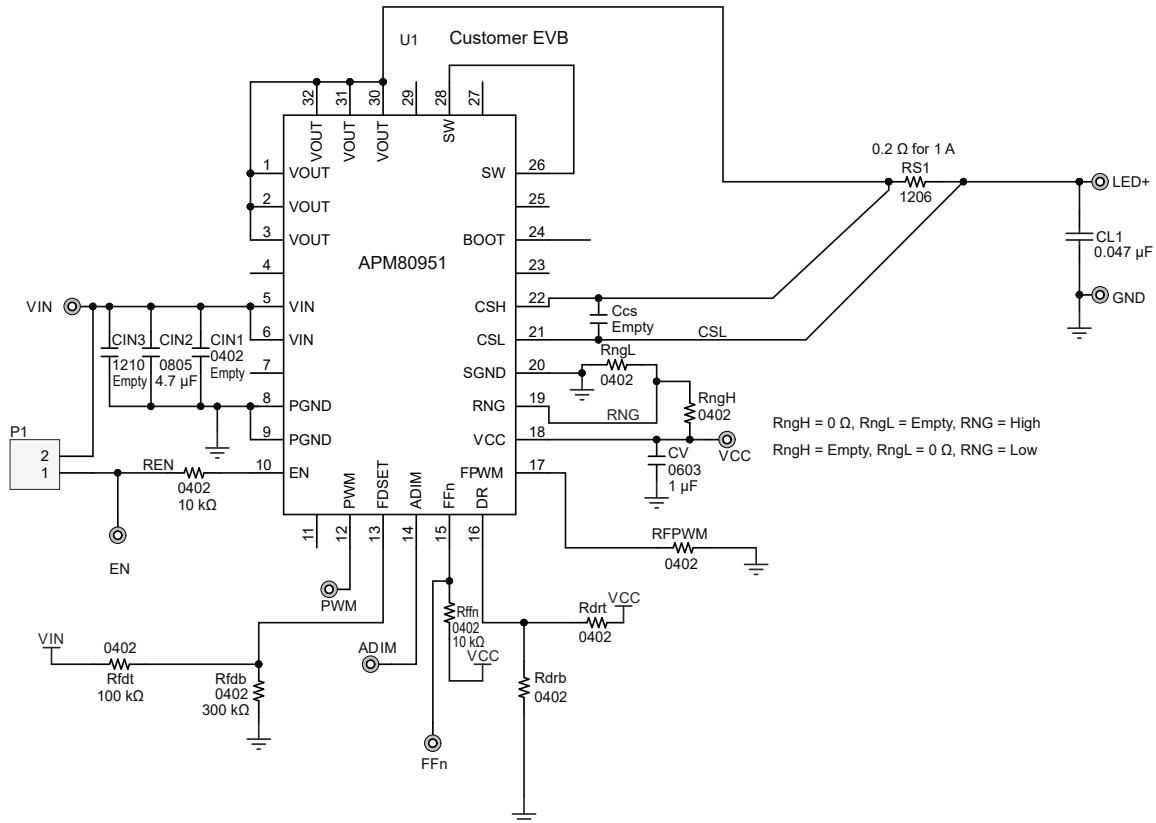


Figure 1: Demo Board Schematic

GENERAL SPECIFICATIONS

Specification	Min	Nom.	Max.	Units
Absolute Maximum Input Voltage	-0.3	-	40	V
Operating Input Voltage Range	4.5	-	36	V
V_{VIN} START Threshold, V_{VIN} rising	-	-	4.3	V
V_{VIN} UVLO Hysteresis	100	-	300	mV
LED Regulation Current	-	-	1.5	A
Enable Input	-0.3	-	$V_{VIN} + 0.3$	V
VCC, ADIM, RNG, FDSET, FFn, PWM, FPWM, DR Terminal Voltages	-0.3	-	7	V

BILL OF MATERIALS

Designator	Description	Footprint	Quantity	Manufacturer	Manufacturer P/N	Source	Purchase P/N
PCB	TED-0003126-PCB (APM80900/04/50/51 PCB)	N/A	1	Allegro MicroSystems		4pcb.com	
U1	APM80951 IC	QFN-32	1	Allegro MicroSystems	APM80951KNBATR		
RS1	Resistor, 0.2 Ω , 1/2 W, 1%	1206	1	Susumu	RL1632R-R200-F	Digikey	RL16R.20FCT-ND
Rfdt	Resistor, 100 k Ω , 1/16 W, 1%	0402	1	Panasonic Electronic	ERA-2AED104X	Digikey	P100KDECT-ND
Rfdb	Resistor, 300 k Ω , 1/16 W, 1%	0402	1	Panasonic Electronic	ERJ-2RKF3003X	Digikey	P300KLCT-ND
RngH	Resistor, 0 k Ω , JUMPER 1/16 W	0402	1	Vishay Dale	CRCW04020000Z0ED	Digikey	541-0.0JCT-ND
REN, Rfn, Rdr, Rdrb	Resistor, 10 k Ω , 1/16 W, 1%	0402	4	Panasonic Electronic	ERA-2AED103X	Digikey	P10KDECT-ND
RFPWM	Resistor, 69.8 k Ω , 1/16 W, 1%	0402	1	Yageo	RT0402BRD0769K8L	Digikey	YAG4300CT-ND
CV	Capacitor, Ceramic, 1.0 μ F, 50 V, 10%, X7R	0603	1	Taiyo Yuden	UMK107AB7105KA-T	Digikey	587-3247-1-ND
CL1	Capacitor, Ceramic, 0.047 μ F, 100 V, X7R 0805	0805	1	Murata TDK	GCM21BR72A473KA37L C2012X7R2A473K125AA	Digikey	490-4969-1-ND 445-2276-1-ND
Cin1, Cin3, CF3, Ccs, RngL	Empty	Various	0				
Cin2	Capacitor, Ceramic, 4.7 μ F, 50 V, X7S	0805	1	Murata	GRM21BC71H475KE11L	Digikey	490-12757-1-ND
FB1	0805 SMT FERRITE BEAD, 120 Ω @ 100 MHz, 3 A	0805	1	Würth Electronics	742792023	Digikey	732-1613-1-ND
D1	DIODE SCHOTTKY 100 V 2 A DO220AA	DO-220AA (SMP)	1	Vishay	SS2PH10HM3/84A	Digikey	SS2PH10HM3/ 84AGITR-ND
Lf	FIXED IND 6.8 μ H 3 A 74 M Ω SMD	4.1 \times 4.1 mm 3.1 mm thick	1	Würth Electronics	74438357068	Digikey	732-11204-1-ND
CF1	Capacitor, Ceramic, 10 nF, 100 V, 10%, X7R	0603	1	TDK	C1608X7R2A103K080AA	Digikey	445-1304-1-ND
CF2	Capacitor, Ceramic, 0.47 μ F, 100 V, X7R	1210	1	TDK	CGA6M3X8R2A474K200AB	Digikey	445-13052-1-ND
Cinf	Capacitor, Ceramic, 4.7 μ F, 100 V, X7R	1210	1	TDK	CGA6M3X7S2A475K200AB	Digikey	445-7005-1-ND
VIN, LED+	Test Points, Red, 0.063" diameter	0.063"	2	Keystone	5010	Digikey	5010K-ND
EN, PWM, ADIM, FFn, VCC	Test Points, White, 0.063" diameter	0.063"	5	Keystone	5012	Digikey	5012K-ND
GND	Test Points, Black, 0.063" diameter	0.063"	4	Keystone	5011	Digikey	5011K-ND
P1	Header, Male, 2 position (open)	0.1" pitch	1	Sullins	PEC02SAAN	Digikey	S1012E-02-ND
PL1, PL2	CONN TERM BLOCK 2 POS 5.08 MM PCB		2	Phoenix Contact	1715721	Digikey	277-1263-ND
Rubber Feet	Self stick rubber feet	Clear	4	3M	SJ-5303 (CLEAR)	Digikey	SJ5303-7-ND

CONFIGURATIONS (Refer to Datasheet)

The customer APM80951 EVB is configured for internal PWM dimming operation mode, so there is no need to apply an external PWM dimming signal at test point PWM when this EVB is used as is. The internal PWM dimming frequency is set at 200 Hz, and the dimming duty cycle is set at about 69%.

To disable internal PWM dimming, replace Rdr1 with 0 Ω resistor to connect DR pin to VCC (refer to schematic above).

Put jumper on P1 connector to connect EN to VIN through a resistor to enable the unit.

RngH or RngL resistors determine the LED current range high or low:

RNG = VCC by making RngH = 0 Ω and RngL = Open	Full rated voltage V_{CSREG} across current sensing resistor $R_{s1} = 200$ mV	$i_{LED} = 0.2 / R_{s1}$
RNG = GND by making RngH = Open and RngL = 0 Ω	Full rated voltage V_{CSREG} across current sensing resistor $R_{s1} = 100$ mV	$i_{LED} = 0.1 / R_{s1}$

- The regulation LED current level is determined by the current sensing resistor on board:

$$i_{LED} = 0.2 / R_{sense} \text{ (A)}$$

On EVB, there is one current sensing resistor, $R_{s1} = 0.2$ Ω. Because RNG = VCC, the full LED current is 1 A.

- The internal PWM dimming frequency is given by the equation below:

$$f_{PWM} = 14000 / R_{FPWM}$$

where R_{FPWM} in kΩ, f_{PWM} in Hz; on EVB, $R_{FPWM} = 69.8$ kΩ sets 200 Hz internal dimming frequency.

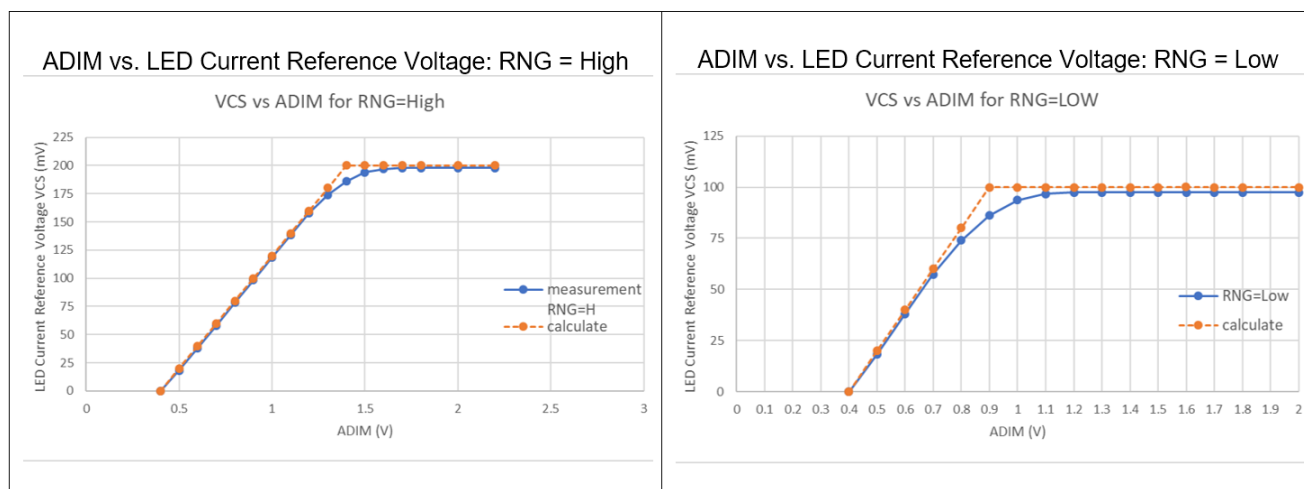
The internal PWM dimming duty cycle can be estimated based on the equation below:

$$D_{PWM} = (V_{DR} / 0.036) \times 100\%$$

- Apply external analog dimming signal at test point ADIM. Do not leave ADIM floating. ADIM pin voltage controls the LED current reference voltage across R_{s1} according to the equation below:

$$V_{CSREG} = (V_{ADIM} - 0.4) / 5 \text{ (V)}$$

The calculation and actual test results are shown below as reference to select the desired ADIM voltage.



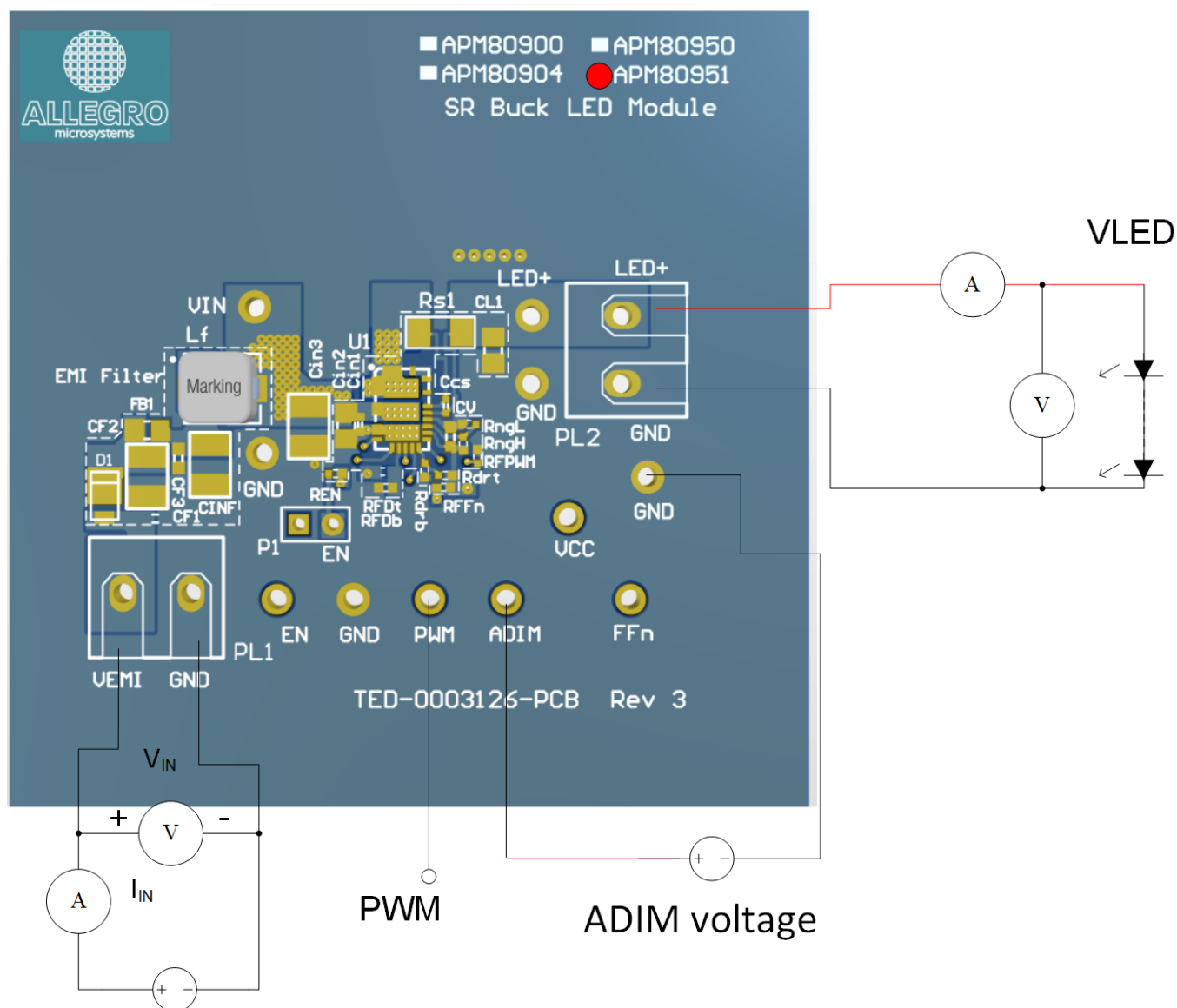
OPERATING INSTRUCTIONS

Refer to figure below for demo board setup.

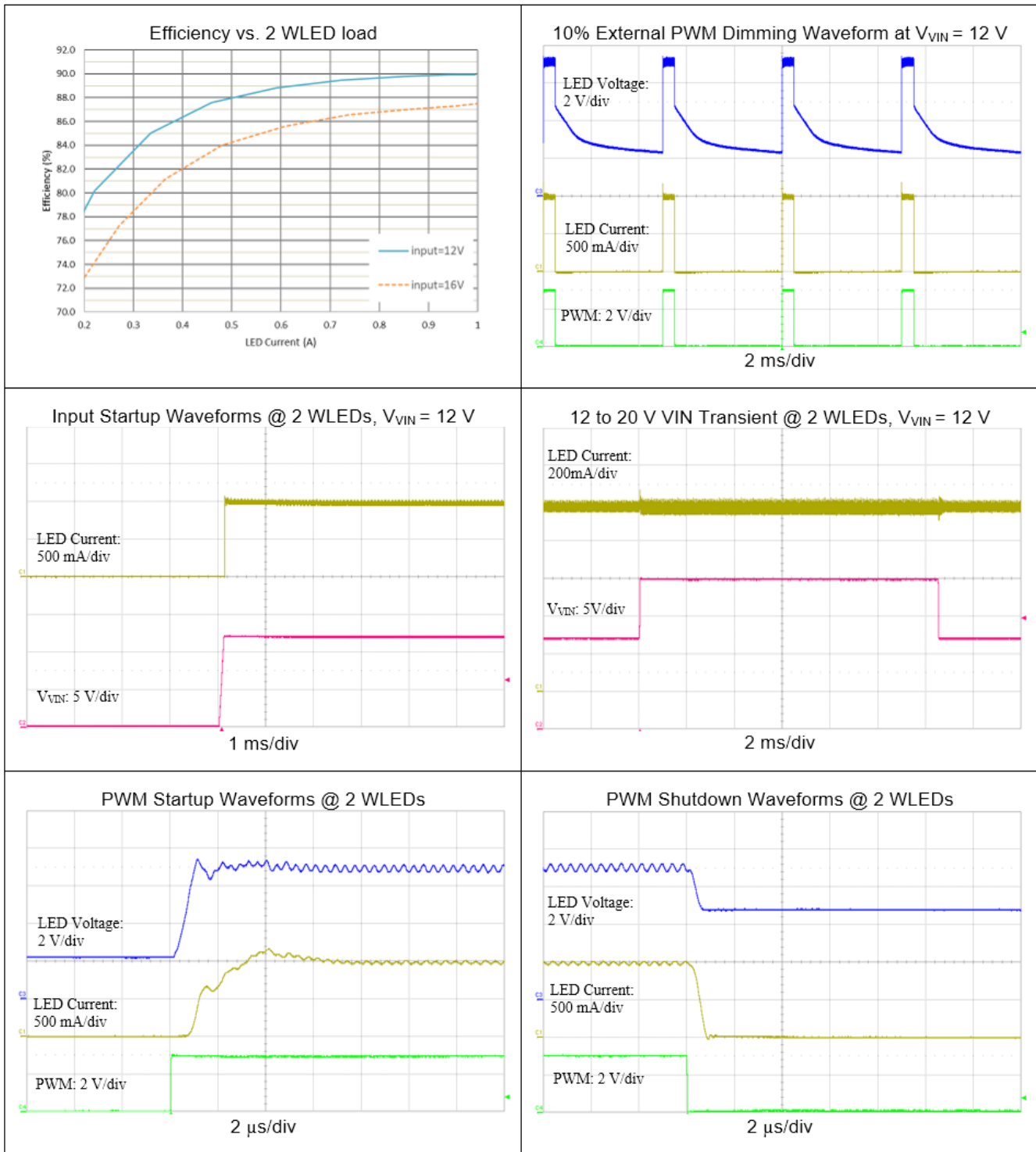
In order to enable the EVB, use the attached jumper to short the connector P1 so that EN is connected to VIN, or apply a voltage level above 1.8 V to the test point EN if the jumper is not used.

Apply the desired ADIM voltage at ADIM test point. For the internal PWM dimming mode, there is no need to apply PWM signal at PWM test point, but for the external PWM dimming mode, PWM signal must be applied at PWM test point.

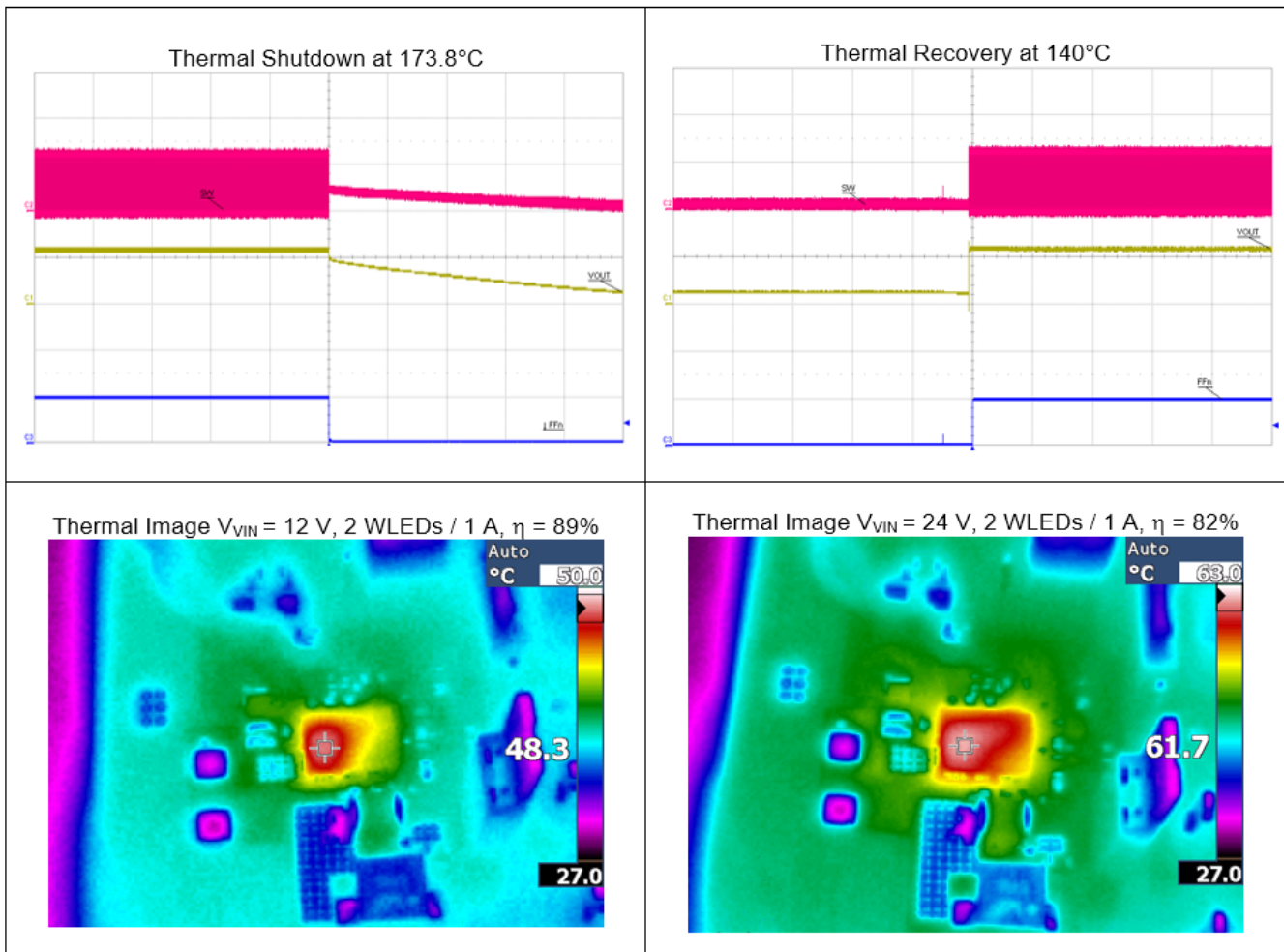
Connect LED load between LED+ to GND; apply input power supply.



DEMO BOARD PERFORMANCE



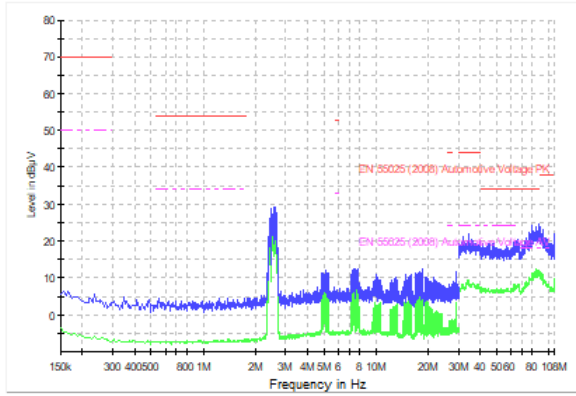
DEMO BOARD PERFORMANCE (continued)



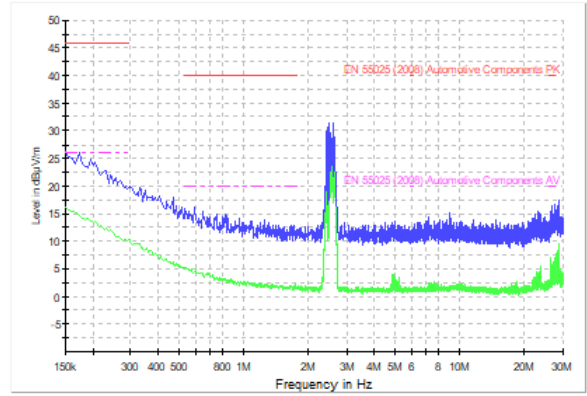
EMI PERFORMANCE

$V_{VIN} = 12\text{ V}$, Load = 2 series white LEDs, $I_{LED} = 0.5\text{ A}$, with EMI filters, as shown in figure below, $T_A = 25^\circ\text{C}$

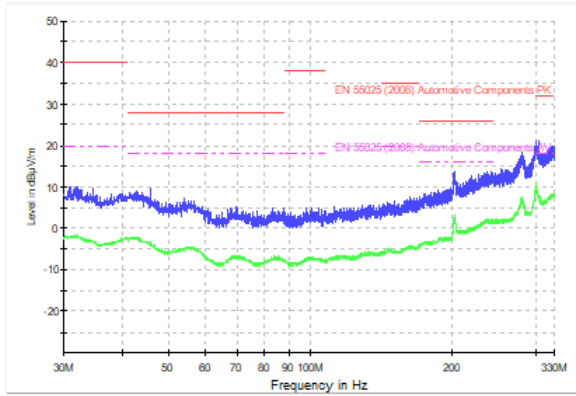
EN55025/CISPR25 Class 5 Peak and Average Conducted Emissions (150 kHz to 108 MHz)



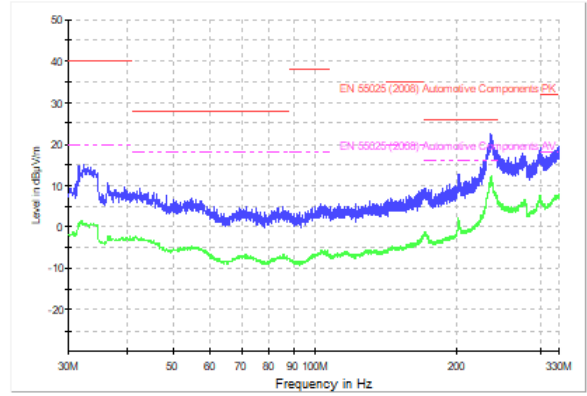
EN55025/CISPR25 Class 5 Peak and Average Rod Antenna Radiated Emissions (150 kHz to 30 MHz)



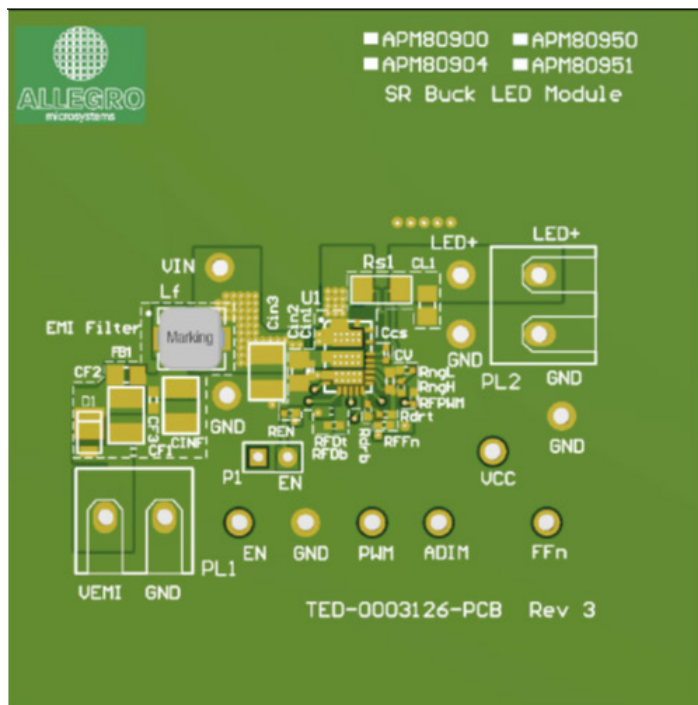
EN55025/CISPR25 Class 5 Peak and Average Biconical Radiated Emissions (Horizontal, 30 to 330 MHz)



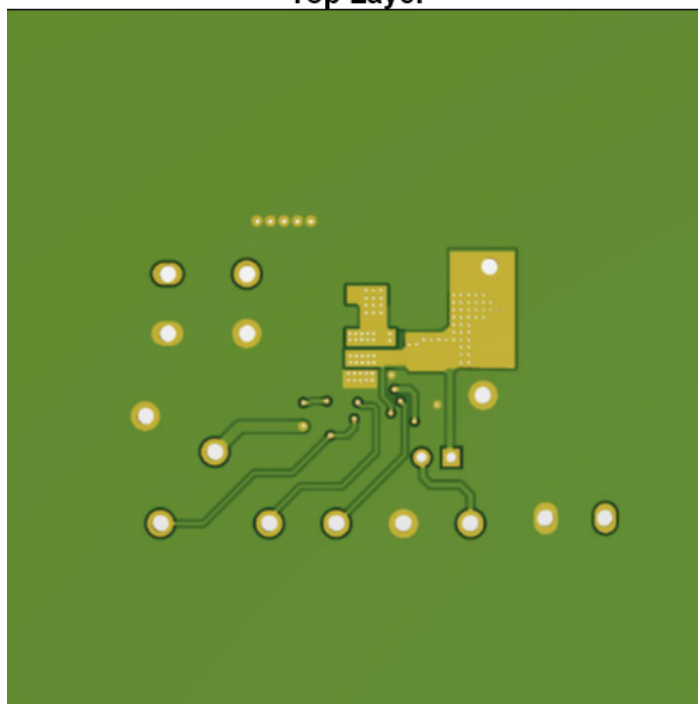
EN55025/CISPR25 Class 5 Peak and Average Biconical Radiated Emissions (Vertical, 30 to 330 MHz)



DEMO PCB LAYOUT



Top Layer



Bottom Layer

Revision History

Number	Date	Description
-	March 12, 2021	Initial Release

Copyright 2020, Allegro MicroSystems.

The information contained in this document does not constitute any representation, warranty, assurance, guaranty, or inducement by Allegro to the customer with respect to the subject matter of this document. The information being provided does not guarantee that a process based on this information will be reliable, or that Allegro has explored all of the possible failure modes. It is the customer's responsibility to do sufficient qualification testing of the final product to ensure that it is reliable and meets all design requirements.

Copies of this document are considered uncontrolled documents.