T-46-35

67C401/13 67C402/23

First-In First-Out (FIFO) 64 x 4, 64 x 5 CMOS MEMORY (Cascadable)

Advanced Micro Devices

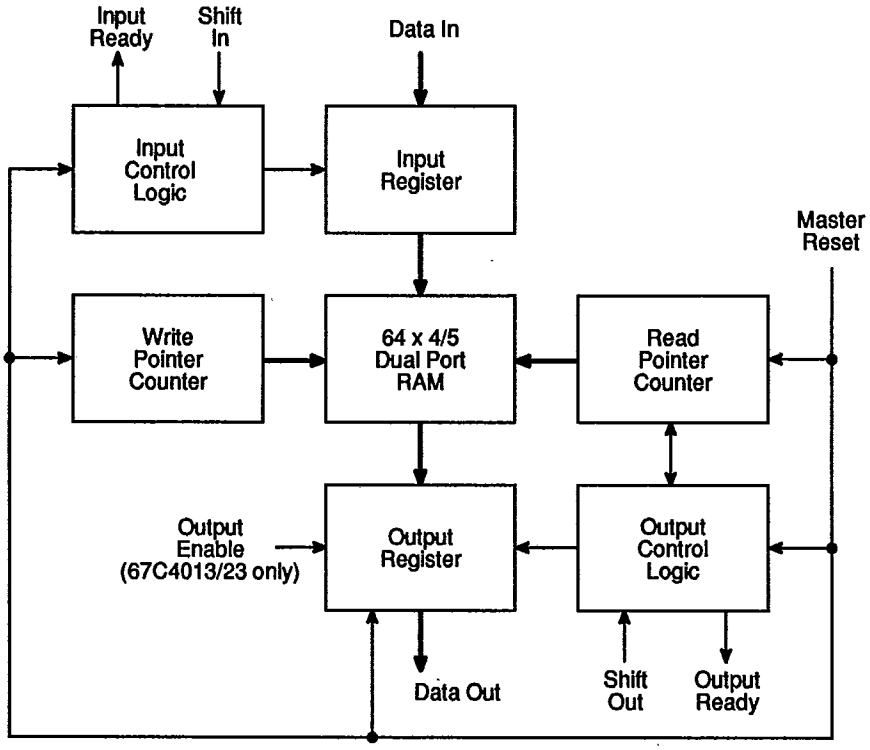
DISTINCTIVE CHARACTERISTICS

- Zero standby power
- High-speed 35-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (67C4013/23)

GENERAL DESCRIPTION

The 67C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 or by 5, bits wide. These devices use Advanced Micro Devices latest CMOS process technology and meet the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disc controllers, graphics, and communication network systems. The 550-µwatt standby power specification makes these devices ideal for ultra-low power and battery-powered systems.

BLOCK DIAGRAM



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CONNECTION DIAGRAMS

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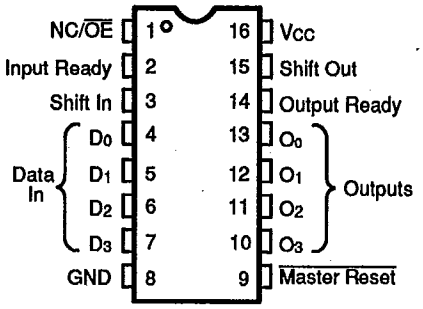
67C401/13



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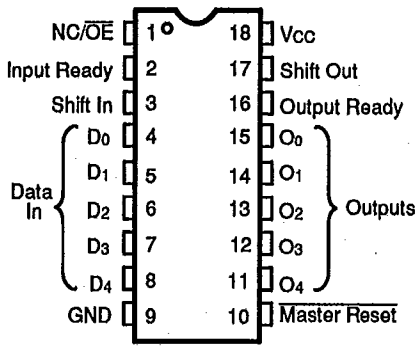

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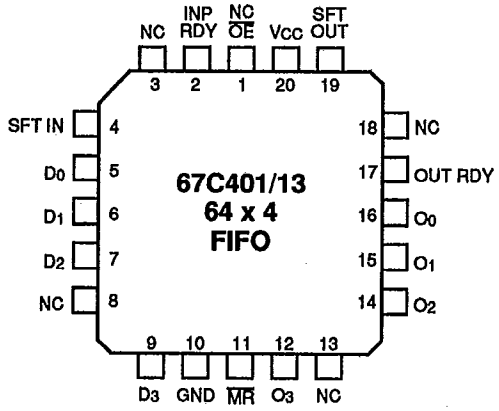
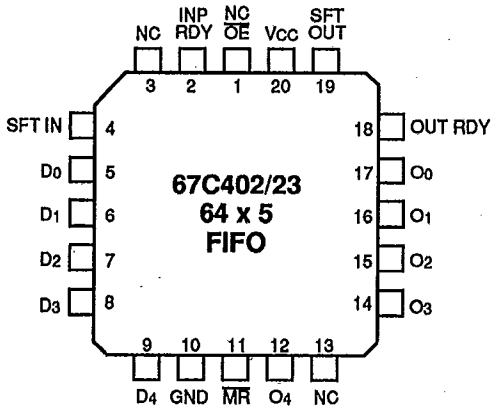


Plastic Leaded Chip Carrier



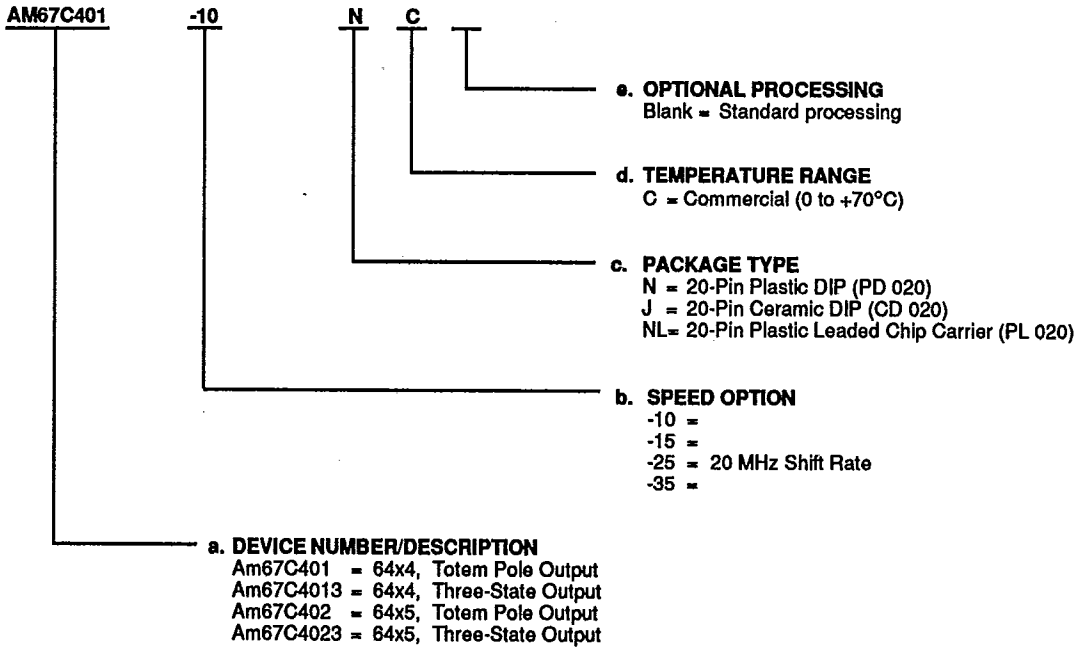
Plastic Leaded Chip Carrier

ORDERING INFORMATION
Standard Products

T-46-35

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM67C401-10	N, J, NL
AM67C401-15	
AM67C4013-10	
AM67C4013-15	
AM67C402-10	
AM67C402-15	
AM67C4023-10	
AM67C4023-15	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc	–0.5 V to +7.0 V
Input Voltage	–1.5 V to +7.0 V
Off-state Output Voltage	–0.5 to Vcc +0.5 V
Storage Temperature	–65°C to +150°C
Power Dissipation	1.0 W

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the device at these limits or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

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Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) With Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

OPERATING CONDITIONS Commercial: V_{CC} = 5 V ±10%, T_A = 0°C to +70°C

Parameter Symbol	Parameter Description	Figure	-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
f_{IN}	Shift in rate	1		10		15		25		35	MHz
t_{SIH}*	Shift in HIGH time	1	14		14		8		8		ns
t_{SIL}*	Shift in LOW time	1	25		25		8		8		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		0		0		0		ns
t_{IDH}	Input data hold time from SI (Shift In)	1	40		40		20		15		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		0		5		2		ns
t_{RIDH}	Input data hold time from IR (Input Ready)	3	30		30		20		15		ns
f_{OUT}	Shift out rate	4		10		15		25		35	MHz
t_{SOH}*	Shift out HIGH time	4	24		21		8		8		ns
t_{SOL}*	Shift out LOW time	4	25		25		8		8		ns
t_{MRW}	Master Reset pulse	8	35		35		25		18		ns
t_{MRS}	Master Reset to SI	8	65		65		10		7		ns

*See AC test and high-speed application note.

DC CHARACTERISTICS over operating ranges unless otherwise specified

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Parameter Symbol	Parameter Description	Test Condition		-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
V_{IL}*	Low-level input voltage				0.8		0.8		0.8		0.8	V
V_{IH}*	High-level input voltage			2		2		2		2		V
I_{IN}	Input Current	V_{CC} = Max., GND < V_{IN} < V_{CC}		–1	1	–1	1	–1	1	–1	1	µA
I_{OZ}	Off-state output current	V_{CC} = Max., GND < V_{OUT} < V_{CC}		–5	5	–5	5	–5	5	–5	5	µA
V_{OL}	Low-level output voltage	V_{CC} = Min.	I_{OL} = 20 µA		0.1		0.1		0.1		0.1	V
			I_{OL} = 8 mA		0.4		0.4		0.4		0.4	
V_{OH}	High-level output voltage	V_{CC} = Min.	I_{OH} = –20 µA	V_{CC} – 0.1		V_{CC} – 0.1		V_{CC} – 0.1		V_{CC} – 0.1		V
			I_{OH} = –4 mA	2.4		2.4		2.4		2.4		
I_{OS}**	Output short-circuit current	V_{CC} = Max.	V_O = 0 V	–90	–20	–90	–20	–90	–20	–90	–20	mA
I_{CC}	Standby supply current	V_{CC} = Max. I_{OUT} = 0	V_{IH} = V_{CC} V_{IL} = GND		100		100		100		100	µA
	Operating supply current		V_{IH} = Min., V_{IL} = Max. f_{IN} = f_{OUT} = Max.		35		45		50		60	mA

*These are absolute voltages with respect to GND and include all overshoots due to system and/or tester noise.
**Not more than one output should be shortened at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Figure	-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
t_{IRL}*	Shift in ↑ to Input Ready Low	1		60		55		21		18	ns
t_{IRH}*	Shift in ↓ to Input Ready HIGH			50		50		28		20	ns
t_{ORL}*	Shift Out ↑ to Output Ready LOW	4		55		45		19		18	ns
t_{ORH}*	Shift Out ↓ to Output Ready HIGH			50		41		34		20	ns
t_{ODH}	Output Data Hold (previous word)		5		5		5		5		ns
t_{ODS}	Output Data Shift (next word)			35		30		34		20	ns
t_{PT}	Data throughput	3,6		100		90		40		34	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		100		100		35		28	ns
t_{MRIRH}	Master Reset ↓ to Input Ready HIGH			100		100		35		28	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			35		35		25		22	ns
t_{IPH}	Input Ready pulse HIGH	3	19		16		8		8		ns
t_{OPH}	Output Ready pulse HIGH	6	14		14		8		8		ns
t_{ORD}	Output Ready ↑ to Data Valid	4		–3		–3		0		0	ns
t_{PHZ}**	Output Disable Delay	A		25		25		15		12	ns
t_{PLZ}**				25		25		15		12	
t_{PZL}**	Output Enable Delay			30		30		20		15	ns
t_{PZH}**				30		30		20		15	

*See AC test and high-speed application note.
**Enable/Disable delays refer to 67C4013/23 only.

CAPACITANCES*

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Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5 V		10	pF
C_{OUT}	Output capacitance			7	

*Not tested in production.

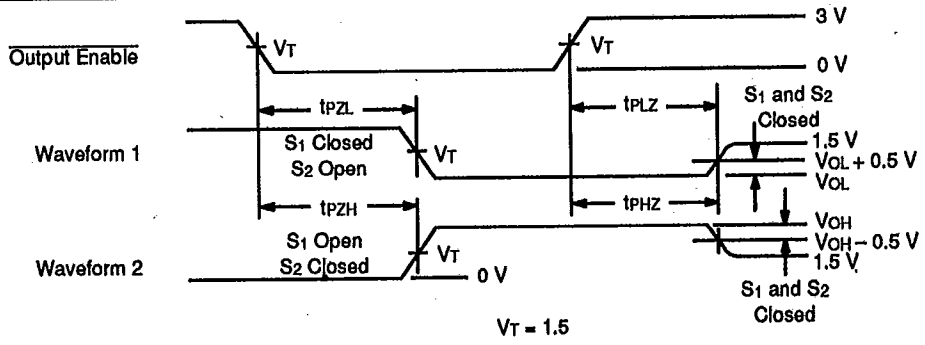
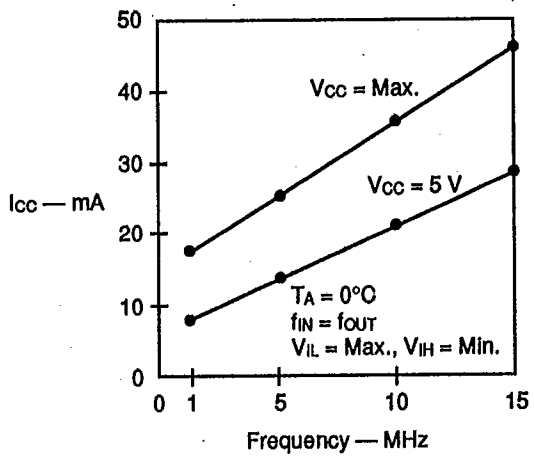


Figure A. Enable and Disable

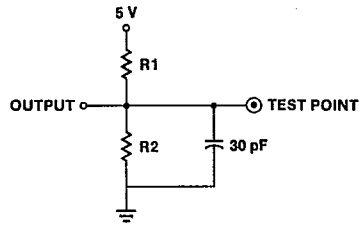
Notes:

1. Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

ICC vs. Frequency



STANDARD AC TEST LOAD



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

RESISTOR VALUES

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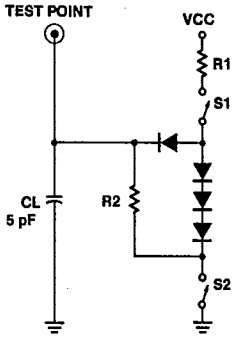
I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

THREE-STATE TEST LOAD



FUNCTIONAL DESCRIPTION

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_X inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

Data Output

Data is read from the O_X outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Advanced Micro Devices recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., a rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not HIGH due to (a) too high a frequency, or (b) FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem also relates to t_{IRH}, t_{ORL}, and t_{ORH}. For high-speed applications, proper grounding technique is essential. In order to diminish timing ambiguities between the Shift-In-Input-Ready or Shift-Out-Output-Ready pairs when operating at high frequencies, it is recommended that the t_{SIH} and t_{SOH} pulse widths be as short as possible within the specified limits.

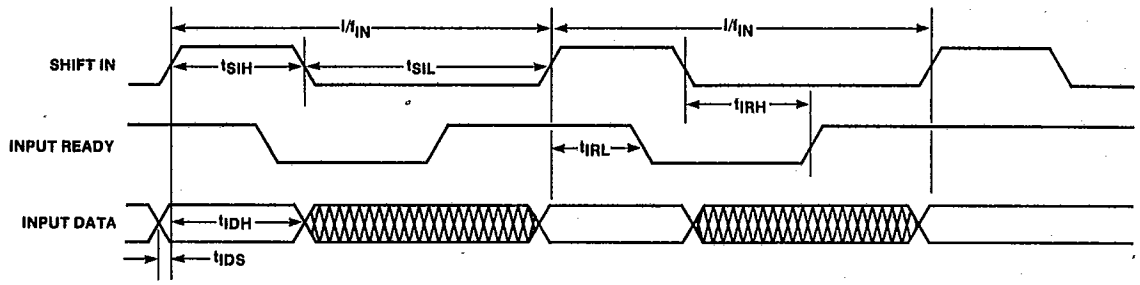


Figure 1. Input Timing

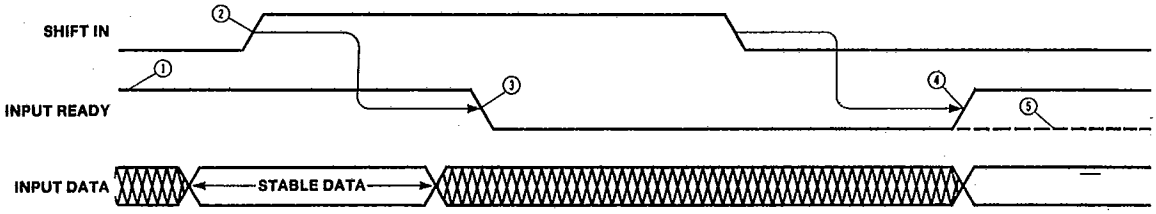


Figure 2. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first available memory location.
③ Input Ready goes LOW indicating this memory location is full.
④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
⑤ If the FIFO is already full then the Input Ready remains LOW.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

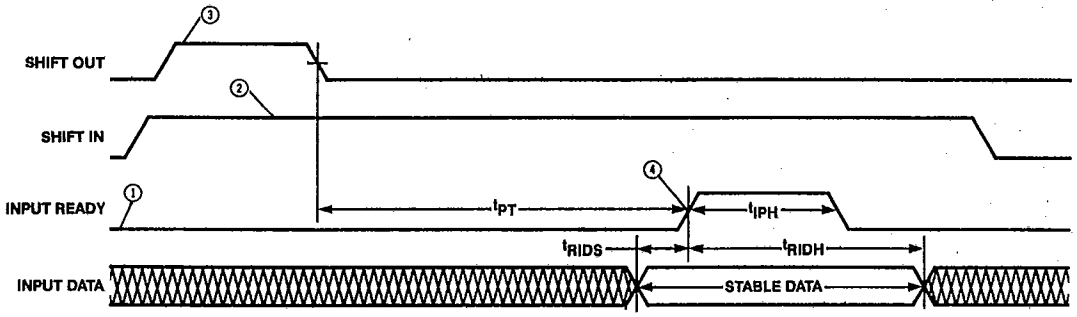


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.
② Shift In is held HIGH.
③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

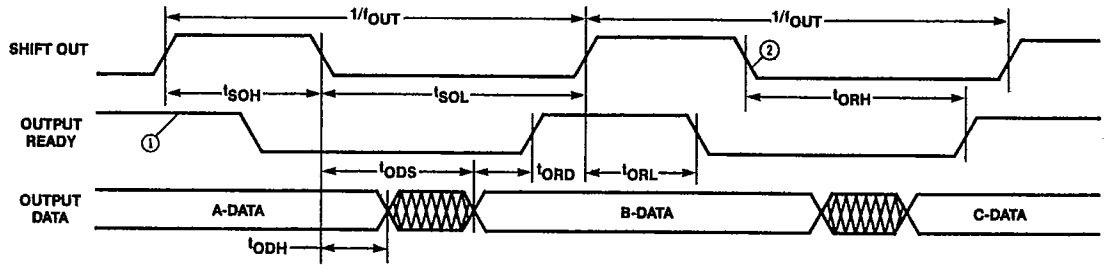


Figure 4. Output Timing

① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

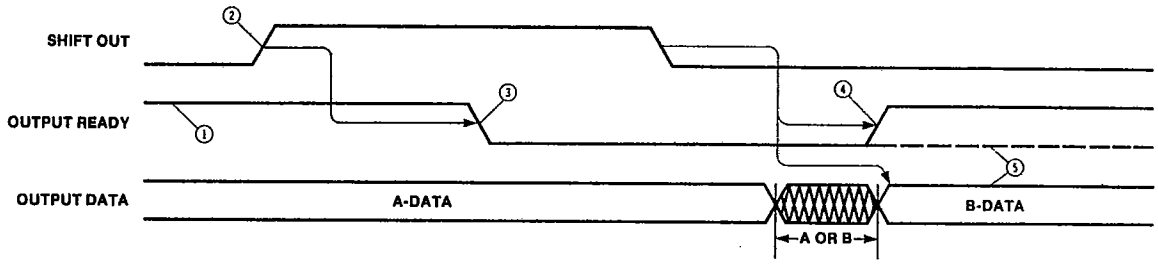


Figure 5. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

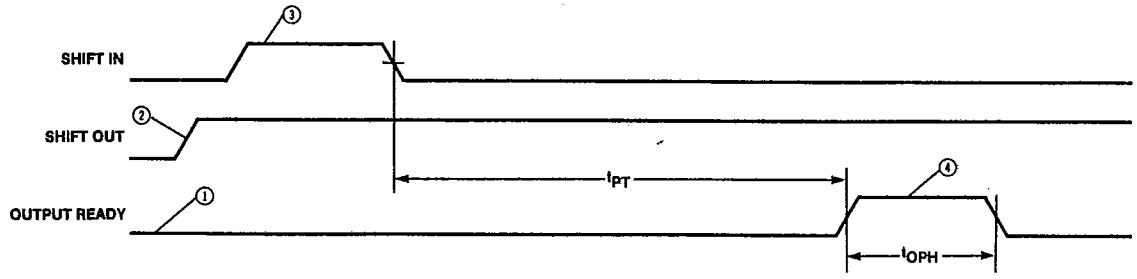


Figure 6. t_{PT} and t_{OPH} Specification

① FIFO initially empty.
② Shift-Out held HIGH.
③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
④ As soon as Output Ready becomes HIGH, the word is shifted out.

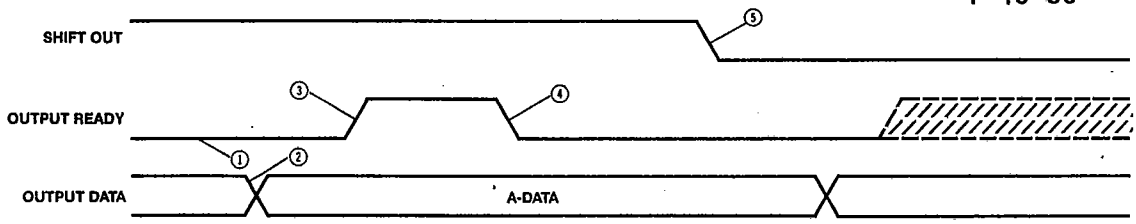
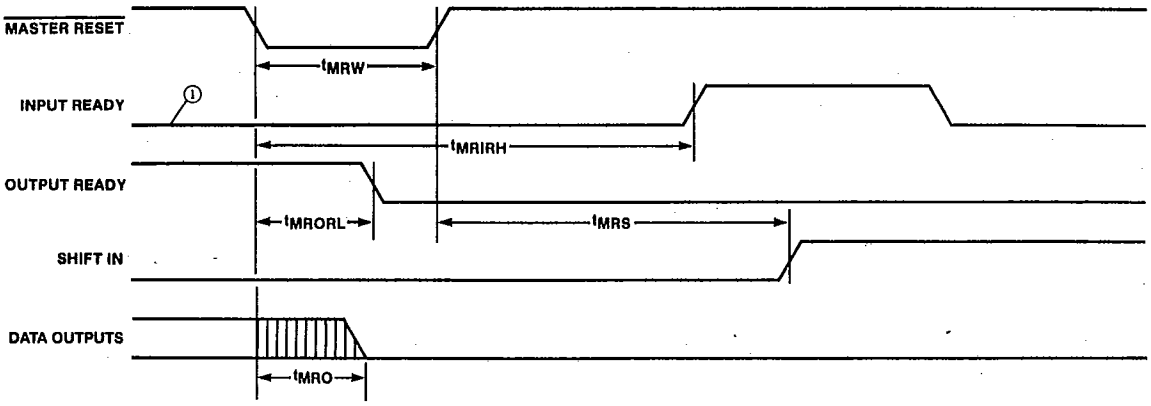


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① The internal logic does not detect the presence of any words in the FIFO.
② New data (A) arrives at the outputs.
③ Output Ready goes HIGH indicating arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional words in the FIFO.



① FIFO is initially full.

Figure 8. Master Reset Timing

NORMALIZED I_{CC} vs FREQUENCY