FAIRCHILD SEMICONDUCTOR™

PRELIMINARY

August 1999

NM24C65U
64K-Bit Serial EEPROM with Write Protect 2-Wire Bus Interface

General Description:

The NM24C65U is a 64K (65,536) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the **Extended** I²C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

NM24C65U incorporates a hardware "Write Protect" feature, by which the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed as long as WP pin is connected to V_{CC}.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

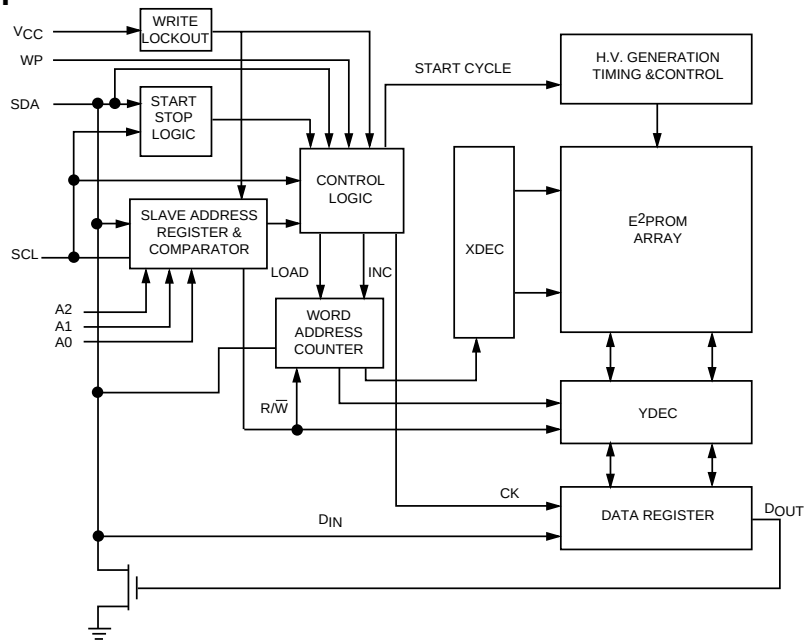
Functions

- I²C™ compatible interface
- 65,536 bits organized as 8,192 x 8
- 100 KHz or 400 KHz operation
- Extended 2.7V – 5.5V operating voltage
- Self timed programming cycle (6ms typical)
- "Programming complete" indicated by ACK polling
- Memory "Upper Block" Write Protect pin

Features

- The I²C™ interface allows the smallest I/O pincount of any EEPROM interface
- 32 byte page write mode to minimize total write time per byte
- Low V_{CC} programming lockout (3.8V)
  — **"H" option (Standard V_{CC} range) parts only**
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram



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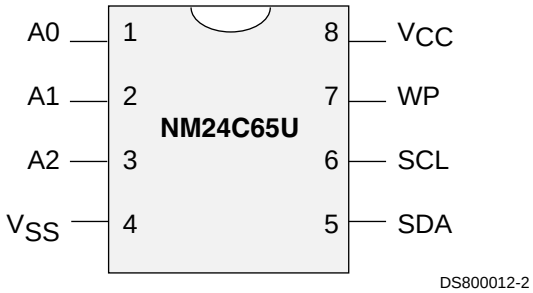
I²C™ is a registered trademark of Philips Electronics N.V.

Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



Top View
See Package Number N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

NM 24 C XX U F LZ E XX

	Letter	Description
Package	N	8-Pin DIP
	M8	8-Pin SOIC
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
	H	4.5V to 5.5V and V_{CC} Lockout
SCL Clock Frequency	Blank	100KHz
	F	400KHz
	Ultralite	CS100UL Process
Density	65	64K with Write Protect
	C	CMOS
Interface	24	IIC
	NM	**Fairchild Non-Volatile Memory**

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C65U	0°C to +70°C
NM24C65UE	-40°C to +85°C
NM24C65UV	-40°C to +125°C
Positive Power Supply	
NM24C65U/NM24C65UH	4.5V to 5.5V
NM24C65UL	2.7V to 5.5V
NM24C65ULZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 kHz f_{SCL} = 100 kHz		0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz f_{SCL} = 100 KHz			0.2	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}	V_{CC} = 2.7V - 4.5V V_{CC} = 2.7V - 4.5V V_{CC} = 4.5V - 5.5V		1 0.1 10	10 1 50	µA µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			0.1	1	µA
V_{IL}	Input Low Voltage			–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA				0.4	V

Capacitance T_A = +25°C, f = 100/400 KHz, V_{CC} = 5V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

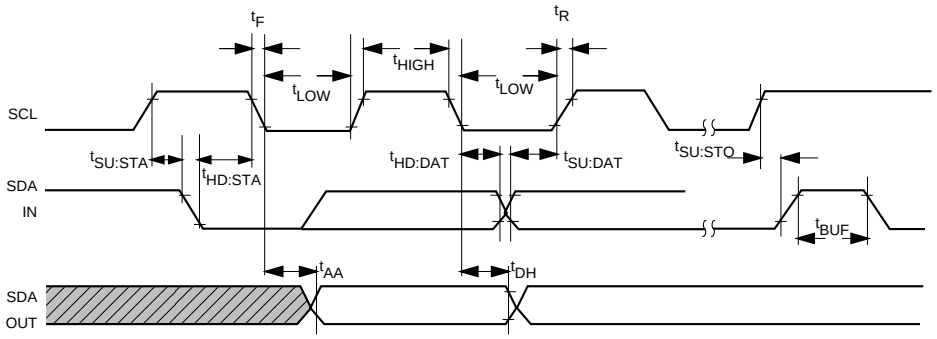
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C65U - NM24C65UL, NM24C65ULZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C65U bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

Bus Timing



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BACKGROUND INFORMATION (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or slave address, must follow the START condition. For EEPROMs, the first 4-bits of the slave address is '1010'. This is then followed by the device selection bits A2, A1 and A0.The final bit in the slave address determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The slave address is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 4M bits in the Extended IIC protocol. EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

	Definitions
Word	8 bits (byte) of data
Page	32 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any IIC device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMS are always considered Slaves).
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave).
Receiver	Device currently RECEIVING data on the bus (Master or Slave).

Pin Description

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a biderectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the upper half of the memory will not be executed. READ operations are always available.

If WP is tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire bit memory array.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C65Uxxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C65Uxxx is considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and reserved for indicating start and stop conditions. *Refer to Figures 2 and 3.*

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C65Uxxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C65Uxxx to place the device in the standby power mode.

Write Cycle Timing

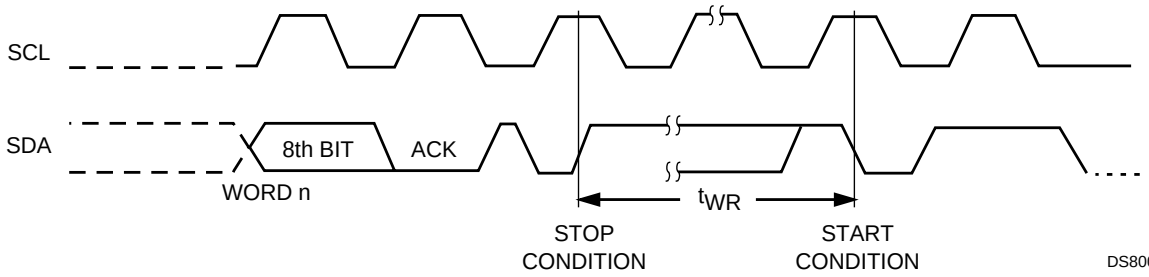
ACKNOWLEDGE

Acknowledge is a hardware convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4*.

The NM24C65Uxxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the NM24C65Uxxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the READ mode the NM24C65Uxxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing (Figure 1)



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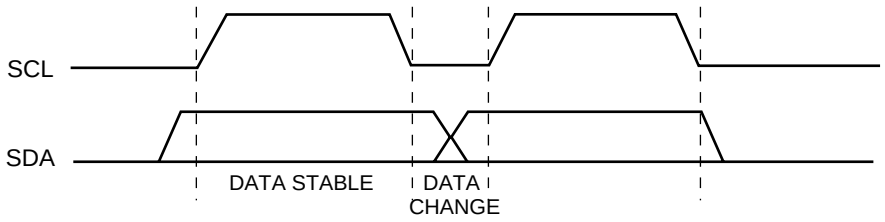
Data Validity (Figure 2)



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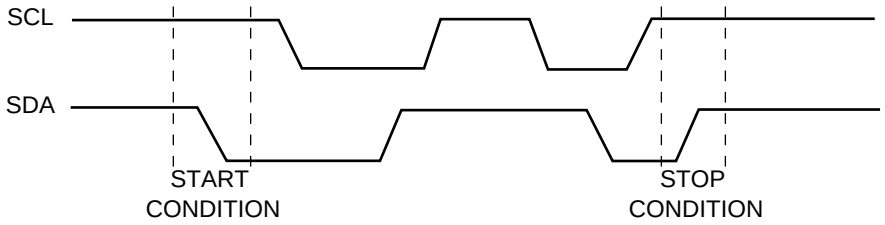
Definition of Start and Stop (Figure 3)



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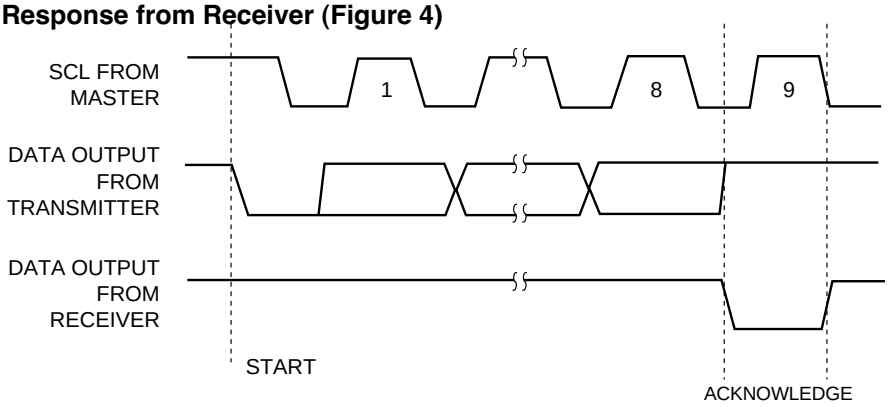
Acknowledge Response from Receiver (Figure 4)



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DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all EEPROM devices.

The next three bits identifies the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the IIC bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the NM24C65Uxxx recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address bytes, with 13 active bits, are required after the SLAVE acknowledge to address the full memory array. The first byte indicates the high-order byte of the word address. Only the five least signicant bits can be changed, the other bits are pre-assigned the value "0". Following the acknowledgement from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the NM24C65Uxxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C65Uxxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer *Figure 5* for the Byte Write sequence.

PAGE WRITE

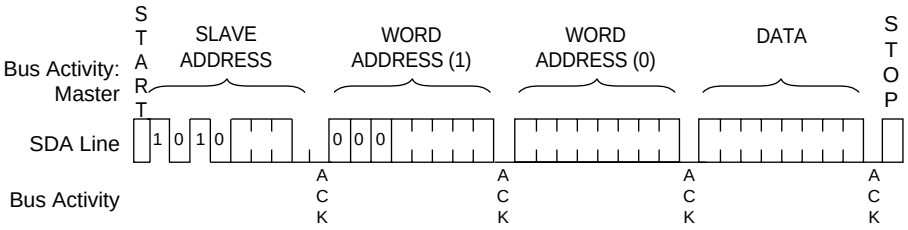
The NM24C65Uxxx is capable of thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transfered, the master can transmit up to thirty-one more words. After the receipt of each word, the device responds with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer *Figure 6* for the Page Write sequence.

Acknowledge Polling

Once the stop condition is isssued to indicate the end of the host's write operation, the NM24C65Uxxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C65Uxxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Byte Write (Figure 5)



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Write Protection

Programming of the upper half of memory will not take place if the WP pin is connected to V_{CC}. The device will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24C65Uxxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Low V_{CC} Lockout

NM24C65UxHx (H option) protects against data corruption during programming by preventing any programming operations if V_{CC} drops below approximately 3.8V (V_{CC} Lockout trip level). This is accomplished by monitoring the "READ/WRITE" (R/$\overline{W}$) bit in the SLAVE address and if the R/$\overline{W}$ bit is "0," indicating a programming operation, the V_{CC} Lockout is activated. At that point, if the V_{CC} drops below the trip level, programming is inhibited and the device does not issue an ACK (the output stays high). To restate, the V_{CC} Lockout feature is active from the time a WRITE bit is received up to the time that the Master's STOP condition is received (the STOP condition turns on the V_{PP} internal high voltage). **Once programming has begun, the programming cycle cannot be interrupted except by removal of V_{CC}, which could result in data corruption.**

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C65Uxxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C65Uxxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge acknowledge the transfer but does generate a stop condition, and therefore discontinues transmission. Refer *Figure 7* for the Current Address Read sequence.

RANDOM READ

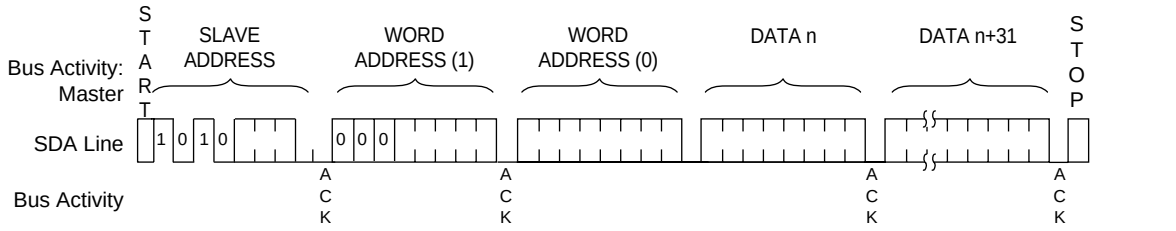
Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address with the R/$\overline{W}$ bit set to "0" and then the word address it is to read from. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to "1". This will be followed by an acknowledge from the NM24C65Uxxx and then by the eight bit data. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C65Uxxx discontinues transmission. Refer *Figure 8* for the Random Read sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C65Uxxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n, followed by the data n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C65Uxxx continues to output data for each acknowledge received. Refer *Figure 9* for the Sequential Read sequence.

Page Write (Figure 6)



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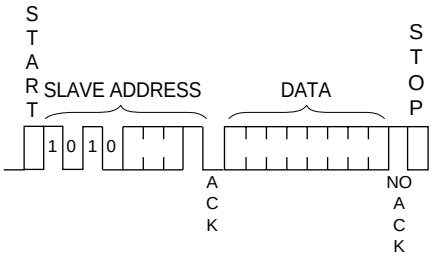
Current Address Read (Figure 7)



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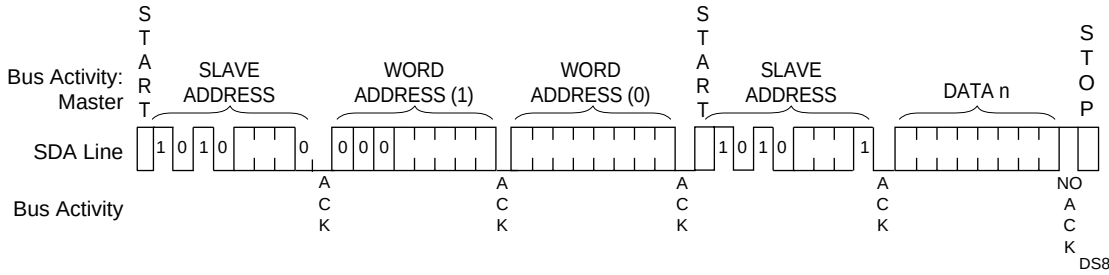
Random Read (Figure 8)



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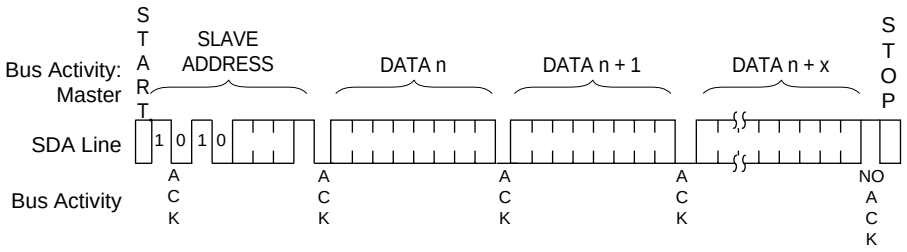
Sequential Read (Figure 9)



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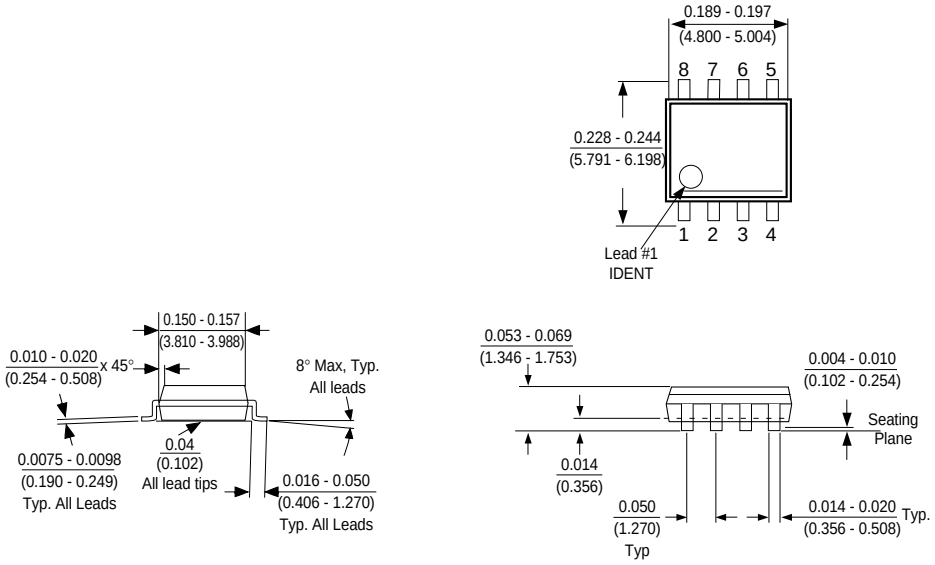
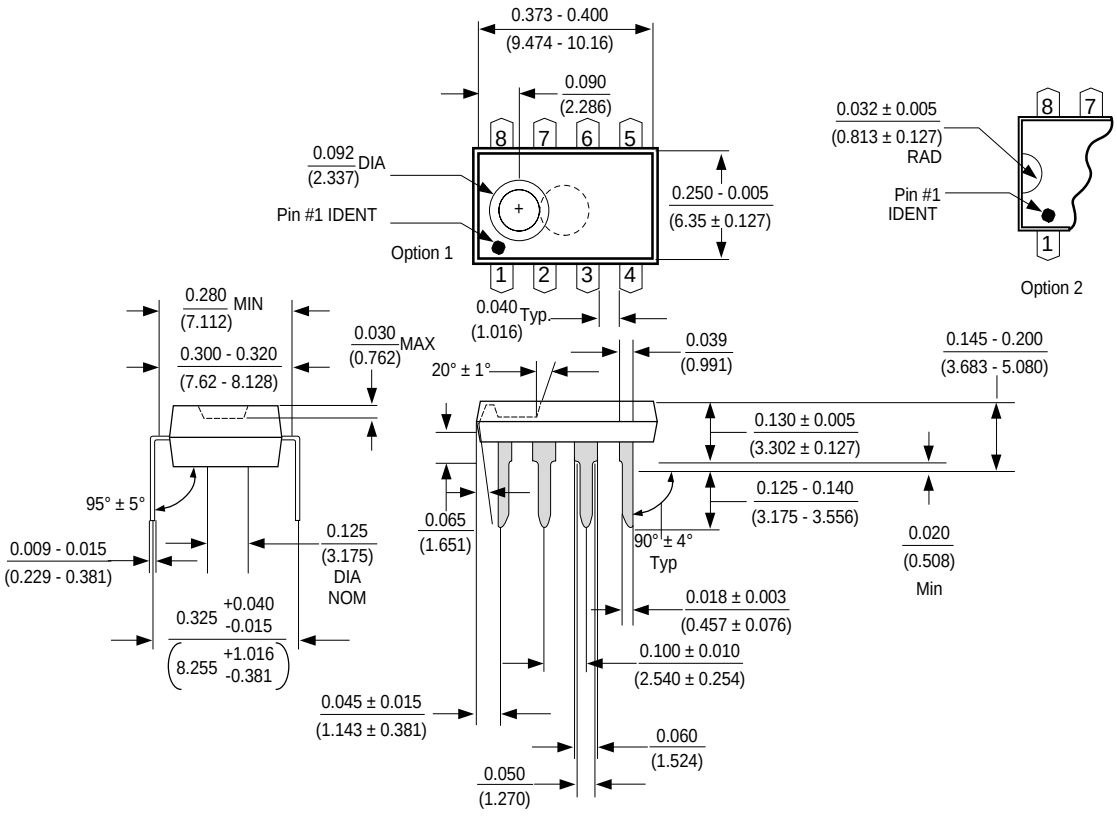
Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM24C65UxxxM8 or NM24C65UxxxEM8
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number NM24C65UxxxN or NM24C65UxxxEN
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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NM24C65U
Product information

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General description

The NM24C65U is a 64K (65,536) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the **Extended** I^2C™ 2-wire protocol which uses Clock (SCL) and Data I/O (SDA) pins to synchronously clock data between the "master" (for example a microprocessor) and the "slave" (the EEPROM device). In addition, the serial interface allows a minimal pin count, packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

Because this device incorporates a hardware "Write Protect" feature, the upper half of the memory can be disabled against programming by connecting the WP pin to V_{CC}. This section of memory then effectively becomes a ROM (Read-Only Memory) and can no longer be programmed.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption for a continuously reliable non-volatile solution for all markets.

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Features

- The I^2C™ interface allows the smallest I/O pincount of any EEPROM interface
- 32 byte page write mode to minimize total write time per byte
- Low V_{CC} programming lockout (3.8V)
  - **"H" option (Standard V_{CC} range) parts only**
- Typical 200µA active current (I_{CCA})
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

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Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Package marking	Packing method
NM24C65UFM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 F	TAPE REEL
NM24C65UN	Not recommended for new designs	$1.26	DIP	8	$Y&Z&2&T 24U65 N	RAIL
NM24C65ULZN	Not recommended for new designs	N/A	DIP	8	$Y&Z&2&T 24U65 LZ	RAIL
NM24C65ULM8	Not recommended for new designs	$1.29	SOIC	8	$Y&Z&2&T 24U65 L	RAIL
NM24C65UFLM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 FLM8	TAPE REEL
NM24C65UEM8	Not recommended for new designs	$1.29	SOIC	8	$Y&Z&2&T 24U65 EM8	RAIL
NM24C65UFLZEM8X	Not recommended for new designs	$1.33	SOIC	8	$Y&Z&2&T 24U65 FLZE	TAPE REEL
NM24C65ULEN	Not recommended for new designs	N/A	DIP	8	$Y&Z&2&T 24U65 LE	RAIL
NM24C65UEN	Not recommended for new designs	$1.29	DIP	8	$Y&Z&2&T 24U65 EN	RAIL

NM24C65UM8X	Not recommended for new designs	$1.26	SOIC	8	$Y&Z&2&T 24U65 M8	TAPE REEL
NM24C65UFLEM8	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 FLE	RAIL
NM24C65UVM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 V	TAPE REEL
NM24C65UM8	Not recommended for new designs	$1.26	SOIC	8	$Y&Z&2&T 24U65 M8	RAIL
NM24C65UFLZEM8	Not recommended for new designs	$1.33	SOIC	8	$Y&Z&2&T 24U65 FLZE	RAIL
NM24C65UFLZM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 FLZ	TAPE REEL
NM24C65ULM8X	Not recommended for new designs	$1.29	SOIC	8	$Y&Z&2&T 24U65 L	TAPE REEL
NM24C65ULZEM8	Not recommended for new designs	$1.33	SOIC	8	$Y&Z&2&T 24U65 LZE	RAIL
NM24C65UFLZM8	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 FLZ	RAIL
NM24C65UFLEM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 FLE	TAPE REEL
NM24C65UEM8X	Not recommended for new designs	$1.29	SOIC	8	$Y&Z&2&T 24U65 E	TAPE REEL
NM24C65ULEM8	Not recommended for new designs	$1.31	SOIC	8	$Y&Z&2&T 24U65 LE	RAIL
NM24C65ULN	Not recommended for new designs	$1.29	DIP	8	$Y&Z&2&T 24U65 L	RAIL
NM24C65UVM8	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 V	RAIL
NM24C65UDWF	Not recommended for new designs	N/A	Wafer	N/A	N/A	RAIL
NM24C65UFLM8	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 FL	RAIL

NM24C65UFM8	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 F	RAIL
NM24C65ULZM8	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 LZ	RAIL
NM24C65ULZM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 LZ	TAPE REEL
NM24C65ULEM8X	Not recommended for new designs	N/A	SOIC	8	$Y&Z&2&T 24U65 LE	TAPE REEL
NM24C65ULZEM8X	Not recommended for new designs	$1.33	SOIC	8	$Y&Z&2&T 24U65 LZE	TAPE REEL

* 1,000 piece Budgetary Pricing

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