ADSP-3128A

FEATURES

128×16 or 64×32 Register File Organization
Flexible "Crossbar" Data Routing via Five Ports
- **Two Input**
- **Two Output**
- **One Bidirectional**

Cascadable Horizontally and Vertically
Supports 20MHz Operation from Single 1×Clock
- **18ns Clock-to-Valid Output (Registered)**
- **35ns Address-to-Valid Output (Transparent)**

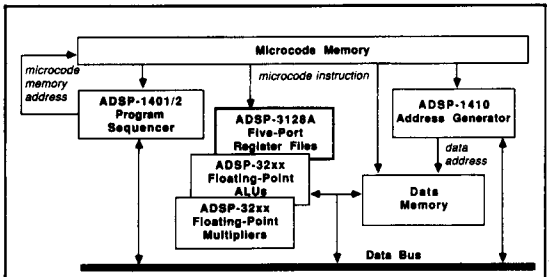
Flexible Latching Modes at Address and Data Ports:
- **Transparent, Latched, Registered**

Prioritized Write Ports
Write Inhibit Control on Each Write Port
Automatically Pipelined Bank Select and Port Select
Register-to-Register Transfers
Three-State Outputs
Fully Static Operation
145-Pin Grid Array

APPLICATIONS

High Speed Temporary Data Storage in
- **Digital Signal Processing**
- **Numeric ProcessingGraphics**

Floating-Point and Fixed-Point



Word-Slice® Floating-Point Microcoded System with ADSP-3128A Multiport Register Files

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GENERAL DESCRIPTION

The ADSP-3128A Multiport Register File is a versatile data storage component that can greatly expand the computational bandwidth of a fast-arithmetic processor. (See Figure 1 for the ADSP-3128A's Functional Block Diagram.) The ADSP-3128A also simplifies processor design by permitting flexible data routing through its five 16-bit data ports: two input ports, two output ports and a bidirectional port. This register file complements the floating-point and fixed-point multipliers and ALUs available from Analog Devices. Because of its flexibility, however, it has application in a broad range of processor designs. The ADSP-3128A is a higher speed, pin-compatible upgrade from the ADSP-3128.

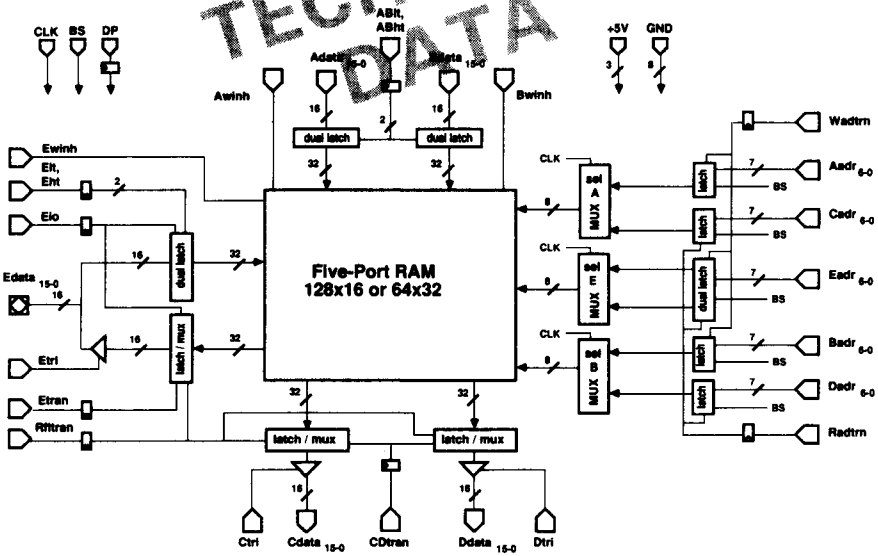

Figure 1. ADSP-3128A Multiport Register File Functional Block Diagram

The ADSP-3128A is configurable via a control pin as either a 128×16 register file or a 64×32 register file. In the Single-Precision 128×16 configuration, the ADSP-3128A is best suited for fixed-point and single-precision (32-bit) floating-point data storage. For single-precision floating-point, two register files should be used "horizontally" yielding 128 words of 32-bit storage. The 64×32 Double-Precision configuration is intended for double-precision (64-bit) floating-point, again with two register files in a horizontal architecture. In this Double-Precision mode, the register files will each transfer 16-bits in each phase of the clock, 32-bits of data per port in a one-cycle write or read operation. Microcode need only be applied to the register file at the system's 1×clock rate.

To accommodate critical system timing requirements, the ADSP-3128A offers a variety of latching modes on both data and address ports. The prioritized write data ports have control lines that define the input data latching mode for Single-Precision as (a) latched on clock HI, (b) transparent or (c) registered on the clock's falling edge. However loaded, data can also be held at the input latches for subsequent cycles.

In *Single-Precision mode*, the Multiport Register File's five ports allow five 16-bit data transfer operations per cycle. The input and output latches transfer data to and from the ADSP-3128A's RAM using 16-bit internal buses. The bidirectional Edata-Port can be directly controlled to either write or read. Normal operation allows up to three 16-bit writes in clock HI and three 16-bit reads in clock LO per cycle. Register-to-register transfers are made via the bidirectional Edata-Port (which can be accomplished in two sequential clock phases by following a read with a write). See the Applications Note, "Register-to-Register Transfers with the ADSP-3128A."

In *Double-Precision mode*, the Multiport Register File's five ports allow five 32-bit data transfer operations per cycle for a total bandwidth of 160 bits per cycle. The input and output latches transfer data to and from the RAM via 32-bit internal buses. The input data latching modes allow either an early input or a late input mode. With early input, the Y_Word (Y_W) is presented to the input data latches in clock HI and the X_Word (X_W) in clock LO. With late input, the Y_Word is presented to the input latches in clock LO and the X_Word in clock HI of the next cycle. For data transfers with a slower system bus, the Edata-Port allows both input and output values to be transferred more slowly than the ADSP-3128A's clock rate (Edata Slow Input and Edata Slow Read). Register-to-register transfers are made via the bidirectional Edata-Port.

Each *write data* port of the ADSP-3128A has an independent write-inhibit control that disables the write operation that normally occurs during clock HI. Write-inhibit allows cancelling a write based on an external condition.

The *read data* ports have control lines that define the output data latching mode for Single-Precision as (a) registered on the clock's rising edge or (b) transparent. In Double-Precision mode, the output data latching modes allow either an early read or a late read. With early read, the Y_Word can be output in clock LO and the X_Word in clock HI of the next cycle. With late read, the Y_Word can be output in clock HI and the X_Word in clock LO of the same cycle. Each read data port has an independent tristate control that allows putting that output port into a high impedance state.

The 7-bit write address latches corresponding to the write ports can be mutually defined to latch addresses in one of two ways. Either (a) write addresses are latched to the address latches on clock HI, or (b) the address latches are transparent. The 7-bit *read address* latches can be mutually defined to latch addresses in one of two different ways. Either (a) read addresses are registered to the address latches on the clock's rising edge, or (b) the address latches are transparent. In Double-Precision mode, there are half as many words that are twice as wide. For Double-Precision addressing, the (unneeded) highest order address bits function as Port Select lines. Port Select (the most significant address bit) enables or disables individual ports consistent with their pipelines.

Bank Select enables or disables an entire ADSP-3128A consistent with all read and write pipelines. Bank Select and Port Select allow the user to expand register file storage "vertically" for more than 128 single-precision or 64 double-precision data words.

The ADSP-3128A is fabricated in double-metal 1.0μm CMOS. Each chip consumes significantly less power than comparable bipolar solutions.

The ADSP-3128A is available for both commercial and extended temperature ranges. Extended temperature range parts are available processed fully to MIL-STD-883, Class B. The ADSP-3128A is packaged in a ceramic 145-lead pin grid array.

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ADSP-3128A MULTIPORT REGISTER FILE PIN LIST (POSITIVE TRUE LOGIC CONVENTION)

Pin Name	Description
DATA PORTS	
$Adata_{15-0}$	Write Adata-Port Input Data
$Bdata_{15-0}$	Write Bdata-Port Input Data
$Cdata_{15-0}$	Read Cdata-Port Output Data
$Ddata_{15-0}$	Read Ddata-Port Output Data
$Edata_{15-0}$	Bidirectional Edata-Port Input and Output Data
ADDRESS PORTS	
$Aadr_{6-0}$	Address Port for Adata-Port Writes
$Badr_{6-0}$	Address Port for Bdata-Port Writes
$Cadr_{6-0}$	Address Port for Cdata-Port Reads
$Dadr_{6-0}$	Address Port for Ddata-Port Reads
$Eadr_{6-0}$	Address Port for Edata-Port Writes and Reads and for Register-to-Register Transfers
GENERAL CONTROLS	
BS	Bank Select (registered or asynchronous, depending on address port Latches)
DP	Double-Precision Mode (registered)
ADDRESS LATCH CONTROLS	
Wadtrn	Write Address Latch Transparent (registered)
Radtrn	Read Address Latch Transparent (registered)
DATA INPUT AND WRITE CONTROLS	
ABlt, ABht	Input Latch Controls for Both Adata-Port and Bdata-Port (registered)
Elt, Eht	Input Latch Controls for Edata-Port (registered)
Awinh	Inhibit Write to RAM from Adata-Port Input Latches (asynchronous)
Bwinh	Inhibit Write to RAM from Bdata-Port Input Latches (asynchronous)
Ewinh	Inhibit Write to RAM from Edata-Port Input Latches (asynchronous)
DATA READ AND OUTPUT CONTROLS	
CDtran	Output Latch Controls (Make Transparent) for Both Cdata-Port and Ddata-Port (registered)
Etran	Output Latch Controls (Make Transparent) for Edata-Port (registered)
Rfltran	Clock-On-Rising/Falling Select for Slow Inputs in Double-Precision Mode (registered)
Eio	Edata-Port Slow Read Control in Double-Precision Mode (registered)
Ctri	Cdata-Port Three-State Control (asynchronous)
Dtri	Ddata-Port Three-State Control (asynchronous)
Etri	Edata-Port Three-State Control (asynchronous)
MISCELLANEOUS	
CLK	Clock
GND	Ground (Eight Lines)
V_{DD}	+5V Power Supply (Three Lines)

FUNCTIONAL DESCRIPTION

The ADSP-3128A Multiport Register File consists of a high speed static RAM (configurable as either 128×16 or 64×32) surrounded by the latches and control logic needed for simple system interfacing (see Figure 1). Six internal data paths, all 32-bits wide, connect this RAM with multiplexers (muxes) and latches. Three are read data paths; three are write data paths. Three 7-bit internal address paths connect this RAM with muxes and address latches. These three address paths are internally time-multiplexed to allow the presentation of six addresses to the RAM per cycle.

Three addresses are presented to RAM in clock HI from the Aadr, Badr and Eadr address latches. These are RAM write addresses. They are prioritized in case of conflict. Three addresses are presented to RAM in clock LO from the Cadr, Dadr and Eadr address latches. These are RAM read addresses. Three simultaneous reads, even from the same RAM location, are possible for clock LO reads. The Eadr–Port feeds both a write (clock HI) address latch and a read (clock LO) address latch, which can be independently set to latched or transparent modes.

Writes to the RAM occur in clock HI when Awinh and/or Bwinh and/or Ewinh are LO. Note that data writen in clock HI is available to be read in the same clock cycle.

The DP control determines whether the Register File is in Double-Precision mode (HI) or Single-Precision mode (LO). In Single-Precision mode, all data paths between RAM and data latches behave as if they were 16 bits. The data latches also behave like 16-bit latches. The register file is organized 128×16 in Single-Precision mode, and each location is addressed with seven bits. DP can be changed dynamically, consistent with the constraints imposed in the timing diagrams (Figures 4 through 13).

In Double-Precision mode, the Register File is organized 64×32, and each location is addressed with six bits. In Double-Precision mode, all data paths between RAM and data latches are 32 bits, as are the data latches. Writes (32-bit) to the RAM occur in clock HI and reads (32 bit) from the RAM occur in clock LO. Multiplexers between the latches and the 16-bit data ports alternately select Y_Word and X_Word. Note that when ADSP-3128A Register Files are configured in horizontal pairs for Double-Precision operation, the Y_Words from the pair will make up half the external 64-bit double-precision word and the X_Words the other half. See Figures 14 and 15.

In Single-Precision mode, the input latches can be configured to latch input data at clock HI, register input data on the falling clock edge, be made transparent, or hold the most recent data. The output latches can be configured to register data from the RAM on the rising clock edge or to be transparent clock LO and latched clock HI. The bidirectional Edata-Port can be configured to do either one read or one write each cycle. Each read port has an independent three-state enable control.

In Double-Precision mode, the input latches can be configured for an early input, a late input, a slow input on the Edata-Port (for transfers from slow devices), or a hold of the most recent data on the A&Bdata-Ports. Early and late inputs are distinguished by a one-half clock cycle difference between when the Y_Word and X_Word are written to the input latches. The output latches can be configured for an early read, a late read or a slow read on the Edata-Port (for transfers to slow devices). Early and late reads are distinguished by a one-half clock cycle difference between when the Y_Word and X_Word are read from the output latches. To accomplish late inputs and early reads, the latches are transparent for 16 bits of the data transfer, allowing either a direct write of the X_Word to RAM or a direct read of the Y_Word from RAM, respectively.

The write address latches can be made transparent or latched in clock HI. The read address latches can be made transparent or registered with the clock's rising edge. In Double-Precision mode, the unused high-order address bit is interpreted as Port Select. Port Select and Bank Select (BS) are treated as part of the address field so that their write-disable and three-state effects properly track the selected pipeline delays.

CONTROLS

The ADSP-3128A Register File has 18 control lines. Their functional descriptions are summarized in mode Tables I through III.

Most control lines are registered, as indicated in the "Pin List" and in Figure 1. All registered controls meet the timing requirements of Figure 2. The timing requirements for the three asynchronous three-state controls, Ctri, Dtri and Etri, are shown in Figure 3. The timing for the remaining asynchronous controls are illustrated in timing diagrams Figures 2 through 13.

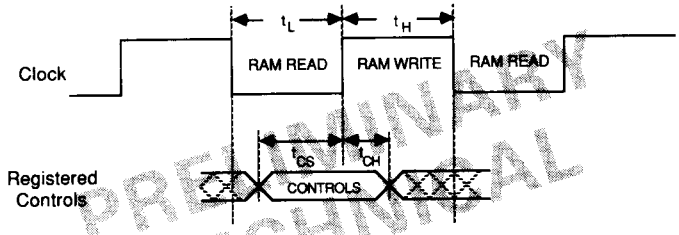


Figure 2. ADSP-3128A Registered Controls Timing

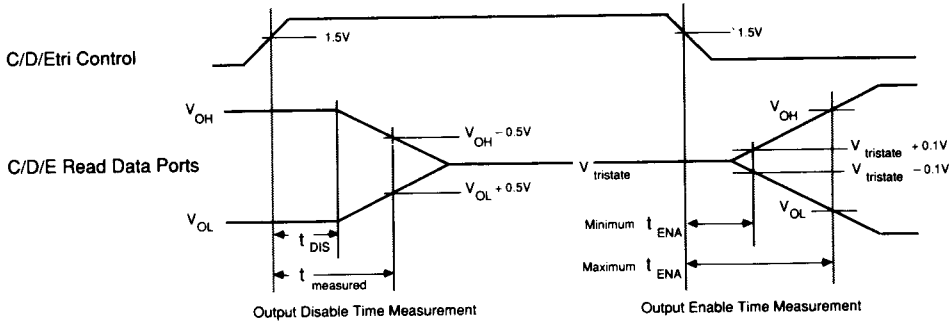


Figure 3. ADSP-3128A Three-State Disable and Enable Timing

BS	DP	AB&Elt	AB&Eht	A&B&Einh	Rfltran	Description
0	X	X	X	X	X	Disable chip (consistent with pipelines) but advance pipelines with clock cycle
1	0	0	0	X	X	Register write data at A&B or Edata input latches on falling edge
1	0	0	1	X	X	Hold most recent data at A&B or Edata input latches for the next cycle
1	0	1	0	X	X	Latch write data at A&B or Edata input latches at clock HI
1	0	1	1	X	X	Make transparent A&B or Edata input latches
1	X	X	X	0	X	Allow write to RAM from the A, B and Edata input latches
1	X	X	X	1	X	Inhibit write to RAM from the A, B and Edata input latches
1	1	0	0	X	X	Early Input to A&B or Edata input latches: register Y_W on falling edge to input latches and latch X_W to input latches in clock HI
1	1	0	1	X	X	Late Input to A&B or Edata input latches: latch Y_W to input latches in clock HI and make input latches transparent for X_W in clock HI
1	1	1	X	X	X	Hold most recent data at A&B input latches for the next cycle
1	1	1	1 → 0	X	0	Edata Slow Input: register Y_W to Edata input latch on next falling edge (Eht only)
1	1	1	0 → 1	X	0	Edata Slow Input: register X_W to Edata input latch on next falling edge (Eht only)
1	1	1 → 0	1	X	1	Edata Slow Input: register Y_W to Edata input latch on next rising edge (Elt only)
1	1	0 → 1	1	X	1	Edata Slow Input: register X_W to Edata input latch on next rising edge (Elt only)

Table I. ADSP-3128A Summary of Data Input and Write Control Modes

BS	DP	CD&Etran	Rfltran	C&D&Etri	Eio	Description
0	X	X	X	X	X	Disable chip (consistent with pipelines) but advance pipelines with clock cycle
1	X	X	X	0	X	Drive data from output latches through C or D or Edata-Port
1	X	X	X	1	X	Three-state (high impedance) output C or D or Edata-Port
1	0	0	X	X	X	Register data from RAM to C&D or Edata output latches on rising edge
1	0	1	0	X	X	C&D or Edata output latches are transparent clock LO, latched clock HI
1	0	X	X	X	0	Edata-Port is configured for one read or one write per cycle
1	1	0	0	X	0	Configured for Late Read at C&D or Edata-Port: register Y_W & X_W from RAM to output latches on rising edge; output Y_W in clock HI, output X_W on next clock LO
1	1	1	0	X	0	Configured for Early Read at C&D or Edata-Port: output Y_W from RAM through transparent output latches in clock LO; latch X_W to output latches and output in clock HI
1	1	0	0	X	1	Configured for Edata Slow Read: hold RAM read data at Edata output latch; output Y_W at clock HI
1	1	1	0	X	1	Configured for Edata Slow Read: hold RAM read data at Edata Output Latch; output X_W at clock HI
1	1	X	1	X	X	Defines Clock-On-Rising/Falling mode for Edata Slow Inputs

Table II. ADSP-3128A Summary of Data Read and Output Control Modes

BS	DP	Wadtrn	Radtrn	A/B/C/D/Eadr$_6$ (Port Select)	Description
0	X	X	X	X	Disable chip (consistent with pipelines) but advance pipelines with clock cycle
1	X	0	X	X	Latch A or B or Eadr write addresses at clock HI
1	X	1	X	X	A or B or Eadr write address latches are transparent
1	X	X	0	X	Register C or D or Eadr read address latches on the rising edge
1	X	X	1	X	C or D or Eadr read address latches are transparent
X	1	X	X	0	Disable A/B/C/D/Edata-Port
1	1	X	X	1	Enable A/B/C/D/Edata-Port

Table III. ADSP-3128A Summary of Address Control Modes

ADDRESS LATCHES FOR BOTH SINGLE- AND DOUBLE-PRECISION MODES

The three read (clock HI) address latches and three write (clock LO) address latches hold the seven bits required for Register File addressing, Port Select and Bank Select. Radtrn controls whether the three read address latches are transparent or latched; Wadtrn controls whether the three write address latches are transparent or latched. When Radtrn/Wadtrn is HI, addresses presented at the read/write address ports are transferred directly to the RAM with no pipeline delay. When Radtrn is LO, addresses presented at the read address ports are registered on the rising edge of the clock, to be used during the next clock LO. When Wadtrn is LO, addresses presented at the write address ports are latched on the rising edge of the clock, to be used immediately during the next clock HI.

Both Radtrn and Wadtrn latch controls are registered and affect the configuration of the address latches on the rising clock edge in which they are registered. They remain in effect until the next rising edge.

Transparent addresses must be valid at least t_{AST} before the end of the phase in which they are used. The setup time for latched or registered addresses is t_{ASR}. All addresses must be held valid t_{AH} after the end of the phase in which they are asserted.

Output delays for transparent data reads from transparent addresses are referenced from address valid. However, an address valid prior to the clock LO in which the RAM is read provides no additional benefit. The output delay, t_{ODTT}, is referenced from address valid or the clock falling edge – whichever is *later*. The transparent read address must be held valid throughout the RAM read phase.

SINGLE-PRECISION OPERATION

Single-Precision mode is determined by the registered DP control being LO. Single-Precision mode must be asserted as shown in the timing diagrams to insure that the high-order single-precision address bits are *not* misinterpreted as Double-Precision Port Select bits and that latch controls are given their proper Single-Precision interpretation. A general discussion of dynamic switching between Single- and Double-Precision modes can be found below in "DP/SP Changeover." In Single-Precision mode, the Register File is configured as 128 words that are 16 bits in width. The 128 words are addressed by 7-bit addresses from the five address ports. All data paths and data latches behave as if they were 16 bits wide.

Up to five 16-bit data transfers per cycle are possible in Single-Precision mode. These transfers can be comprised of three writes and two reads, or two writes and three reads.

SP Reads

The operations of transferring data from RAM to a latch and from a latch to the output pins are logically distinct with the ADSP-3128A. Transfers from RAM to latch are called "reads" in this data sheet; transfers from latch to output port are called "outputs."

Read addresses can be transparent or registered (Figure 4). In all timing diagrams, the phase in which an address causes a RAM *read or write* is indicated by a Greek letter. For Figure 4's reads, all addresses shown cause a read in phase α. Not all controls are shown on this or other timing diagrams as explicit waveforms. In Figure 4, for example, the expression "Radtrn = 1" at a rising edge implies that Radtrn was asserted HI before that edge and met the standard setup and hold time requirements of Figure 2 for controls.

The output latches can be set transparent via registered controls CDtran HI and/or Etran HI. Note that one control, CDtran, affects both Cdata-Port and Ddata-Port output latches. From a transparent read address (Radtrn HI), read data when the output latches are transparent will be valid t_{ODTT} after a valid read address or after the clock falling edge – whichever is *later*. From a transparent read address, read data will be valid t_{ODC} after the rising clock edge when the output latches are in registered mode from the C&Ddata-Ports and/or the Edata-Port.

When the read addresses are registered (Radtrn LO), the data output timing is very similar except that the output delay for a transparent read is now referenced from a clock edge rather than address valid. The transparent read data will be valid t_{ODRT} after the falling clock edge.

Note that in all four combinations of address and output latching modes, the read from RAM took place in phase α. Specifying registered output latches simply introduces an additional clock phase of pipelining. Note also that for all Single-Precision reads, the data out is held valid throughout the phase *after* the data became valid. In the case of transparent data reads, the latch is actually holding the data valid for this phase. Data will be held valid t_{ODH} after the clock edge for all reads (in all modes).

Each read port has its own asynchronous three-state control: Ctri, Dtri and Etri. See Figure 3 for enable and disable timing.

SP Writes

Single-Precision mode must be asserted as shown in Figure 5 to insure that the high-order single-precision address bits are *not* misinterpreted as Double-Precision Port Select bits and that latch controls are given their proper Single-Precision interpretation. The operations of transferring data from a port to a latch and from a latch to the RAM are logically distinct with the ADSP-3128A. Transfers from port to latch are called "inputs" in this data sheet; transfers from latch to RAM are called "writes."

Write addresses can be transparent (Wadtrn HI) or registered (Wadtrn LO), exactly as with read addresses (Figure 5).

The Adata-Port and Bdata-Port input latches can be set to transparent, latched or clock-on-falling mode via the ABlt and ABht controls (Table I and Figure 5). The Edata-Port input latch can be set to transparent, latched or clock-on-falling mode via the Elt and Eht controls. When the "lt" and "ht" controls are both asserted HI, the latches are transparent ("t"). When only "lt" is asserted, the latches are in latched mode ("l"). When only "ht" is asserted the latches are in hold mode ("h"). When both controls are LO, the latches are in clock-on-falling mode.

Note that one set of controls, ABlt and ABht, affects both Adata-Port and Bdata-Port input latches. (These controls also permit holding the most recent write data at the input latches. See "SP Input to Input Latches and Hold" below.) These controls are always registered on the rising edge and become effective as of the next falling edge. When the input latches are transparent, write data must be valid t_{DST} before the end of the write phase. When the input latches are in latched mode, write data must be valid t_{DSR} before the beginning of the write phase. When the input latches are in clock-on-falling mode, write data must be valid t_{DSN} before the falling clock edge prior to the write phase. In all cases, the write data presented at write data ports must be held t_{DH} after the next clock edge.

The operations of inputting data to an input latch and writing data from the input latch to RAM are distinct. To write input data to the RAM, the asynchronous Write Inhibit Controls (Awinh, Bwinh, and/or Ewinh) must be LO as shown in Figure 5. Writes should be enabled no later than t_{WEN} before the falling edge.

Note that a write can be enabled later than a write can be inhibited. If you might want to inhibit a write to the Register File as late as the very phase in which a write is attempted, you can keep the A/B/Ewinh controls normally HI, i.e., write inhibited, and bring them LO every time you actually want to write. Alternatively, for simplicity, the A/Bwinh controls can be wired LO (write enable) and dummy writes be performed to an unused RAM location in every clock HI. Write addresses must always be stable, however, whenever the Write Inhibit controls are LO. In general, do not hardwire Ewinh LO; any Edata-Port output data will be written back to unintended RAM locations.

The write ports are prioritized with the Edata-Port of highest priority, followed by the Adata-Port, followed by the Bdata-Port. If writes to the same RAM location are attempted in a given clock HI phase, the data presented at the higher priority enabled write data port will be the data written to RAM.

SP Bidirectional Edata-Port

The Edata-Port will behave like any write port if treated as such according to the timing diagrams. Alternatively, it will also behave like any read port if treated as such. The Edata-Port can be used as a write port in one cycle, a read port in the next and a write port in the third cycle, as long as the Edata-Port is disabled to high impedance before setting up write data.

SP Input to Input Latches and Hold

Data input to the input latches can be held at those latches with the ABlt and ABht and Elt and Eht controls (Table I). These controls are always registered on the rising edge and become effective at the next falling edge. Figure 6 shows how data written to the latches in any of the three input modes can be held at a latch as long as desired. As of the falling edge after hold is asserted, data at the write data port is ignored and will be ignored until the next falling edge after one of the three input modes is asserted. The hold feature allows the input latches to be used for temporary data storage. Examples of using this feature include delaying a write to the RAM to avoid overwriting some data currently in the RAM or writing the same data to multiple RAM locations.

SP Bank Select

Bank Select is treated in exactly the same way in both Single-Precision and Double-Precision modes (Figure 12). The BS control is not registered in general but rather follows the addresses through the address latches (Figure 1). Hence, its setup requirement is t_{AST} and t_{ASR}, the setup requirement for read and write addresses for transparent and latched/registered modes respectively. All applicable requirements must be met. Flowing with addresses allows Bank Select to track all read and write pipelines as shown in Figure 12. When LO, writes will be disabled and output ports put in high impedance.

With Bank Select, the user's register file space can be extended "vertically" beyond 128 single-precision words to whatever register file space is desired. The user would typically use more than seven bits for addressing, decoding the high-order bits to select a horizontal row of ADSP-3128As that produce a single "word" and applying the low-order seven bits to the address ports in all rows.

The only restriction on extending the register file address space using Bank Select is that all reads and writes in a given cycle must be from the same horizontal row of ADSP-3128As. (Port Select removes this restriction for Double-Precision mode). In Single-Precision mode, the user can select/deselect individual *ports*, even if in different rows, using the asynchronous Write Inhibit and Three-State controls. The user would have to apply these with timing based on the latch modes currently selected to properly track the pipelines.

Note that the timing requirements for Bank Select are simple if write addresses are latched but are more complicated for transparent write addresses because of the way BS flows with the write address. For a Bank Deselect, the BS control must be LO in the clock HI write phase β (Figure 12). If writes are currently enabled, BS must be set up in phase α; if they're inhibited, BS is not needed LO until phase β to disable writes. The Write Inhibit controls for the three write data ports are independent. Therefore, if *any* Write Inhibit is LO (write enable) in phase α, BS will have to be LO in phase α to disable *all* writes.

DOUBLE-PRECISION OPERATION

Double-Precision mode is determined by the registered DP control being HI. A general discussion of dynamic switching between Single- and Double-Precision modes can be found below in "DP/SP Changeover." In Double-Precision mode, the Register File is configured as 64 words that are 32 bits in width. The 64 words are addressed by 6-bit addresses from the five address ports. The seventh, high-order bit used in Single-Precision addressing becomes a Port Select bit. All data paths between RAM and data latches are true 32-bit paths. That is, all 32-bit reads from the RAM to the latches and 32-bit writes to the RAM from the latches take place in a single read or write clock phase. The ports, however, are 16-bits wide. Data transfers through the ports are time-multiplexed.

The ADSP-3128A automatically controls the multiplexing through the data ports once the DP control is HI. The user only supplies one address to reference the two 16-bit halves of the data word transferred through the data ports. In Edata-Port Slow Input and Slow Read modes, however, the user has direct control over these multiplexers to allow communication with slower devices.

Up to five 32-bit data transfers per cycle are possible in Double-Precision mode. These five transfers can be comprised of three writes and two reads or two writes and three reads, depending on whether the Edata-Port is used as a read port or a write port.

Double-Precision mode is intended for interfacing to processors that use time-multiplexed 64-bit data, like Analog Devices' ADSP-32XX Floating-Point Multipliers and ADSP-32XX Floating-Point ALUs. Normally, two ADSP-3128A Multiport Register Files would be used "horizontally" to communicate with 32-bit buses.

In the descriptions that follow, one 16-bit half of a given ADSP-3128A's 32-bit word is referenced as an "Y_Word," the other half as an "X_Word." Note that normally a user would put together the Y_Words from two ADSP-3128As to create a 32-bit half of a 64-bit double-precision floating-point number. Similarly, the floating-point number's other 32-bit half would be constituted from the X_Words of two ADSP-3128As.

What is called a "Y_Word" in this data sheet is simply the 16-bit half of a 32-bit field that is written to the Register File first and read from the Register File first. But it is nothing more than a semantic convention; what are called here "Y_Words" can be used used to make up either Most Significant or Least Significant Words, depending on system requirements. The key point is that whichever half is written first will be the half read first.

DP Normal Reads

Double-Precision mode must be asserted as shown in Figure 7 to insure that the Port Select bits are *not* misinterpreted as Single-Precision address bits and that latch controls are given their proper Double-Precision interpretation. Addresses can be transparent or registered (Figure 7), just as in Single-Precision mode.

The two normal read options in Double-Precision mode are Early Read and Late Read. They are controlled via registered controls CDtran and/or Etran, which can make the output latches transparent or latched. The effect in Double-Precision mode is to create two pipelining options. Note that one control, CDtran, affects both Cdata-Port and Ddata-Port output latches.

Early Reads are generated when CDtran and/or Etran are HI. The Y_Word is read transparently from the RAM in phase γ through the output data port with delays, t_{ODRT} and t_{ODTT}, corresponding to registered and transparent read addresses respectively. The X_Word is also read from the RAM in phase γ but is held at the 32-bit output latch to be multiplexed out the output data port in the next phase with output delay t_{ODC}. Data hold times for Early Reads, as for all other kinds, is t_{ODH}. As described in "Address Latches," the transparent address can be set up before the RAM read phase but t_{ODTT} will then be referenced from the falling clock edge rather than address valid.

Late Reads are generated when CDtran and/or Etran are LO. As with Early Reads, both the Y_Word and X_Word are read from the RAM to the 32-bit output latches in phase γ. In the case of Late Read, the Y_Word is held at the output latch until the next phase, when it is driven off chip with delay t_{ODC}. The X_Word follows in the phase after that with the same delay characteristic of registered reads.

Each read port has its own asynchronous three-state control: Ctri, Dtri and Etri. See Figure 3 for enable and disable timing.

DP Writes

Double-Precision mode must be asserted as shown in Figure 8 to insure that the Port Select bits are *not* misinterpreted as Single-Precision address bits and that latch controls are given their proper Double-Precision interpretation. Addresses can be transparent or registered (Figure 8), just as with Double-Precision reads.

The two normal write options in Double-Precision mode are Early Write and Late Write. They are exactly analogous to Early Read and Late Read in that they offer two pipelining options. They are controlled via registered controls ABlt, ABht, Elt and Eht as shown in Figure 8 and Table II. Note that one set of controls, ABlt and ABht, affects both Adata-Port and Bdata-Port input latches. These controls become effective as of the falling edge after they are registered.

In Early Write, both Y_Word and X_Word are input to the 32-bit input latches before they are both written to RAM in phase δ. Both Y_Word and X_Word have the setup time requirement, t_{DSR}, characteristic of latched-mode data inputs. Data hold requirements for Early Write and all other writes is t_{DH}.

With Late Write, the user can input the Y_Word and X_Word into the Register File latches one half cycle later for a write to RAM in the same phase δ. The Y_Word is latched with setup time t_{DSR}. The X_Word, however, is transparently written to RAM in phase δ. Note that the setup requirement on the X_Word is therefore t_{DST}.

The actual write to RAM occurs in the single phase δ. Hence the Write Inhibit controls in Double-Precision work exactly as they do in Single-Precision. To write input data to the RAM, the asynchronous Write Inhibit Controls (Awinh, Bwinh and/or Ewinh) must be LO as shown in Figure 8. Writes should be enabled no later than t_{WEN} before the falling edge.

Note that a write can be enabled later than a write can be inhibited. If you might want to inhibit a write to the Register File as late as the very phase in which a write is attempted, you can keep the A/B/Ewinh controls normally HI, i.e., write inhibited, and bring them LO every time you actually want to write. Alternatively, for simplicity, the A/Bwinh controls can be wired LO (write enable) and dummy writes be performed to an unused RAM location in every clock HI. Write addresses must always be stable, however, whenever the Write Inhibit controls are LO. In general, do not hardwire Ewinh LO; any Edata-Port output data will be written back to unintended RAM locations.

The write ports are prioritized with the Edata-Port of highest priority, followed by the Adata-Port, followed by the Bdata-Port. If writes to the same RAM location are attempted in a given clock HI phase, the data presented at the higher priority enabled write data port will be the data written to RAM.

DP Edata-Port Slow Input and Slow Read

The bidirectional Edata-Port is intended to be the port interfaced to a system bus, which may run more slowly than local buses. To simplify the interface for Double-Precision, the ADSP-3128A provides a mode for loading the Y_Word and X_Word into the input latches over multiple ADSP-3128A clock cycles (Figure 9). Also a mode is provided for multiplexing Y_Word and X_Word read data from the output latches over multiple clock cycles (Figure 10).

For a Slow Input (Figure 9), the input latches are updated when there is a *transition* in a designated control input from one clock rising edge to the next clock rising edge. Both Clock-on-Falling and Clock-on-Rising Slow Input modes are supported. Rfltran LO indicates that data is to be loaded on the clock's falling edge, Rfltran HI indicates rising edge. In the case of Clock-on-Falling, the transition *in Eht* updates the latches while Elt is concurrently HI (Hold mode). Call Eht the "transition control" for Clock-on-Falling and Elt the "background control". Clock-on-Rising reverses the role of these two controls; the transition *in Elt* causes the latches to update while Eht is concurrently HI. In other words, for Clock-on-Rising, Elt becomes the transition control, Eht the background control. Regardless of which clock edge is loading the data, it must be set up to the input latches with set up time t_{DSR} as shown.

When the transition control goes from HI to LO, the external data will be input to the Y_Word position in the Edata input latch and be held there. When the transition control goes from LO to HI, the external data will be input to the X_Word position in the Edata input latch and be held there. A write to RAM can be enabled (with Ewinh LO) at the next clock HI from either latched or transparent Eadr.

For a Slow Read, registered control Eio, when asserted HI in conjunction with Double-Precision (DP HI), configures the Edata-Port for a Slow Read. When Eio goes HI, data at the output latch is held. In Figure 10, this is the 32-bit data read at phase γ. For a Slow Read, output delays will be t_{ODC}. Data will be held t_{OH} after the clock edges shown in Figure 10. When configured for Slow Read, the ADSP-3128A's registered Etran control becomes a direct, asynchronous controller of the Edata-Port's Double-Precision output multiplexer. When Etran is LO, the Y_Word read from RAM in phase γ will be driven through the Edata-Port (if enabled with Etri). When Etran is HI, the X_Word read from RAM in phase γ will be driven through the Edata-Port (if enabled with Etri). The outputs will be driven as long as Eio is HI and Etran doesn't change.

DP Input to A&B Data-Port Input Latches and Hold

Data input to the A&Bdata-Port input latches can be held at those latches with the ABlt and ABht, controls (Table I). These controls are always registered on the rising edge and become effective as of the next falling edge. Figure 11 shows how data written to the latches in either Early Write or Late Write modes can be held at a latch as long as desired. As of the falling edge after hold is asserted with ABlt HI, data at the write data port is ignored. It will continue to be ignored until the next falling edge after ABlt goes LO. The hold feature allows the input latches to be used for temporary data storage. Note that the Edata-Port supports Input-and-Hold in SP only, since Elt is used in DP for Slow Edata-Port inputs.

DP Bank Select and Port Select

Bank Select is treated in exactly the same way in both Single-Precision and Double-Precision modes (Figure 12). The BS control is not registered in general but rather follows the addresses through the address latches (Figure 1). In Double-Precision, the seventh address bit (not needed for Double-Precision addressing) is redefined to function as Port Select for the ports being addressed. DP must be asserted HI as shown in Figure 13 to insure that these bits are interpreted as Double-Precision Port Selects and not Single-Precision address bits (and that latch controls are given their proper Double-Precision interpretation).

Behaving as addresses, both BS and A/B/C/D/Eadr$_6$ have setup requirements of t_{ASTx} and t_{ASRx}, the setup requirement for read and write addresses for transparent and latched/registered modes, respectively. All applicable requirements must be met. Flowing with addresses allows Bank Select and Port Select to track all read and write pipelines as shown in Figures 12 and 13. When LO, writes will be disabled and output ports put in high impedance.

The only restriction on extending the register file address space using Bank Select is that all reads and writes in a given cycle must be from the same horizontal row of ADSP-3128As. Port Select removes this restriction for Double-Precision mode (only). Like Bank Select, the Port Select controls track the ADSP-3128A's internal pipelines. But since every port can be independently selected or deselected, reads can be made from and writes made to any combination of locations in the user's register file space. They need not be all made from the same horizontal row.

Note that the timing requirements for Bank Select and Port Select are simple if write addresses are latched but are more complicated for transparent write addresses because of the way BS and A/B/Eadr$_6$ flow with the write address. For a Bank or Port Deselect, the BS or A/B/Eadr$_6$ control must be LO in the clock HI write phase β (Figures 12 and 13). If writes are currently enabled, BS or A/B/Eadr if they're inhibited, BS or A/B/Eadr$_6$ is not needed LO until phase β to disable writes. Since the Write Inhibit controls for the three write data ports are independent, if any is enabled in phase α, BS or A/B/Eadr$_6$ will have to be LO in phase α to disable all writes.

DP/SP Changeover

Many controls are interpreted and internal states affected by the DP control. The timing diagrams show when DP must be HI and when it must be LO to accomplish the operation described in each timing diagram. For times when the state of DP is not explicitly shown, it can be changed. That is, the user can dynamically reconfigure the ADSP-3128A from Single-Precision to Double-Precision and conversely as long as these restrictions are observed.

Internal RAM Organization

It may be useful to know that a 32-bit word in Double-Precision mode consists of two 16-bit words that can be addressed in Single-Precision mode with seven bit addresses by the six bit address used in double precision mode (*n*) and that address plus 64 (*n+64*). The Y_Word of the double-precision word will be in *n*; the X_Word in *n+64*. By switching from Double- to Single-Precision, the user can independently access the Y_Word and the X_Word.

DESIGN CONSIDERATIONS

Power Up

At power up, any or all of the three output ports, Edata-Port, Cdata-Port or Ddata-Port, may be driving off chip. Because of pipelining, Bank Select should not be used to serve a reset or "chip select" function unless no other devices on the buses driven by these ports could themselves possibly be driving. Bank Select will tristate these ports, but they cannot be guaranteed to be in a high impedance state until t_{DIS} into the second cycle after the rising edge at which BS is LO (Figure 12).

Any ADSP-3128A output port that shares a buses should be forced into a high impedance state at power up using the Etri/-Ctri/Dtri controls. The bits driving these pins from microcode can be gated with the user's general system reset control.

Power Supply Decoupling

The ADSP-3128A register file is designed with high speed drivers on all output pins. This means that large peak currents may pass through the driver ground and V_{DD} pins, particularly when all output port lines are simultaneously charging their load capacitance in transition, whether from LO to HI or vice versa. These peak currents can cause a large disturbance in the ground and supply lines. To help isolate the effects of this disturbance, the ADSP-3128A provides separate pins for driver GND and V_{DD}s and logic GND and V_{DD}s.

The ADSP-3128A's GND and V_{DD} pins must be tied directly to solid ground and V_{DD}planes and properly bypassed. Lead lengths and trace lengths should be as short as possible. The ground plane should tie to driver GND in particular with a very low inductance path. High frequency bypass capacitors (0.1μF ceramic) should be located as close as possible to the V_{DD} pins. Low frequency bypass capacitors (20μF tantalum) should be located *outside* the chip perimeter (not directly under the chip). System noise immunity can be improved by careful design of V_{DD} and GND planes. See the Applications Note, "Power and Ground Connection Guidelines for Pin Grid Arrays" for layout suggestions.

KEY CHANGES FROM JUNE 1988 ADSP-3128A
A PRELIMINARY DATA SHEET

The ADSP-3128A is a pin-compatible speed-upgrade to the ADSP-3128 with the following qualifications:

1. The specification t_{WINH} has been added and the specification t_{WIN} has been redefined to make it easier to use. The Write Inhibit Delay (t_{WIN}) is the maximum time after the rising edge of the clock before the A/B/Ewinh pin must be high to inhibit a write to the register file. The new specification Write Inhibit Control Hold Time (t_{WINH}) is the minimum hold time required after the falling edge of the clock to insure that the enable write or inhibit write has occurred. New versions of Figure 5 and Figure 8 show this timing.
2. The Elt and Eht lines are reversed in Figure 9 and the last two entries of Table I in the June 1988 Data Sheet for Double Precision Clock-on-Rising Slow Inputs to the E-port. Figure 9 and Table I have been corrected. Paragraph two of DP Edata-Port Slow Input and Slow Read on Page 3–54 has also been changed.
3. The specifications t_{AST} and t_{ASR} have been separated for reads and writes. The new specifications are:

Transparent Address Setup – Read	t_{ASTR}
Transparent Address Setup – Write	t_{ASTW}
Registered Address Setup – Read	t_{ASRR}
Registered Address Setup – Write	t_{ASRW}

4. The low-level input voltage level on the Clock line is 0.6V maximum. On all other lines it remains 0.8V maximum.
5. I_{DD} Supply Current is 600mA maximum.
6. The Edata-port can function in any one cycle as either a read port or a write port. It cannot both read and write in one cycle.
7. Extra reads from the C, D and Edata-ports are no longer allowed.
8. The following specifications have been removed:

t_{EDIS}	Three-State E Port Auto-Disable
t_{HIER}	Clock Period HI – Write Plus Extra Read
t_{ODRTH}	Clock Address-to-Transparent Delay – Extra Reads
t_{CLK}	Clock Period – Clocked Reads
t_{CLKS}	Clock Period – Trans Reads
t_{CLKA}	Clock Period – Transparent I/O
t_{ASTBS}	Trans. Clk HI Bank Select Setup
t_{ODCE}	Clk-to-Data Output Delay – Eport

SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-3128A J and K Grades Min	Max	ADSP-3128A S and T Grades[2] Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature (Ambient)	0	+70	−55	+125	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-3128A J and K Grades Min	Max	ADSP-3128A S and T Grades[2] Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0				V
V_{IHA}	High-Level Input Voltage, CLK and All Asynchronous Control Inputs	@ V_{DD} = max	2.2				V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8			V
V_{IL}	Low-Level Input Voltage (CLK)	@ V_{DD} = min		0.6			V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4				V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4			V
I_{IH}	High-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 5.0V		10			μA
I_{IL}	Low-Level Input Current, All Inputs	@ V_{DD} = max & V_{IN} = 0.0V		10			μA
I_{OZ}	Three-State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0V or max		50			μA
I_{DD}	Supply Current[3]	@ max Clock Rate; TTL Inputs (CLK = 0, 3V)		600			mA
I_{DDQ}	Supply Current-Quiescent	All V_{IN} = 2.4V		100			mA

3

ORDERING INFORMATION

Part Number	Temperature Range	Package
ADSP-3128AJG	0 to +70°C	144-Pin Grid Array
ADSP-3128AKG	0 to +70°C	144-Pin Grid Array
ADSP-3128ASG	−55 to +125°C	144-Pin Grid Array
ADSP-3128ATG	−55 to +125°C	144-Pin Grid Array
ADSP-3128ASG/883B	−55 to +125°C	144-Pin Grid Array
ADSP-3128ATG/883B	−55 to +125°C	144-Pin Grid Array

SWITCHING CHARACTERISTICS

Parameter		ADSP-3128A J Grades 0 to +70°C Min	J Grades 0 to +70°C Max	K Grades 0 to +70°C Min	K Grades 0 to +70°C Max	S Grades[2] −55 to +125°C Min	S Grades[2] −55 to +125°C Max	T Grades[2] −55 to −125°C Min	T Grades[2] −55 to −125°C Max	Unit
t_L	Clock LO Period			20						ns
t_H	Clock HI Period			22						ns
t_{CS}	Control Setup			10						ns
t_{CH}	Control Hold			1						ns
t_{ASTR}	Transparent Address Setup – Read			18						ns
t_{ASTW}	Transparent Address Setup – Write			30						ns
t_{ASRR}	Registered Address Setup – Read			4						ns
t_{ASRW}	Registered Address Setup – Write			11						ns
t_{AH}	Address Hold			3						ns
t_{ENA}	Three-State Enable Delay			2	21					ns
t_{DIS}	Three-State Disable Delay				11					ns
t_{DISBS}	Three-State Disable Delay – Bank & Port Sel				24					ns
t_{ODTT}	Trans Adr-to-Trans Output Delay				39					ns
t_{ODC}	Clk-to-Data Output Delay – C & Dports				18					ns
t_{ODRT}	Clkd Adr-to-Trans Output Delay				40					ns
t_{ODH}	Output Data Hold			3						ns
t_{DSR}	Latched Data Setup				7					ns
t_{DST}	Transparent Data Setup				18					ns
t_{DSN}	Clock-on-Falling Data Setup				12					ns
t_{DH}	Input Data Hold			1						ns
t_{WEN}	Write Enable Setup			23						ns
t_{WIN}	Write Inhibit Delay				0					ns
t_{ATBE}	Trans Adr to Write Enable			1						ns
t_{WINH}	Write Inhibit Control Hold Time			0						

NOTES

[1]All min and max specifications are over power-supply and temperature range indicated. Input levels are GND and 3.0V. Rise times are 5ns. Input timing reference levels and output reference levels are 1.5V, except for t_{ENA}, t_{DIS} and t_{DISBS} which are as indicated in Figures 3, 12 and 13.

[2]S and T grade parts are available processed in accordance with MIL-STD-883, Class B. The processing and test methods used for S/883B and T/883B versions of the ADSP-3128A can be found in Analog Devices' Military Data Book. Regular S and T grade parts are tested at +125°C.

[3]Worst-case with all outputs switching twice per cycle. (Example: DP Reads)

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

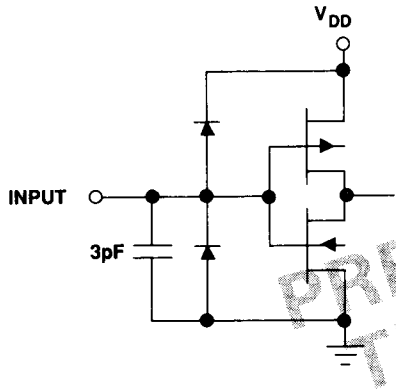
Supply Voltage . . . . . −0.3V to +7V
Input Voltage . . . . . −0.3V to V_{DD} +0.3V
Output Voltage Swing . . . . . −0.3V to V_{DD} +0.3V
Operating Temperature Range (Ambient) . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (10sec) PGA . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

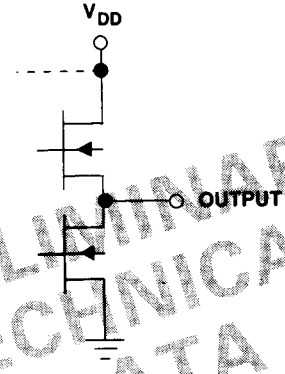
ESD SENSITIVITY

The ADSP-3128A features proprietary input protection circuitry. Per Method 3015 of MIL-STD-883C, the ADSP-3128A has been classified as a Class 1 device.

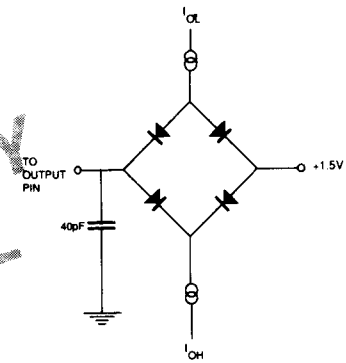
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.



Equivalent Input Circuits



Equivalent Output Circuits



Normal Load for ac Measurements

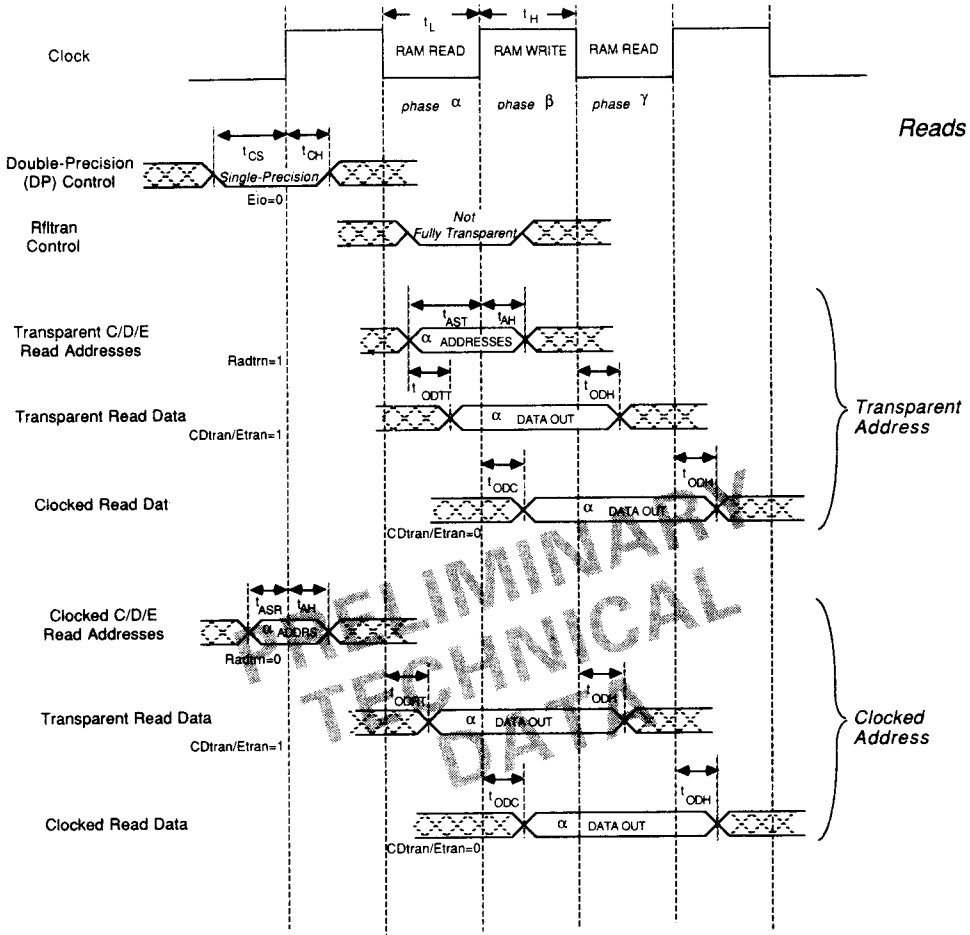


Figure 4. ADSP-3128A Single-Precision Read Output Timing

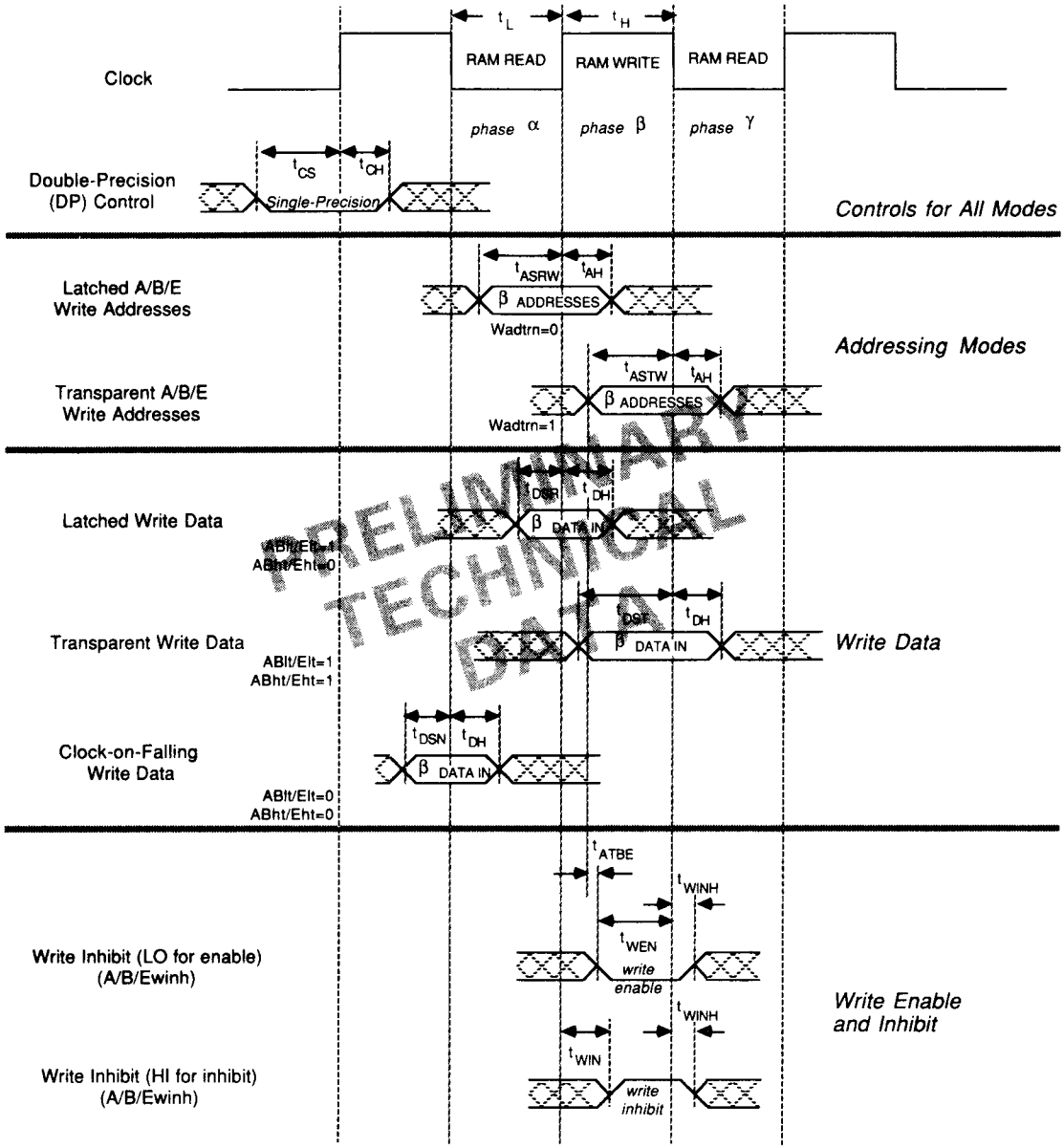


Figure 5. ADSP-3128A Single-Precision Write Input Timing

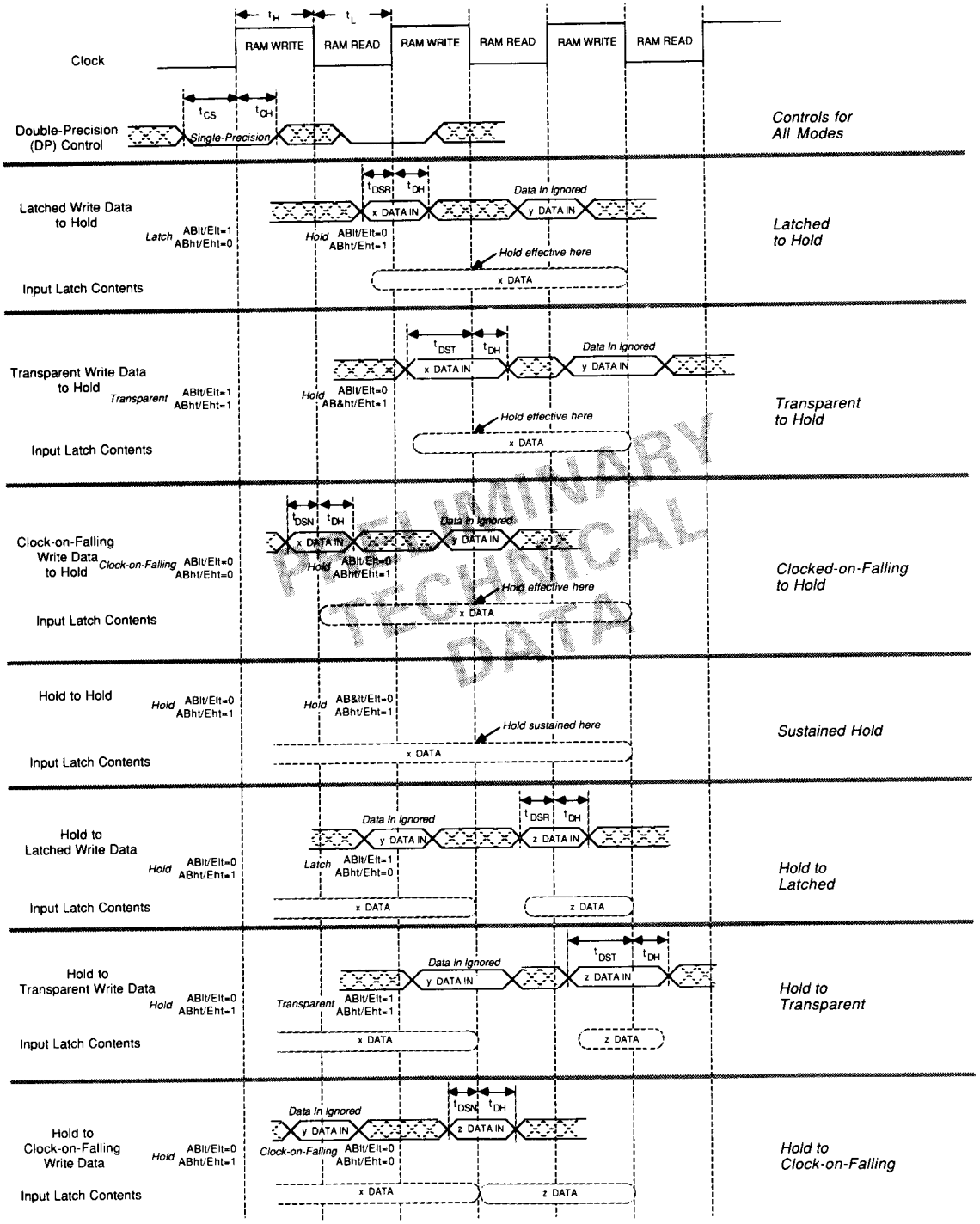


Figure 6. ADSP-3128A Single-Precision Write to Input Latches and Hold Timing

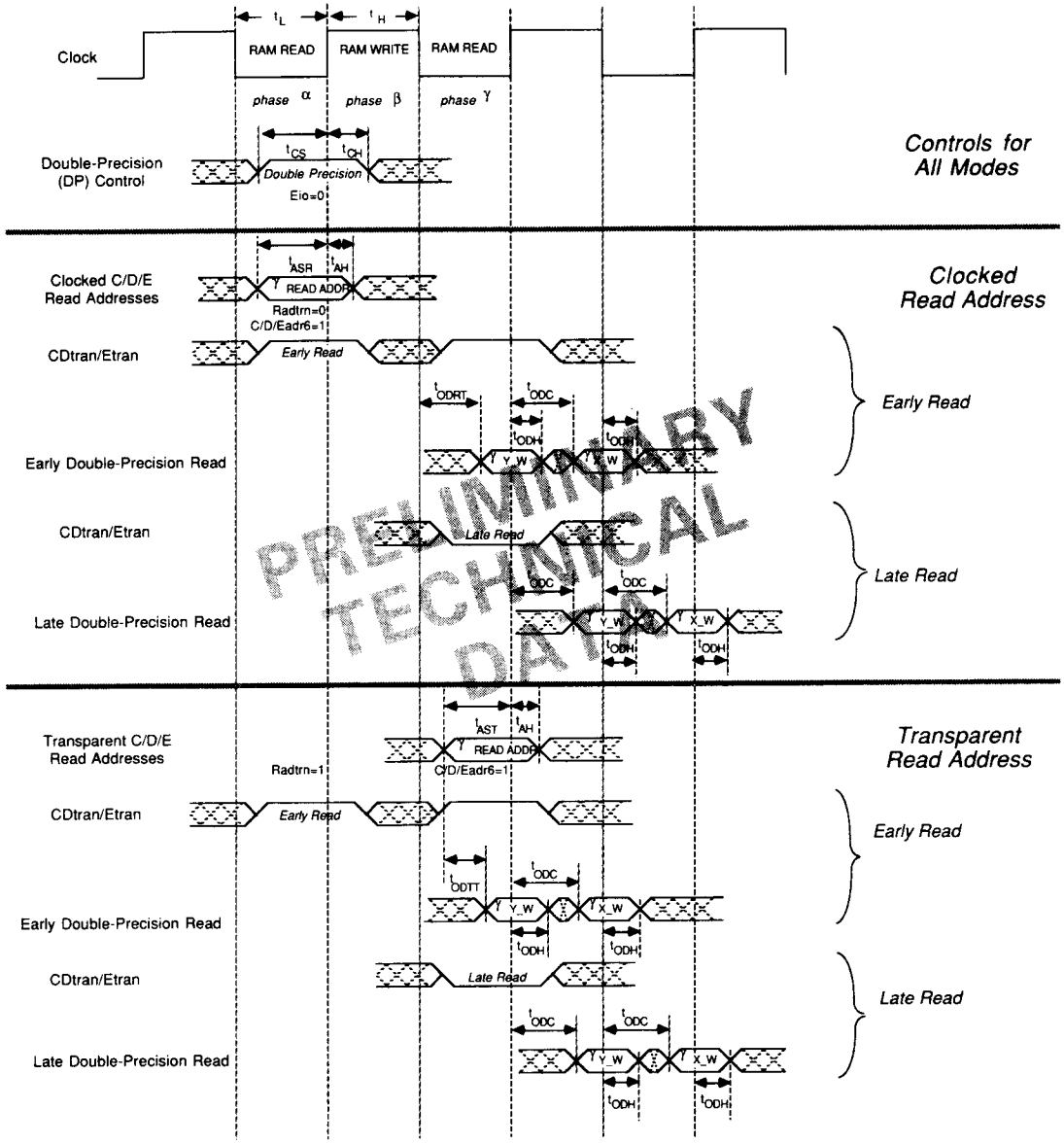


Figure 7. ADSP-3128A Double-Precision Read Output Timing

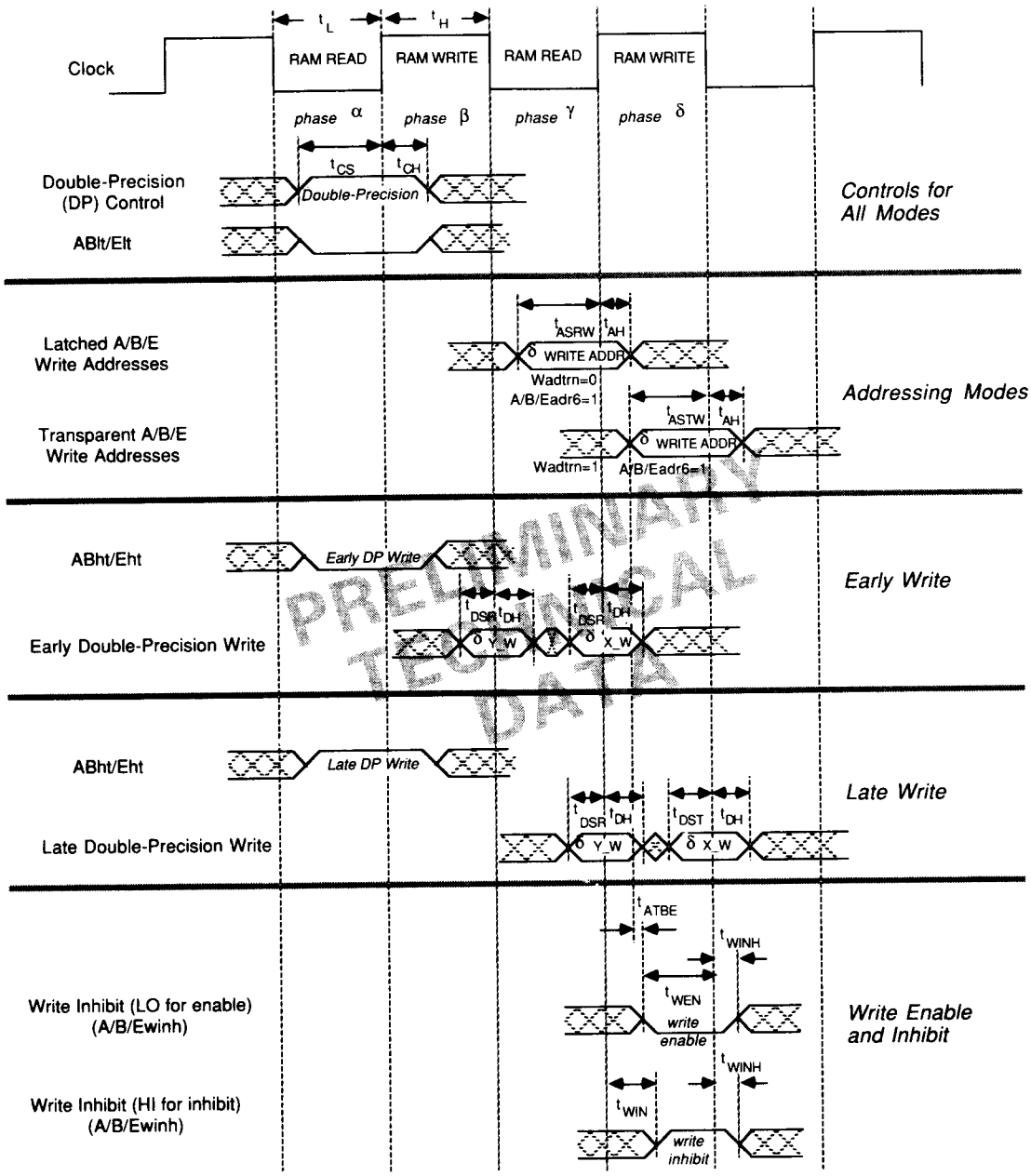
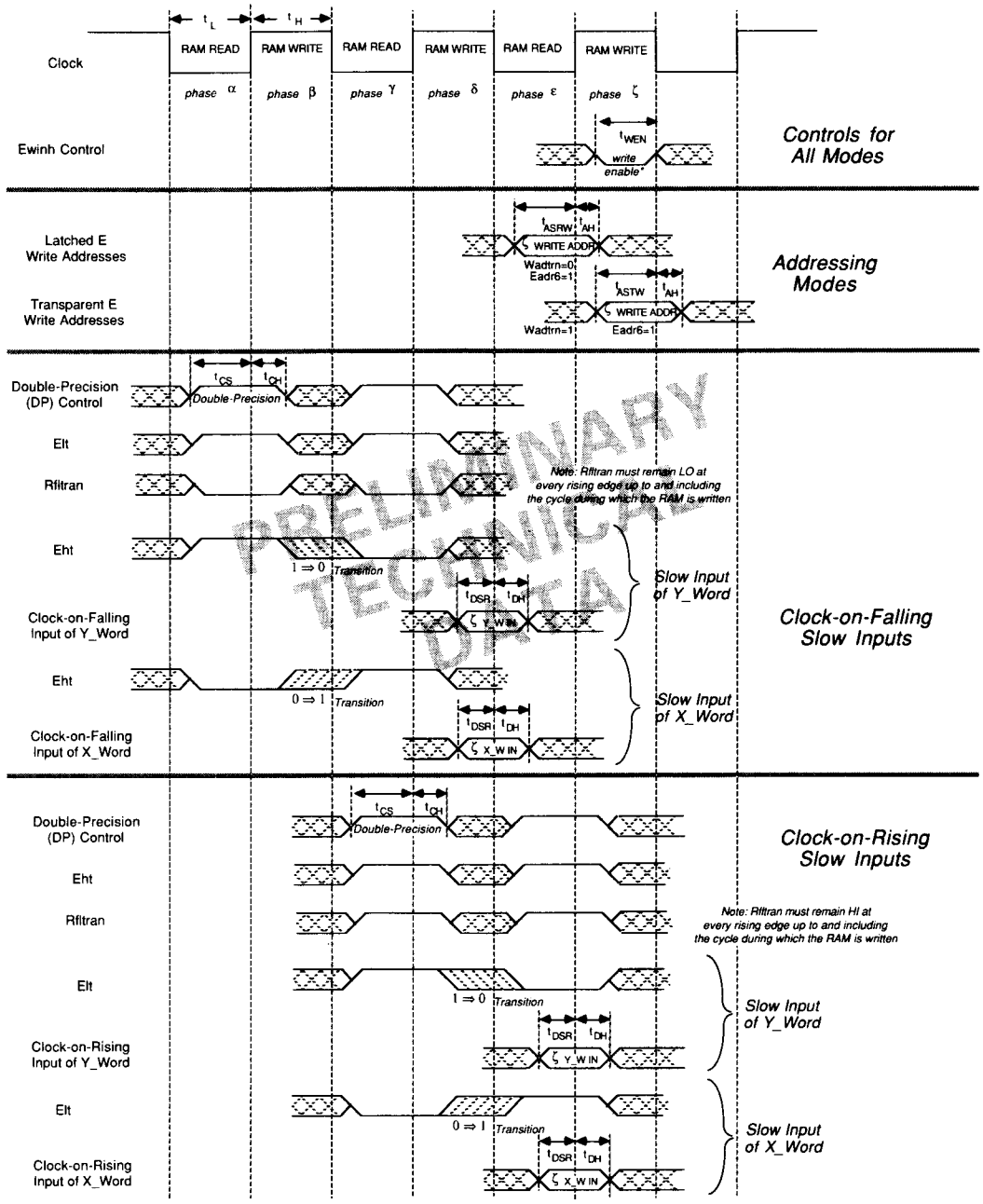


Figure 8. ADSP-3128A Double-Precision Write Input Timing



* See Figure 9 for the complete set of conditions for Ewinh

Figure 9. ADSP-3128A Double-Precision Slow Edata-Port Input Timing

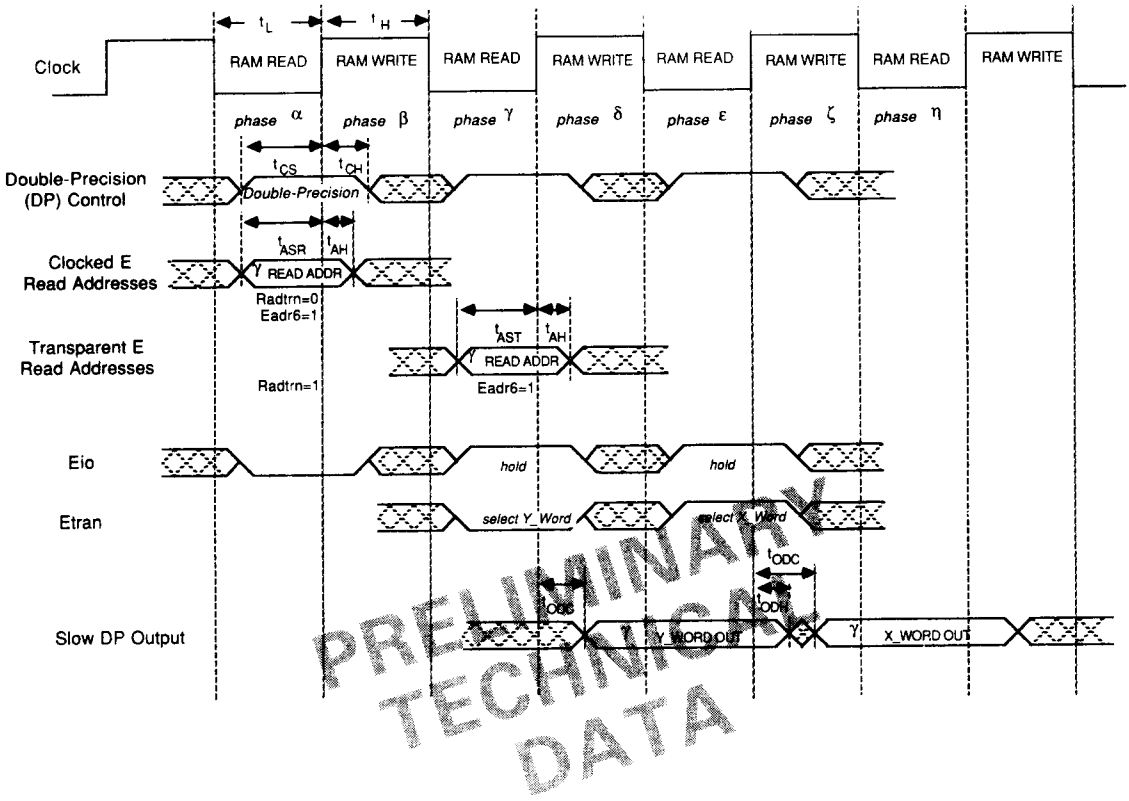


Figure 10. ADSP-3128A Double-Precision Slow Edata-Port Read Output Timing

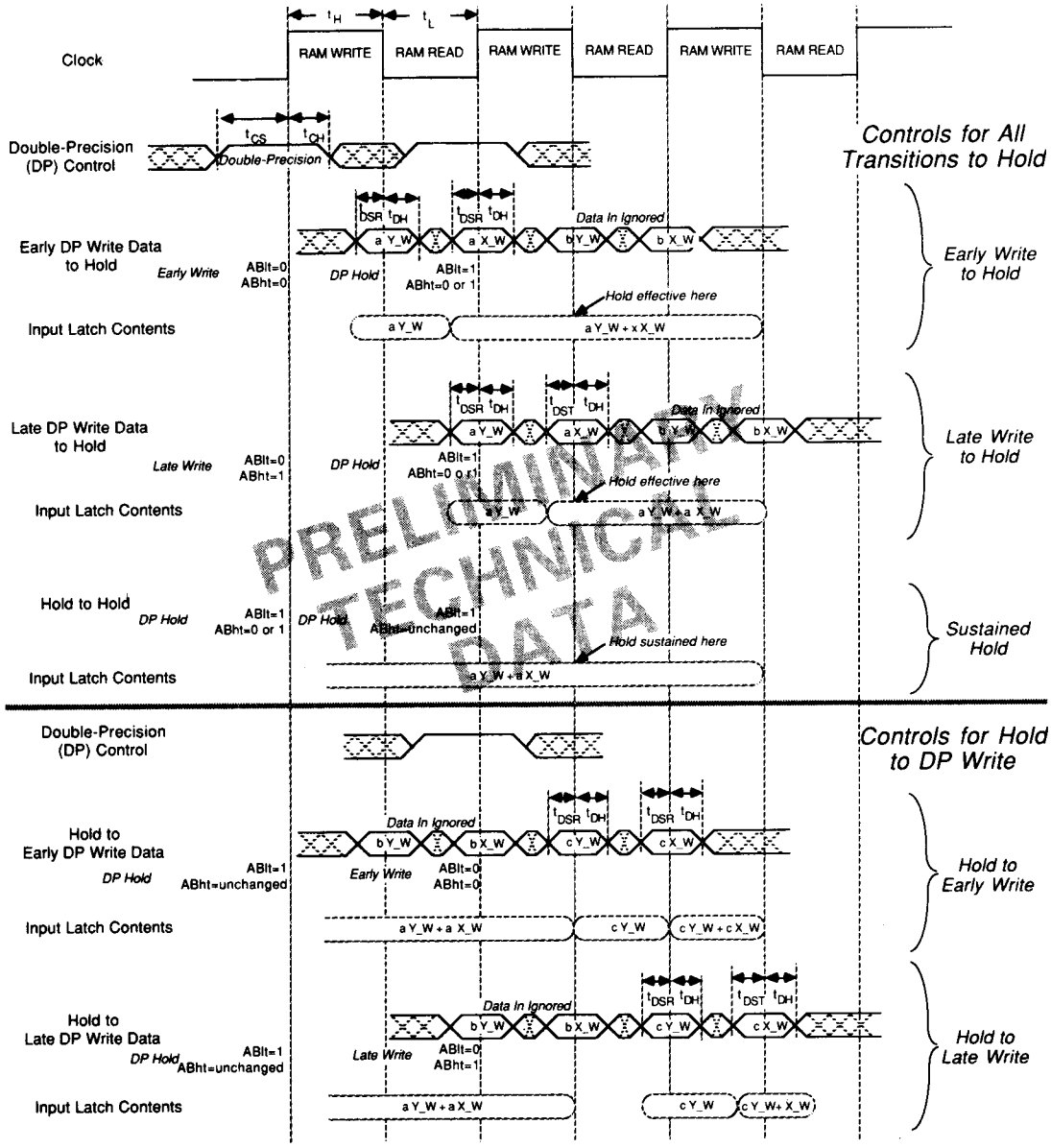


Figure 11. ADSP-3128A Double-Precision Write to Input Latches and Hold Timing (Adata-Port and Bdata-Port only)

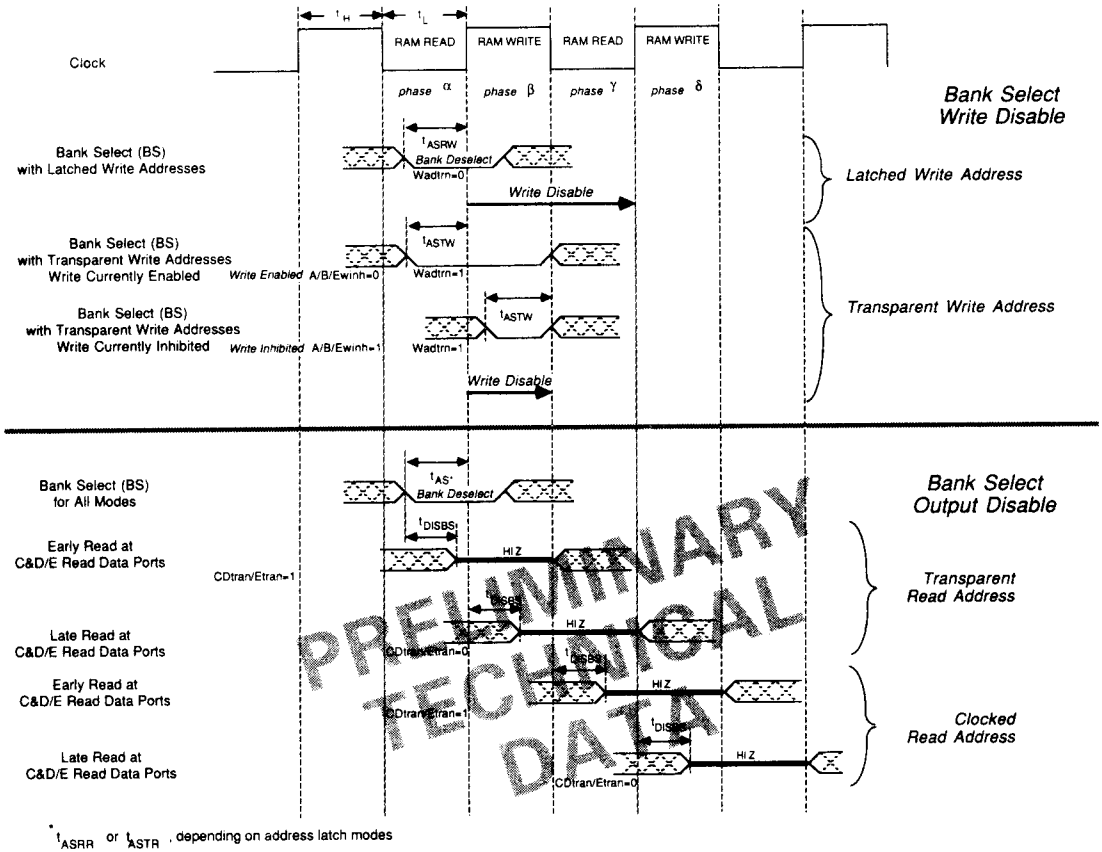


Figure 12. ADSP-3128A Bank Select Timing

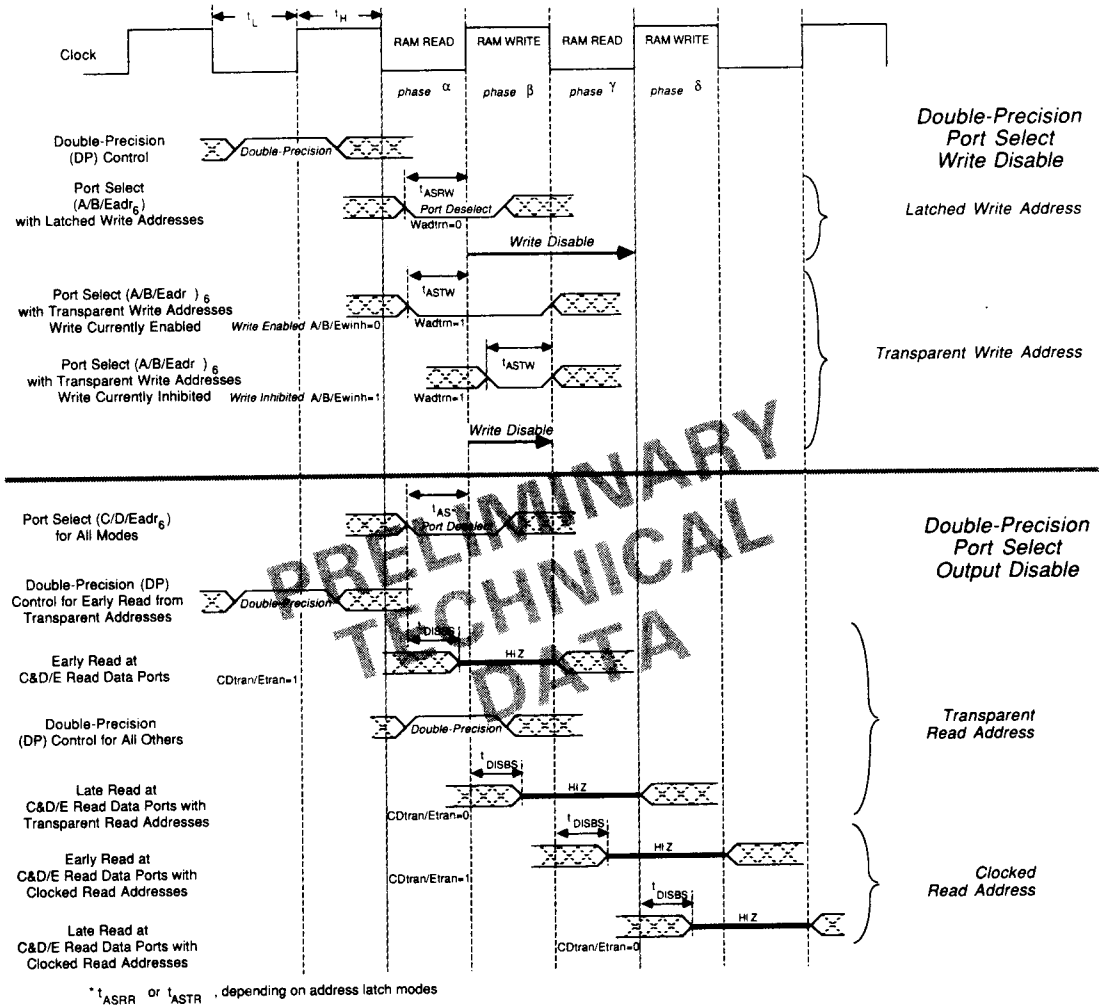


Figure 13. ADSP-3128A Double-Precision Port Select Timing

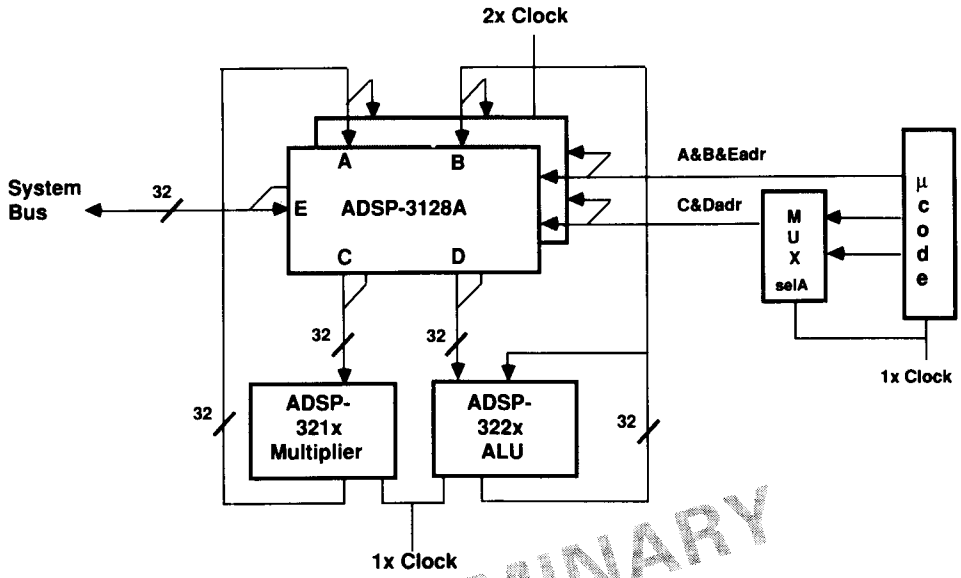


Figure 14. ADSP-3128A Single-Precision Application with ADSP-32XX

Muxing the read addresses allows two reads (at 1×clock) for loading the input ports of both the ADSP-321X and ADSP-322X with two 32-bit words per 32XX cycle (at 1×clock) while still using 1×μcode rates. In this application, write data is latched on clock HI and read data is registered on the rising edge. Write addresses are latched; read addresses are transparent.

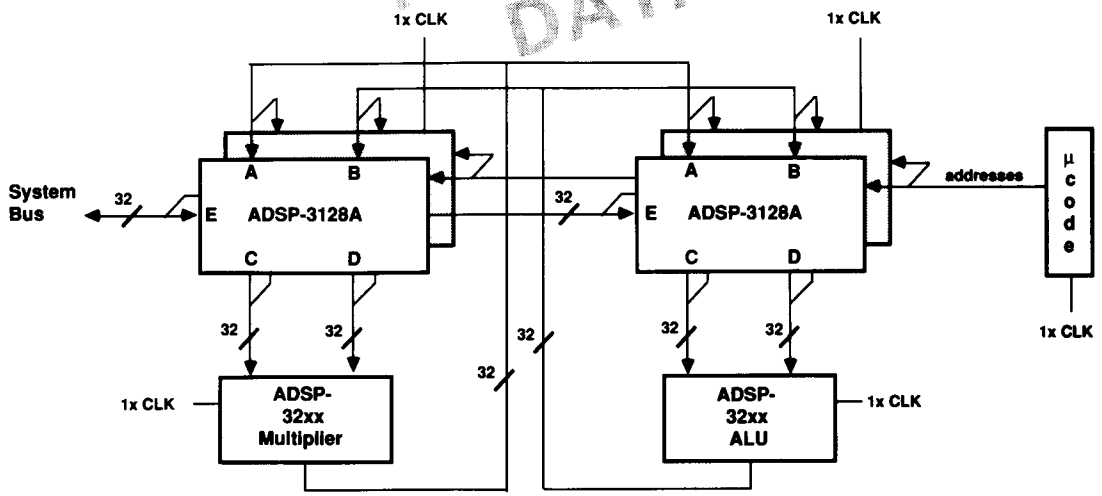


Figure 15. ADSP-3128A Seven-Port Double-Precision Application with ADSP-32XX

Double-Precision mode allows transfer of both MSW and LSW in a single cycle while still using μcode at the same cycle rate. Pairing pairs of ADSP-3128As creates a seven-port register file for unconstrained data transfers. The same data is always written to both the right and left pairs (therefore, the same A, B and Eadrs go to both pairs). In this application, Early Writes are used at the input ports for the simplest interface to the floating-point chipset's output. The data read from the two sides is generally distinct, so the C and Dadrs for each pair are distinct. Late Reads match the input loading requirements of these chips and are, therefore, used on the rightmost pair of ADSP-3128As.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Q	Bdata8	Bdata5	Bdata2	Bdata0	Adata13	Adata10	Adata9	Adata7	Adata4	Adata3	Eht	ABht	ABlt	Awinh	Aadr0	Q
P	Bdata12	Bdata9	Bdata6	Bdata4	Bdata1	Adata14	Adata12	Adata8	Adata2	Adata1	Elt	DP	Bwinh	internal GND	Aadr3	P
N	Edata15	Bdata13	Bdata10	Bdata7	Bdata3	Adata15	Adata11	Adata6	Adata5	Adata0	Ewinh	internal GND	internal GND	Aadr2	Aadr6	N
M	Edata14	Bdata15	Bdata11										Aadr1	Aadr4	Badr1	M
L	Edata12	Edata13	Bdata14										Aadr5	Badr0	Badr4	L
K	Edata8	Edata10	Edata11										Badr2	Badr3	Cadr0	K
J	Edata7	Edata9	Edata6										Badr6	Badr5	Cadr1	J
H	Edata4	Edata3	Edata5										Cadr4	Cadr2	Cadr3	H
G	Edata2	Ddata15	Edata0										Cadr5	Dadr1	Cadr6	G
F	Edata1	Ddata13	Ddata12										Dadr3	Dadr2	Dadr0	F
E	Ddata14	Ddata10	Ddata8										Eadr2	Dadr5	Dadr4	E
D	Ddata11	internal GND	driver Vdd	driver GND									Eadr5	Eadr1	Dadr6	D
C	Ddata9	Ddata7	Ddata4	Ddata3	Ddata0	Cdata10	driver GND	driver GND	Cdata1	Etri	Wadtrn	driver Vdd	internal Vdd	Eadr3	Eadr0	C
B	driver GND	Ddata5	Ddata1	Cdata15	Cdata12	Cdata9	Cdata8	Cdata4	Cdata0	CDtran	Ctri	Radtrn	Rfltran	Eadr6	Eadr4	B
A	Ddata6	Ddata2	Cdata14	Cdata13	Cdata11	Cdata7	Cdata6	Cdata5	Cdata3	Cdata2	Etran	Dtri	BS	Eio	CLK	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

BOTTOM VIEW

ADSP-3128A Pinout