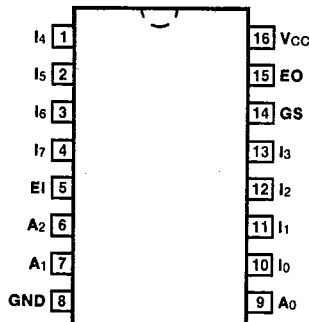


18

T-66-31-51

9318
93L18
8-INPUT PRIORITY ENCODER

CONNECTION DIAGRAM
PINOUT A



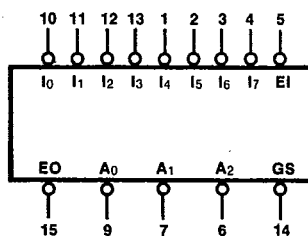
DESCRIPTION — The '18 multipurpose encoders are designed to accept eight inputs and produce a binary weighted code of the highest order input.

- MULTIFUNCTION CAPABILITY
CODE CONVERSIONS
MULTI-CHANNEL D/A CONVERTER
DECIMAL TO BCD CONVERTER
- CASCADING FOR PRIORITY ENCODING OF N BITS
- INPUT ENABLE CAPABILITY
- PRIORITY ENCODING — AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE
- OUTPUT ENABLE — ACTIVE LOW WHEN ALL INPUTS HIGH
- GROUP SIGNAL OUTPUT — ACTIVE WHEN ANY INPUT IS LOW

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	9318PC, 93L18PC		9B
Ceramic DIP (D)	A	9318DC, 93L18DC	9318DM, 93L18DM	6B
Flatpak (F)	A	9318FC, 93L18FC	9318FM, 93L18FM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

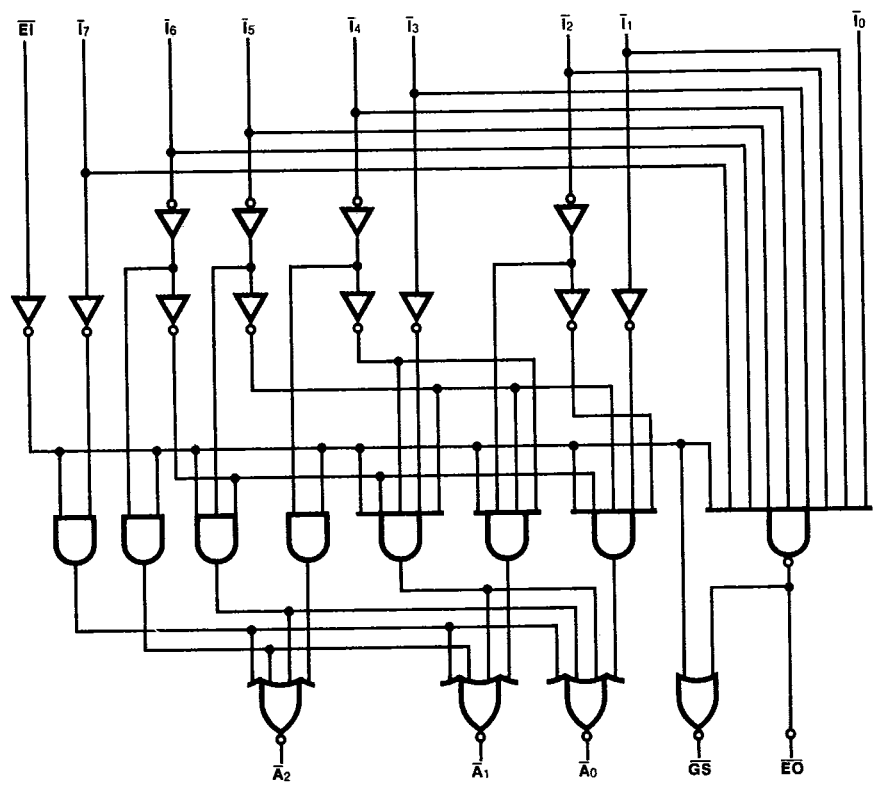
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
I ₀	Priority Input (Active LOW)	1.0/1.0	0.5/0.25
I ₁ — I ₇	Priority Inputs (Active LOW)	2.0/2.0	1.0/0.5
EI	Enable Input (Active LOW)	2.0/2.0	1.0/0.5
EO	Enable Output (Active LOW)	20/10	10/5.0 (3.0)
GS	Group Select Output (Active LOW)	20/10	10/5.0 (3.0)
A ₀ — A ₂	Address Outputs (Active LOW)	20/10	10/5.0 (3.0)

T-606-31-51

FUNCTIONAL DESCRIPTION — The '18 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input (\overline{EI}) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output (\overline{GS}) and Enable Output (\overline{EO}) are provided with the three data outputs. The \overline{GS} is active LOW when any input is LOW; this indicates when any input is active. The \overline{EO} is active LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both \overline{EO} and \overline{GS} are in the inactive HIGH state when the input enable is HIGH.

LOGIC DIAGRAM



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T. 66-31-51

TRUTH TABLE

	INPUTS								OUTPUTS					
	\overline{EI}	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	\overline{GS}	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	\overline{EO}
H	X	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	H	L	L	L	L	H
L	X	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current $I_0 - T_7, \overline{EI}$		1.0			mA	$V_{CC} = \text{Max}, V_{IN} = 5.5 \text{ V}$
I_{OS}	Output Short Circuit Current	-20	-70			mA	$V_{CC} = \text{Max}, V_{OUT} = 0 \text{ V}$
I_{CC}	Power Supply Current		77		22	mA	$V_{CC} = \text{Max}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}, T_A = +25^\circ \text{ C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$		$C_L = 15 \text{ pF}$			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay T_n to \overline{EO}	10 18		18 50		ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay \overline{EI} to \overline{GS}	14 16		20 28		ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay \overline{EI} to \overline{EO}	14 22		20 36		ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay \overline{EI} to $\overline{A_n}$	17 17		33 26		ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay T_n to \overline{GS}	14 16		60 26		ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay T_n to $\overline{A_n}$	21 21		36 36		ns	Figs. 3-1, 3-20