HARRIS
SEMICONDUCTOR

HSP45240

Address Sequencer

Features

- **Block Oriented 24-Bit Sequencer**
- **Configurable as Two Independent 12-Bit Sequencers**
- **24 x 24 Crosspoint Switch**
- **Programmable Delay on 12 Outputs**
- **Multi-Chip Synchronization Signals**
- **Standard μP Interface**
- **100pF Drive on Outputs**
- **DC to 50MHz Clock Rate**

Applications

- **1-D, 2-D Filtering**
- **Pan/Zoom Addressing**
- **FFT Processing**
- **Matrix Math Operations**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45240JC-33	0°C to +70°C	68 Lead PLCC
HSP45240JC-40	0°C to +70°C	68 Lead PLCC
HSP45240JC-50	0°C to +70°C	68 Lead PLCC
HSP45240GC-33	0°C to +70°C	68 Lead PGA
HSP45240GC-40	0°C to +70°C	68 Lead PGA
HSP45240GC-50	0°C to +70°C	68 Lead PGA

Description

The Harris HSP45240 is a high speed Address Sequencer which provides specialized addressing for functions like FFTs,1-D and 2-D filtering, matrix operations, and image manipulation. The sequencer supports block oriented addressing of large data sets up to 24-bits at clock speeds up to 50MHz.

Specialized addressing requirements are met by using the onboard 24 x 24 crosspoint switch. This feature allows the mapping of the 24 address bits at the output of the address generator to the 24 address outputs of the chip. As a result, bit reverse addressing, such as that used in FFTs, is made possible.
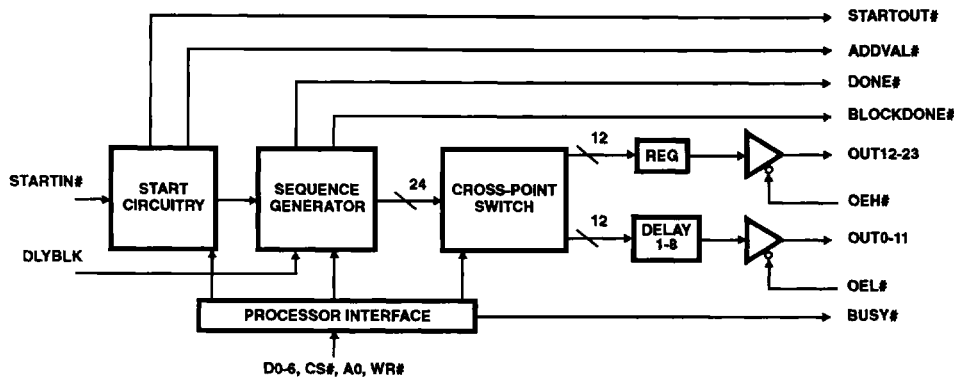
A single chip solution to read/write addressing is also made possible by configuring the HSP45240 as two 12-bit sequencers. To compensate for system pipeline delay, a programmable delay is provided on 12 of the address outputs.

The HSP45240 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs, with the exception of clock, are TTL compatible.

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SPECIAL
FUNCTION

Block Diagram

File Number **2489.3**

HSP45240

Package Pinouts

ADDRESS SEQUENCER HSP45240
68 PIN PLASTIC LEADED CHIP CARRIER (PLCC)

Top pins (left to right): GND, OUT23, OUT22, V_CC, OUT21, OUT20, GND, OUT19, OUT18, V_CC, OUT17, OUT16, GND, OUT15, OUT14, OUT13, NC
Pin numbers: 9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61

Left side:
NC	10
D0	11
D1	12
D2	13
D3	14
D4	15
D5	16
D6	17
GND	18
WR.#	19
A0	20
CS.#	21
GND	22
CLK	23
V_CC	24
RST.#	25
NC	26

Right side:
60	NC
59	OUT12
58	GND
57	OUT11
56	OUT10
55	V_CC
54	OUT9
53	OUT8
52	GND
51	OUT7
50	OUT6
49	V_CC
48	OUT5
47	OUT4
46	GND
45	OUT3
44	NC

Bottom pin numbers: 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
Bottom pins (left to right): NC, OEH.#, OEL.#, DLYBLK, STARTIN.#, STARTOUT.#, ADDVAL.#, V_CC, BUSY.#, BLOCKDONE.#, DONE.#, GND, OUT0, OUT1, V_CC, OUT2, NC

68 PIN GRID ARRAY (PGA)
(BOTTOM VIEW)

	1	2	3	4	5	6	7	8	9	10	11
L		OEH.#	DLYBLK	START OUT.#	VCC	BLOCK DONE.#	GND	OUT1	OUT2	NC	
K	NC	NC	OEL.#	START IN.#	ADD VAL.#	BUSY.#	DONE.#	OUT0	VCC	NC	OUT3
J	RST.#	VCC								GND	OUT4
H	CLK	GND								OUT5	VCC
G	CS.#	A0								OUT6	OUT7
F	WR.#	GND								GND	OUT8
E	D6	D5								OUT9	VCC
D	D4	D3								OUT10	OUT11
C	D2	D1								GND	OUT12
B	D0	NC	OUT22	OUT21	GND	OUT18	OUT17	GND	OUT14	NC	NC
A		GND	OUT23	VCC	OUT20	OUT19	VCC	OUT16	OUT15	OUT13	

Pin Descriptions

NAME	TYPE	PLCC PIN NUMBER	DESCRIPTION
V$_{CC}$	I	6,24,34,41 49,55,68	+5V power supply pin.
GND	I	3,9,18,22 38,46,52 58,65	GROUND
RST#	I	25	RESET: This active low input causes a chip reset which lasts for 26 clocks after RST# has been de-asserted. The reset initializes the Crosspoint Switch and some of the configuration registers as described in the Processor Interface section. The chip must be clocked for reset to complete.
CLK	I	23	CLOCK: The "CLK" signal is a CMOS input which provides the basic timing for address generation.
WR#	I	19	WRITE: The rising edge of this input latches the data/address on D0-6 to be latched into the Processor Interface.
CS#	I	21	CHIP SELECT: This active "low" input enables the configuration data/address on D0-6 to be latched into the Processor Interface.
A0	I	20	ADDRESS 0: This input defines D0-6 as a configuration register address if "high", and configuration data if "low", (see Processor Interface text).
D0-6	I	11-17	DATA BUS: Data bus for Processor Interface.
OEH#	I	28	OUTPUT ENABLE HIGH: This asynchronous input is used to enable the output buffers for OUT12-23.
OEL#	I	29	OUTPUT ENABLE LOW: This asynchronous input is used to enable the output buffers for OUT0-11.
STARTIN#	I	31	START-IN: This active low input initiates an addressing sequence. May be tied to STARTOUT# of another HSP45240 for multi-chip synchronization. STARTIN# should only be asserted for one CLK because address sequencing begins after STARTIN# is de-asserted.
DLYBLK	I	30	DELAY BLOCK: This active "high" input may be used to halt address generation on address block boundaries (see Sequence Generator text). The required timing relationship of this signal to the end of an address block is shown in Application Note 9205.
OUT0-23	O	39,40,42,45, 47,48,50,51, 53,54,56,57, 59,62-64,66, 67,1,2,4,5, 7,8	OUTPUT BUS: TTL compatible 24-bit Address Sequencer output.
BLOCKDONE#	O	36	BLOCK DONE: This active low output signals when the last address in an address block is on OUT0-23.
DONE#	O	37	DONE: This active low output signals when the last address of an address sequence is on OUT0-23.
ADDVAL#	O	33	ADDRESS VALID: This active low output signals when the first address of an address sequence is on OUT0-23.
STARTOUT#	O	32	START-OUT: This active low output is generated when an address sequence is initiated by a mechanism other than STARTIN#. May be tied to the STARTIN# of other HSP45240's for multichip synchronization.
BUSY#	O	35	BUSY: This active low output is asserted one CLK after RST# is de-asserted and will remain asserted for 25 CLK's. While BUSY# is asserted all writes to the Processor Interface are disabled.

# Denotes active low.

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SPECIAL FUNCTION

Functional Description

The Address Sequencer is a 24-bit programmable address generator. As shown in the Block Diagram, the sequencer consists of 4 functional blocks: the start circuitry, the sequence generator, the crosspoint switch, and the processor interface. The addresses produced by the sequence generator are input into the crosspoint switch. The crosspoint switch maps 24 bits of address input to a 24 bit output. This allows for addressing schemes like "bit-reverse" addressing for FFT's. A programmable delay block is provided to allow the MSW of the output to be skewed from the LSW. This feature may be used to compensate for processor pipeline delay when the sequence generator is configured as two independent 12 bit sequencers. Address Sequencer operation is controlled by values loaded into configuration registers associated with the sequence generator, crosspoint switch, and start circuitry. The configuration registers are loaded through the processor interface.

Start Circuitry

The Start Circuitry generates the internal START signal which causes the Sequence Generator to initiate an addressing sequence. The START signal is produced by writing the Processor Interface's "Sequencer Start" address (see Processor Interface text), by asserting the STARTIN# input, or by the terminal address of a sequence generated under "One-Shot Mode with Restart" (see Sequence Generator section). Care should be taken to assert STARTIN# for only one clock cycle to insure proper operation. A programmable delay from 1 to 31 clocks is provided to delay the initiation of an addressing sequence by delaying the internal START signal (see Processor Interface text).

The Start Circuitry generates the output signal ADDVAL# which is asserted when the first valid output address is at the pads. In addition, the Start Circuitry generates the "STARTOUT#" signal for multichip syncronization. Note: STARTOUT# is only generated when an addressing sequence is started by writing the "Sequencer Start" address of the Processor Interface, or an internal START is generated by reaching the end of an addressing sequence produced by "One-Shot Mode with Restart".

Sequence Generator

The Sequence Generator is a block oriented address generator. This means that the desired address sequence is subdivided into one or more address blocks each containing a user defined number of addresses. User supplied configuration data determines the number of address blocks and the characteristics of the address sequence to be generated.

As shown in Figure 1, the Sequence Generator is subdivided into the an address generation and control section. The address generation section performs an accumlation based on the output of MUX1 and MUX2. The control section governs the operation of the multiplexers, enables loading of the Block Start Address register, and signals completion of an address sequence.

An address sequence is started when the control section of the Sequence Generator receives the internal START signal from the Start Circuitry. When the START signal is received, the control section multiplexes the contents of the Start

Address Register and a "0" to the adder. The result of this summation is the first address in the first block of the address sequence. This value is stored in the Block Start Address register by an enable generated from the control section, and the multiplexers are switched to feed the output of the Holding and Address Increment registers to the adder. Address generation will continue with the Address Increment added to the contents of the Holding Register until the first address block has been completed.

An address block is completed when the number of addresses generated since the beginning of the address block equals the value stored in the Block Size register. When the last address of the block is generated, BLOCKDONE# is asserted to signal the end of the address block (see Application Note 9205). On the following CLK, the multiplexers are configured to pass the contents of the Block Start Address and Block Increment registers to the adder which generates the first address of the next address block. An enable from the control section allows this value to update the Block Start Address register, and the multiplexers are switched to feed the Holding and Address Increment registers to the adder for generation of the remaining addresses in the block.

The address sequence is completed when the number of address blocks generated equals the value loaded into the Number of Blocks register. When the final address in the last address block has been generated, DONE# and BLOCKDONE# are asserted to signal the completion of the address sequence.

The parameters governing address generation are loaded into five 24-bit configuration registers via the Processor Interface. These parameters include the Start Address, the beginning address of the sequence; the Block Size, the number of addresses in the address block; the Address Increment, the increment between addresses in a block; the Number of Blocks, the number of address blocks in a sequence (minimum 1); the Block Increment, the increment between starting addresses of each block. The loading and structure of these registers is detailed in the Processor Interface text.
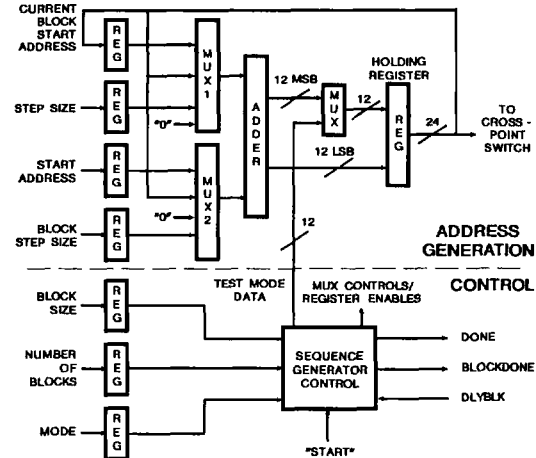

FIGURE 1. SEQUENCE GENERATOR BLOCK

Three modes of operation may be selected by loading the 6-bit Mode Control register (see Processor Interface). The three modes of operation are:

1. One-Shot Mode without Restart Address generation halts after completion of the user specified address sequence. Address generation will not resume until the internal START signal is generated by the Start Circuitry. When the final address in the final block of the address sequence is generated, both DONE# and BLOCKDONE# are asserted and the last address is held on OUT0-23 (See Application Note 9205). 2.

2. One-Shot Mode with Restart: This mode is identical to One-Shot Mode without Restart with the exception that the Start Circuitry automatically generates an internal START at the end of the user specified sequence to restart address generation. The end of the address sequence is signaled by the assertion of DONE#, BLOCKDONE#, and STARTOUT# as shown in Application Note 9205. In this mode, the first address of the next sequence immediately follows the last address of the current sequence if start delay is disabled.

3. Continuous Mode: Address generation never terminates. Address generation proceeds based on the Start Address, Address Increment, Block Size, and Block Increment Parameters. The Number of Blocks parameter is ignored, and the DONE# signal is never asserted.

The Mode Control register is also used to configure the Sequence Generator for operation as two independent 12-bit address sequencers. In dual sequencer mode, the adder in the sequence generator suppresses the carry from the 12 LSBs to the 12 MSBs. With the carry suppressed, two independent sequences may be produced. These 12-bit address sequences may be delayed relative to each other by programming the Mode Control register for a delay up to 7 clocks. This feature is useful to compensate for pipeline delay when using dual sequencer mode to generate read/write addressing.

The DLYBLK input can be used to halt address generation at the end of any address block within a sequence. In addition, DLYBLK can be used to delay an address sequence from restarting if asserted at the end of the final address block generated under "One-Shot Mode with Restart". See Application Note 9205 for the timing relationship of DLYBLK to the end of the address block required to halt address sequencing.

Crosspoint Switch

The crosspoint switch is responsible for reordering the address bits output by the sequence generator. The switch allows any of its 24 inputs to be independently connected to any of its 24 outputs. The crosspoint switch outputs can be driven by only one input, however, one input can drive any number of switch outputs. If none of the inputs are mapped to a particular output bit, that output will be "low".

The input to output map is configured through the processor interface. The I/O map is stored in a bank of 24 configuration registers. Each register corresponds to one output bit. The output bit is mapped to the input via a value, 0 to 23, stored in the register. After power-up, the user has the option of configuring the switch in 1:1 mode by using the reset input,

"RST#". In 1:1 mode the cross-point switch outputs are in the same order as the input. More details on configuring the switch registers are contained in the Processor Interface text.

Processor Interface

The Processor Interface consists of a 10 pin microprocessor interface and a register bank which holds configuration data. The data is loaded into the register bank by first writing the register address to the processor Interface and then writing the data. An auto address increment mode is provided so that a base address may be written followed by a number of data writes.

The microprocessor interface consists of a 7 bit data bus (D0-6), a one bit address select (A0) to specify D0-6 as either address or data, a write input (WR#) to latch data into the Processor Interface, and a chip select input (CS#) to enable writing to the interface. The Processor Interface input is decoded as either data or address as shown by the bit map in Table 1.

TABLE 1.

	A0	D6	D5	D4	D3	D2	D1	D0
REGISTER ADDRESSES								
Switch Output Registers	1	x	0	n	n	n	n	n
Sequencer Starting Address	1	x	1	0	0	0	n	n
Sequencer Block Size	1	x	1	0	0	1	n	n
Sequencer Number of Blocks	1	x	1	0	1	0	n	n
Sequencer Block	1	x	1	0	1	1	n	n
Address Increment								
Sequencer Address	1	x	1	1	0	0	n	n
Increment								
Mode Control	1	x	1	1	0	1	0	0
Test Control	1	x	1	1	0	1	0	1
Start Delay Control	1	x	1	1	0	1	1	0
Address Sequencer "START"	1	x	1	1	1	1	1	1
DATA WORDS								
Current Address Data	0	0	n	n	n	n	n	n
(no address increment)								
Current Address Data (address increment)	0	1	n	n	n	n	n	n

NOTES:

1. Table 1 "x" means "don't care", and "n" denotes bits which are decoded as an address in address registers and data in data registers.

2. When WR# transitions "high" to write the Sequencer "Start" address (1x111111), it must remain high until after a rising edge of clock. Otherwise, the sequencer "start" signal will not be generated.

The register bank consists of a series of 6 bit registers which may be addressed individually as shown in Table 1. The data in these registers is down loaded into configuration registers in the Start Circuitry, Sequence Generator, and Crosspoint Switch when an address sequence is initiated by the internal START signal (see Start Circuitry). This double buffered architecture allows new configuration data to be down loaded to the Processor Interface while an address sequence is being completed using previous configuration data.

The register bank has five sets of four registers which contain address generation parameters. These parameters include: Address Start, Block Size, Number of Blocks, Block Increment, and Address Increment. Each register set maps to one of five 24-bit configuration registers in the Sequence Generator block (see Sequence Generator). The mapping of the 6-bit registers in the register bank to the 24-bit configuration registers is determined by the 2 LSB's of the register address. The higher the value of the 2 LSB's the higher the relative mapping of the 6-bit register to the 24-bit register. For example, if the 2 LSB's of the register address are both 0, the register contents will map to the 6 LSB's of the configuration register.

The register bank has 24 registers which contain the data for Crosspoint Switch I/O mapping. These registers are accessed via the 5 LSB's of the address for the Crosspoint Mapping registers in Table 1. A value from 0 to 23 accesses the mapping registers for OUT0-23 repectively. A value greater than 23 is ignored. The output bit represented by a particular register is mapped to the input by the 6-bit value loaded into the register. If the value loaded into the register exceeds 23, the correponding output bit will be "0". For example, if the 5 LSB's of the Crosspoint Mapping address are equal to 3, and the valued loaded into the register accessed by this address is equal to 23, OUT3 would be mapped to the MSB of the sequence generator output.

After a reset, the Mode Control, Test Control, and Start Delay registers are reset as described in the section describing each register's bit map; the Crosspoint Mapping registers are reset to a 1:1 crosspoint switch mapping; the registers which hold the five address generation parameters are not affected.

To save the user the expense of alternating between address and data writes, an auto address increment mode is provided. The address increment mode is invoked by performing data writes with a "1" in the D6 location of the data word as shown in Table 1. For example, the crosspoint switch could be configured by 25 writes to the Processor Interface (one write for the starting address of the crosspoint mapping registers followed by 24 data writes to those registers).

Mode Control Register

The Mode Control Register is used to control the operation of the sequence generator. In addition, it also controls the output delay between the MSW and the LSW of OUT0-23. The following tables illustrate the structure of the mode control register.

TABLE 2. MODE CONTROL REGISTER FORMAT

ADDRESS LOCATION: 1x110100					
D5	D4	D3	D2	D1	D0
OD2	OD1	OD0	DS	M1	M0

ODx – Output Delay: Delays OUT0-11 from OUT12-23 by the following number of clocks.

OD2	OD1	OD0	
0	0	0	Output Delay of 0
0	0	1	Output Delay of 1
0	1	0	Output Delay of 2
0	1	1	Output Delay of 3
1	0	0	Output Delay of 4
1	0	1	Output Delay of 5
1	1	0	Output Delay of 6
1	1	1	Output Delay of 7

DS – Dual Sequencer Enable: Allows two independent 12- bit sequences to be generated.

0	A 24-bit sequence is generated.
1	Two 12-bit sequences are generated.

Mx – Mode: Sequencer Mode.

M1	M0	
0	0	One-Shot Mode without Restart
0	1	One-Shot Mode with Restart
1	x	Continuous Mode (x = don't care)

During reset, this register will be reset to all zeroes. This will configure the chip as a 24-bit sequencer with zero delays on the outputs. The chip will also be in one-shot mode without restart.

Start Delay Control Register

The Start Delay Control Register is used to configure the start circuitry for delayed starts from 1 to 31 clock cycles. Internal "START", external "START", and restarts will be delay by the programmed amount. The structure of the Start Delay Control Register is shown in Table 3.

TABLE 3. START DELAY CONTROL REGISTER FORMAT

ADDRESS LOCATION: 1x110110					
D5	D4	D3	D2	D1	D0
SDE	SD4	SD3	SD2	SD1	SD0

SDE – Start Delay Enable: Enables "START" to be delayed by the programmed amount. When Start Delay is enabled, a minimum of "1" is required for the programmed delay.

0	Start Delay is Disabled.
1	Start Delay is Enabled.

SDx – Start Delay: Delays the "START" by the decoded number of clocks.

SD4	SD3	SD2	SD1	SD0	
0	0	0	0	1	Start Delay of 1
0	0	0	1	0	Start Delay of 2
0	0	0	1	1	Start Delay of 3
1	1	1	1	1	Start Delay of 31

During reset, this register will be reset to all zeros. This will bring the chip up in a mode with Start Delay disabled.

Test Control Register

A Test Control Register is provided to configure the sequence generator to produce test sequences. In this mode, the sequence generator can be configured to multiplex out the contents of the down counters in the sequence generator control circuitry, Figure 2. These counters are used to determine when a block or sequence is complete. As shown in Figures 1 and 2, the MSW or LSW in the down counters is multiplexed to the MSW of the address generator output. In addition, a test mode is provided in which the sequence generator performs a shifting operation on the contents of the start address register. The structure of the Test Control Register is shown in Table 4.
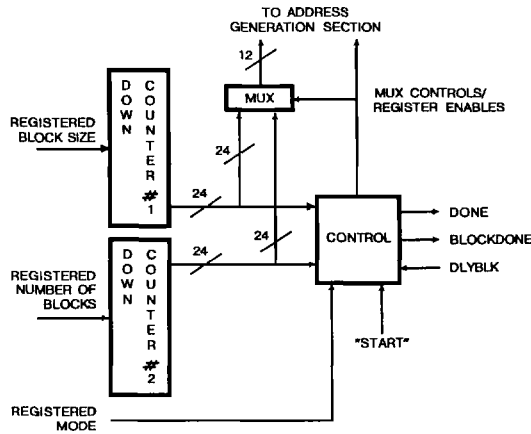
FIGURE 2. SEQUENCE GENERATOR CONTROL

TABLE 4. TEST CONTROL REGISTER FORMAT

ADDRESS LOCATION: 1x110101					
D5	D4	D3	D2	D1	D0
xx	xx	SE	COE	CS1	CS0

Bits "D5" and "D6" are currently not used.

SE - Shifter Enable: Input to crosspoint switch is generated by shifting Start Address Register one bit per clock.

0	Sequence Generator Functions Normally
1	Sequence Generator Functions as Shift Register

COE - Counter Output Enable: Enable contents of down counters in the sequence generator control circuitry to be muxed to the 12 MSB's of the address generator output.

0	Disable Muxing of down counters
1	Enable Muxing of down counters

CS - Counter Select: Selects which 12-bit word of the down counters is muxed to the MSW of the address generator output.

CS1	CS0	
0	0	Select Counter #1, bits 0-11
0	1	Select Counter #1, bits 12-23
1	0	Select Counter #2, bits 0-11
1	1	Select Counter #2, bits 12-23

During reset, this register will be reset to all zeroes. This will bring the chip up in the mode with all of the test features disabled.

Applications

Image Processing

The application shown in Figure 3 uses the HSP45240 Address Sequencer to satisfy the addressing requirements for a simple image processing system. In this example the controller configures the sequencers to generate specialized addressing sequences for reading and writing the frame buffers. A typical mode of operation for this system might be to perform edge detection on a sub-section of an image stored in the frame buffer. In this application, data is fed to the 2-D Convolver by the address sequence driving the input frame buffer.

A graphical interpretation of sub-image addressing is shown in Figure 4. Each dot in the figure corresponds to an image pixel stored in memory. It is assumed that the pixel values are stored by row. For example, the first 16 memory locations would contain the first row of pixel values. The 17th memory location would contain the first pixel of the second row.
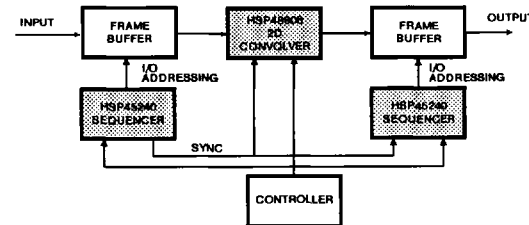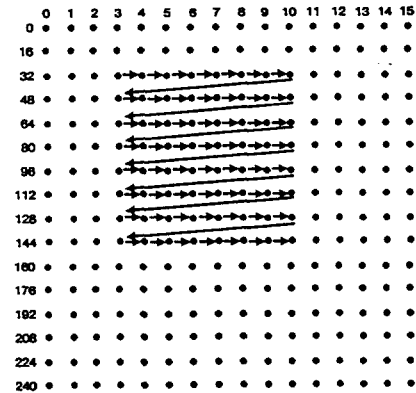

FIGURE 3. IMAGE PROCESSING SYSTEM

FIGURE 4. SEQUENCER SUB-IMAGE ADDRESSING

The sub-image address sequence shown in Figure 3 is generated by configuring the sequence generator with the following:

1. Start Address = 35   4. Step Size = 1
2. Block Size = 8   5. Block Step Size = 16
3. Number of Blocks = 8

In this example the start address corresponds to the address of the first pixel of the first row. The row length corresponds to the Block Size which is programmed to 8. Within the block, consecutive addresses are generated by programming the Step Size to 1. At the completion of first block of addresses, the Block Step Size of 16 is added to the Start Address to generate the address of the first pixel of the second row. Finally, 8 rows of addressing are generated by setting the Number of Blocks to 8.

In this application, the sub-image is processed one time and then a new sub-image area is chosen. As a result, the Mode Control Register would be configured for One-Shot mode without Restart. Also, the Start Delay Control register of the Sequencer driving the output frame buffer would be configured with a start delay to compensate for the pipeline delay introduced by the 2-D Convolver. Finally, the crosspoint switch would be configured in 1:1 mode so that the sequence generator output has a 1 to 1 mapping to the chip output.

For applications requiring decimation of the original image, the Step Size could be increased to provide addressing which skips over pixels along a row. Similary, the Block Step Size could be increased such that pixel rows are skipped.

FFT Processing

The application shown in Figure 5 depicts the architecture of a simplified radix 2 FFT processor. In this application the Address Sequencer drives a memory bank which feeds the arithmetic processor with data. In a radix 2 implementation, the arithmetic processor takes two complex data inputs and produces two results. These results are then stored in the registers from which the data came. This type of implementation is referred to as an "in place" FFT algorithm.

The arithmetic processing unit performs an operation know as the radix 2 butterfly which is shown graphically in Figure 6. In this diagram the node in the center of the butterfly represents summing point while the arrow represents a multiplication point. The flow of an FFT computation is described by diagrams comprised of many butterflies as shown in Figure 7.

The FFT processing shown in Figure 7 consists of three stages of radix 2 butterfly computation. The read/write addressing, expressed in binary, for each stage is shown in Table 5. The specialized addressing required here is produced by using the crosspoint switch to map the address bits from the sequence generator to the chip output.

The mapping for the sequencer's crosspoint switch is determined, by inspecting the addressing for each stage. For example, the first stage of addressing is generated by configuring the crosspoint switch so that bit 0 of the switch input is mapped to bit 2 of the switch output, bit 1 of the

switch input is mapped to bit 0 of the output, and bit 2 of the switch input is mapped to bit 1 of the switch output. The remainder of the switch I/O map is configured 1:1, i.e. bit 3 of the switch input is mapped to bit 3 of the switch output. Under this configuration, a sequence generator output of 0,1,2,3,4,5,6,7 will produce a crosspoint switch output of 0,4,1,5,2,6,3,7. The switch maps for the other stages as well as a map for the bit-reverse addressing of the FFT result is given in Table 5.

The serial count required as input for the crosspoint switch is generated by configuring the sequence generator with the following:

1. Start Address = 0   4. Step Size = 1
2. Block Size = 8   5. Block Step Size = 0
3. Number of Blocks = 1

Under this configuration the sequence generator will produce a count from 0 to 7 in increments of 1. The FFT length corresponds to the Block Size, in this case 8.

The serial count from the sequence generator is converted into the desired addressing sequence by applying the appropriate map to the crosspoint switch. In this application, the switch mapping changes for each stage of the FFT computation. Thus, while one address sequence is being completed, the crosspoint switch is being configured for the next stage of FFT addressing. When one stage of addressing is complete, the new switch configuration is loaded into the current state registers by an internal or externally generated start or restart.

The crosspoint switch is configured for the first stage of addressing by writing a 0 to switch output register 2, a 2 to switch output register 1, and a 0 to switch output register 2. These values are loaded by first writing the address of switch output register 0 and then loading data using auto-address increment mode (see Table 1). The remaining registers are assumed to be configured in 1:1 mode as a result of a prior "RESET". The second and third stages of addressing are generated by reconfiguring the above three registers.

The Address Sequencer can be configured in dual sequencer mode to provide both read and write addressing for each butterfly. Since 2 independent 12 bit sequences can be generated by the Address Sequencer, it can be used to provide read/write addressing for FFT's up to 4096 points. The programmable delay between the MSW and LSW of the Sequencer output is used to compensate for the pipeline delay associated with the arithmetic processor.

TABLE 5. FFT ADDRESSING BY COMPUTATIONAL STAGE

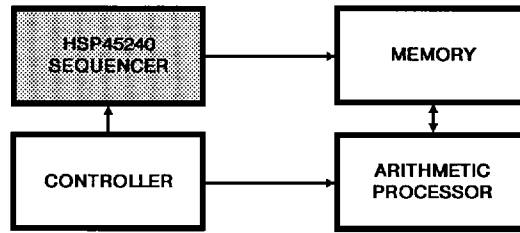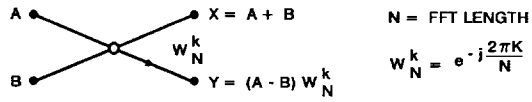| STAGE 1 R/W ADDR.	STAGE 2 R/W ADDR.	STAGE 3 R/W ADDR.	OUTPUT ADDRESSING
000	000	000	000
100	010	001	100
001	001	010	010
101	011	011	110
010	100	100	001
110	110	101	101
011	101	110	011
111	111	111	111
SWITCH MAPPING			
021	201	210	012

FIGURE 5. FFT PROCESSOR
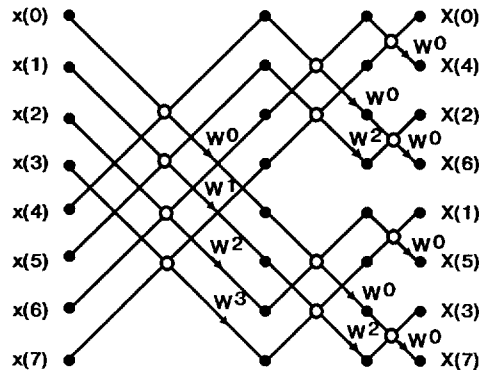

FIGURE 6. BUTTERFLY FOR DECIMATION-IN-FREQUENCY

FIGURE 7. COMPLETE EIGHT-POINT IN-PLACE DECIMATION-IN-FREQUENCY FFT

7

SPECIAL
FUNCTION

Absolute Maximum Ratings

Supply Voltage . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . GND−0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . −65°C to +150°C
Maximum Package Power Dissipation at +70°C . . . . 1.86W (PLCC), 2.84W (PGA)
θ_{jc} . . . . 15.1°C/W (PLCC), 10.1°C/W (PGA)
θ_{ja} . . . . 43.1°C/W (PLCC), 37.1°C/W (PGA)
Gate Count . . . . 8388 Gates
Junction Temperature . . . . +150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering, Ten Seconds) . . . . +300°C
ESD Classification . . . . Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . +5.0V ± 5%
Operating Temperature Range . . . . 0°C to +70°C

D.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	–	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	–	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	–	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	–	0.8	V	V_{CC} = 4.75V
Output HIGH Voltage	V_{OH}	2.6	–	V	I_{OH} = −400µA, V_{CC} = 4.75V
Output LOW Voltage	V_{OL}	–	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_I	−10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	−10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Power Supply Current	I_{CCSB}	–	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs open
Operating Power Supply Current	I_{CCOP}	–	99	mA	f = 33MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open, (Note 1)
Input Capacitance	C_{IN}	–	10	pF	f = 1MHz, V_{CC} = Open, all measurements are referenced to device GND. (Note 2).
Output Capacitance	C_O	–	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 3mA/MHz.

2. Not tested, but characterized at initial design and at major process/design changes.

A.C. Electrical Specifications (V_{CC} = 5.0V + 5%, T_A = 0°C to +70°C) (Note 2)

PARAMETER	SYMBOL	-33 (33MHz) MIN	-33 (33MHz) MAX	-40 (40MHz) MIN	-40 (40MHz) MAX	-50 (50MHz) MIN	-50 (50MHz) MAX	UNIT	TEST CONDITIONS
Clock Period	T_{CP}	30	-	25	-	20	-	ns	
Clock Pulse Width High	T_{CH}	12	-	10	-	9	-	ns	
Clock Pulse Width Low	T_{CL}	12	-	10	-	9	-	ns	
Setup Time D0-6 to WR# High	T_{DS}	14	-	13	-	12	-	ns	
Hold Time D0-6 from WR# High	T_{DH}	0	-	0	-	0	-	ns	
Set-up Time A0, CS#, to WR# Low	T_{AS}	5	-	5	-	5	-	ns	
Hold Time A0, CS#, from WR# High	T_{AH}	0	-	0	-	0	-	ns	
Pulse Width for WR# Low	T_{WRL}	13	-	12	-	10	-	ns	
Pulse Width for WR# High	T_{WRH}	13	-	12	-	10	-	ns	
WR# Cycle Time	T_{WP}	30	-	25	-	20	-	ns	
Set-up Time STARTIN#, DLYBLK, to Clock High	T_{IS}	12	-	10	-	8	-	ns	
Hold Time STARTIN#, DLYBLK, to Clock High	T_{IH}	0	-	0	-	0	-	ns	
Clock to Output Prop. Delay on OUT0-23	T_{PDO}	-	15	-	13	-	12	ns	
Clock to Output Prop. Delay on STARTOUT#, BLKDONE#, DONE#, ADDVAL#, and BUSY#	T_{PDS}	-	15	-	13	-	12	ns	
Output Enable Time	T_{EN}	-	20	-	15	-	13	ns	
Output Disable Time	T_{OD}	-	20	-	15	-	13	ns	Note 1
Output Rise/Fall Time	T_{ORF}	-	5	-	3	-	3	ns	Note 1
RST# Low Time	T_{RST}	2 Clock Cycles						ns	

NOTES:

1. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

2. A.C. Testing is performed as follows: Input levels (CLK Input) = 4.0V and 0V; Input levels (All other inputs) = 0V and 3.0V; Input timing reference levels: (CLK) = 2.0V, (Others) = 1.5V; Output timing references: $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$.
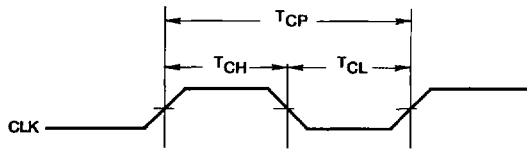
A.C. Test Load Circuit

OUTPUT PIN	C_L
BLOCKDONE# DONE# ADDVAL# STARTOUT# BUSY#	40pF
OUT0-23	100pF
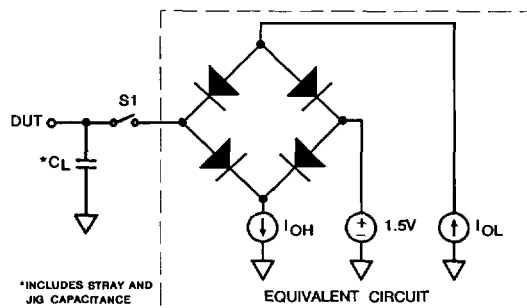
*INCLUDES STRAY AND JIG CAPACITANCE

EQUIVALENT CIRCUIT

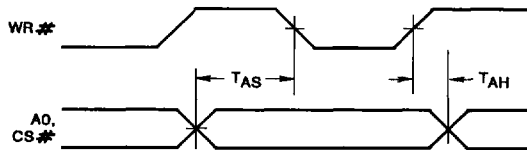*Test Head Capacitance
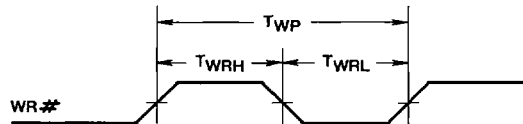Switch S1 Open for I_{CCSB} and I_{CCOP} Tests.

Timing Diagrams

CLOCK AC PARAMETERS
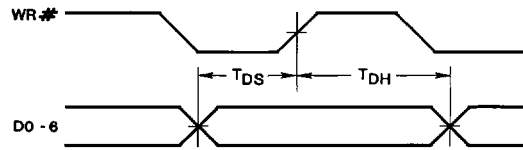
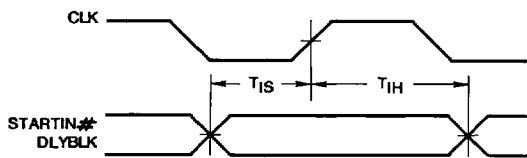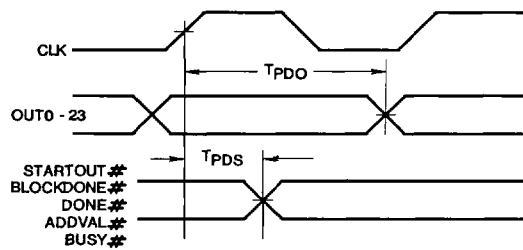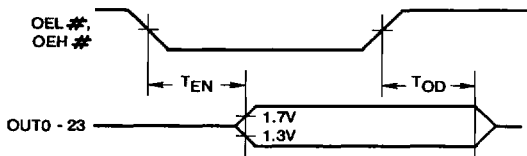DATA SETUP AND HOLD

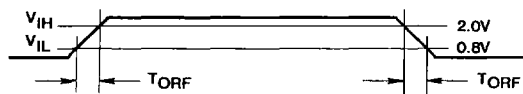ADDRESS/CHIP SELECT SETUP AND HOLD

WR# AC PARAMETERS

INPUT SETUP AND HOLD

OUTPUT PROPOGATION DELAY

OUTPUT ENABLE, DISABLE TIMING

OUTPUT RISE AND FALL TIMING