Am9520/Am9521/AmZ8065

Burst Error Processor

DISTINCTIVE CHARACTERISTICS

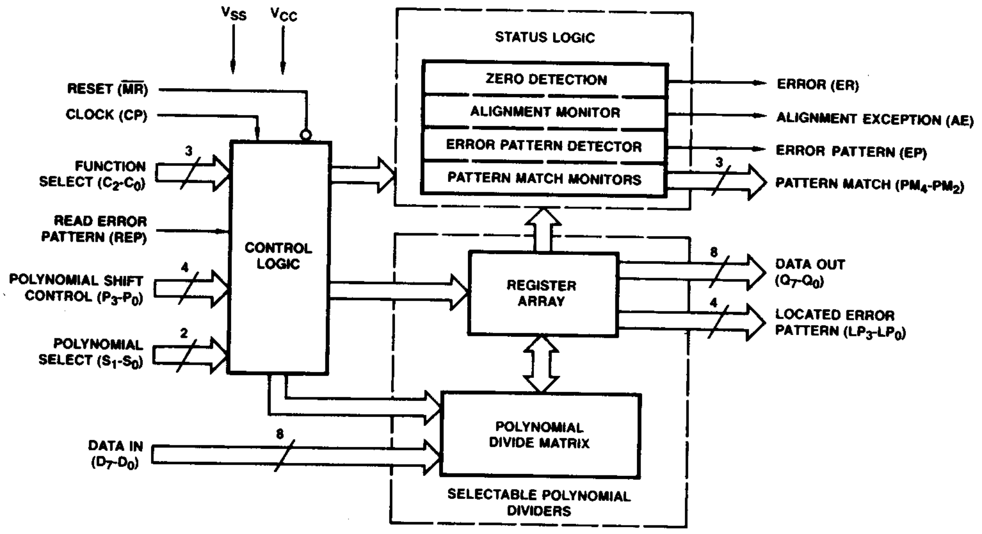
- **Provides for detection and correction of burst errors**
  Detects errors in serial data up to 585K bits long. Allows correction of error bursts of up to 12 bits.
- **High-Speed Operation**
  Effective data rates up to 20 Mbits/second for Am9520/Am9521/AmZ8065 and 30 Mbits/second for -1 versions. Fast enough for high-performance hard and soft disk systems.
- **Selectable Industry-Standard Polynomials**
  35-bit and 32-bit polynomials on Am9521. Am9520/AmZ8065 additionally has popular IBM 56-bit and 48-bit versions.
- **Three correction algorithms provide flexibility**
  !q j Full-period clock-around method for conforming to current practices. Chinese remainder theorem reduces correction time by orders of magnitude. Reciprocal polynomial makes correction possible with 48-bit code.
- **Designed for use in both microprogrammed and microprocessor disk controller systems**
  Device complements both AmZ8000 and Am2900 microprocessor families and can also be used with other microprocessors.

GENERAL DESCRIPTION

The Burst Error Processor (BEP) provides for error detection and correction for high-performance disk systems and other systems in which high-speed serial data transfer takes place. As data density and transfer rates increase in both hard and floppy disks and other storage media, error detection and correction become increasingly important. The BEP is an LSI circuit that facilitates the most common error detection and correction schemes accommodating data streams of up to 585K bits at up to 20M bits/second effective data rate.

The BEP provides a choice of four standard polynomials, including the popular 56-bit and 48-bit versions, to satisfy a broad range of applications. The device divides the data stream by the selected polynomial using the rules of algebra in polynomial fields. The resulting remainder is the check word, which is then appended to the data for writing on the disk as a record. When the record is read back, the BEP computes the syndrome for data validation. If an error is detected, the location and pattern of this burst in the data stream is determined for corrections.

BLOCK DIAGRAM



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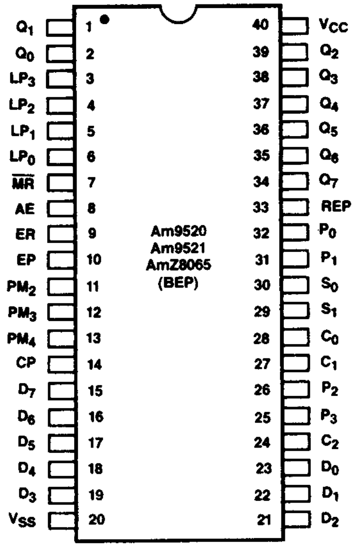
Refer to page 7-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-40



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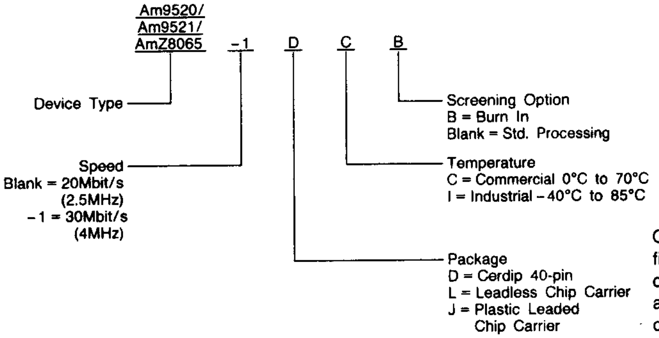
Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Device Type

Speed
Blank = 20Mbit/s
(2.5MHz)
-1 = 30Mbit/s
(4MHz)

Screening Option
B = Burn In
Blank = Std. Processing

Temperature
C = Commercial 0°C to 70°C
I = Industrial -40°C to 85°C

Package
D = Cerdip 40-pin
L = Leadless Chip Carrier
J = Plastic Leaded
Chip Carrier

Valid Combinations		
	20Mbit/s Data Rate	**30Mbit/s Data Rate**
Am9520/ Am9521/ AmZ8065/	DC, DCB, DI, DIB, LC, LCB, LI, LIB	-1DC, -1DCB, -1DI, -1DIB, -1LC, -1LCB, -1LI, -1LIB

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

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PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>40</td><td>V_{CC}</td><td></td><td>+5V Power Supply.</td></tr>
<tr><td>20</td><td>V_{SS}</td><td></td><td>Ground.</td></tr>
<tr><td>30,29</td><td>S_0-S_1</td><td>I</td><td>Polynomial Select. Logic levels on these two inputs select one of the four standard polynomials provided in the Am9520. The following table specifies the polynomial select codes.
<b>POLYNOMIAL SELECT CODES</b>
<table>
<tr><th>S_1</th><th>S_0</th><th>Polynomial</th><th>Number of Check Bits</th></tr>
<tr><td>L</td><td>L</td><td>$(X^{22}+1) \bullet (X^{11}+X^7+X^6+X+1) \bullet$
$(X^{12}+X^{11}+X^{10}+ \ldots +X+1) \bullet$
$(X^{11}+X^9+X^7+X^6+X^5+X+1)$</td><td>56</td></tr>
<tr><td>L</td><td>H</td><td>$(X^{21}+1) \bullet (X^{11}+X^2+1)$</td><td>32</td></tr>
<tr><td>H</td><td>L</td><td>$(X^{23}+1) \bullet$
$(X^{12}+X^{11}+X^8+X^7+X^3+X+1)$</td><td>35</td></tr>
<tr><td>H</td><td>H</td><td>$(X^{13}+1) \bullet$
$(X^{35}+X^{23}+X^8+X^2+1)$</td><td>48</td></tr>
</table></td></tr>
<tr><td>23,22
21,19
18,17
16,15</td><td>D_0-D_7</td><td>I</td><td>Data In. These eight inputs are used for entering information. D_0 is the least significant bit, and D_7 is the most significant bit position. HIGH on any input corresponds to 1, and LOW represents 0. Data entry occurs on the LOW-to-HIGH transition of the CP input. Any change on the D_0-D_7 inputs must take place only when the CP input is HIGH. See Timing diagram for details on set-up and hold time specifications.</td></tr>
<tr><td>28,27
24</td><td>C_0-C_2</td><td>I</td><td>Function Select. These three inputs specify the desired function according to the following table. Detailed description of each function is found in later sections of this document. Any change on the C_0-C_2 inputs must take place only when the CP input is HIGH. See Timing diagram for set-up and hold time specifications.
<b>FUNCTION SELECT CODES</b>
<table>
<tr><th>C_2</th><th>C_1</th><th>C_0</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Compute check bits</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Write check bits</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Read normal</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Read high speed</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Load</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Reserved</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Correct normal (Full period clock around)</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Correct high speed
(Chinese remainder theorem method)</td></tr>
</table></td></tr>
<tr><td>14</td><td>CP</td><td>I</td><td>Clock. Operations are controlled by this input. Outputs become valid after the LOW-to-HIGH transition on the CP input. The quiescent state of the CP input is HIGH. Any changes on the data and control inputs must take place only when the CP input is HIGH. See Timing diagrams for exact specifications. During operations, it may be required to stop the clock; the clock must be stopped in the HIGH state only. Also, note that requirements on the CP input during correction operations differ from those during other functions. See Timing diagram for details.</td></tr>
<tr><td>7</td><td>$\overline{MR}$</td><td>I</td><td>Master Reset. LOW on this input initializes the device. This input must remain LOW for a specified time to accomplish initialization before returning to the quiescent HIGH state. In general, the devices require initialization prior to performing Compute Check Bits, Read Normal, Read High Speed and Load functions.</td></tr>
<tr><td>2,1,39
38,37
36,35
34</td><td>Q_0-Q_7</td><td>O</td><td>Data Out (3-State). The check bits are made available on these eight outputs one byte at a time. Q_0 is the least significant bit position, and Q_7 is the most significant. HIGH on these outputs represents 1 and LOW 0.
The Q_0-Q_7 are active only during the following conditions:
a) The C_0-C_2 inputs specify Write Check Bits Function.
b) The REP input is HIGH.
During all other conditions Q_0-Q_7 are in a high-impedance state.</td></tr>
<tr><td>6,5
4,3</td><td>LP_0-LP_3</td><td>O</td><td>Located Error Pattern (3-state). The LP_0-LP_3 outputs together with the Q_0-Q_7 outputs provide the 12-bit error pattern in which Q_7 is the most significant bit and LP_0 is the least significant bit position. HIGH represents 1, and LOW represents 0. The REP input must be HIGH to read the error pattern. If the REP input is LOW, the LP_0-LP_3 outputs are in the high-impedance state.</td></tr>
<tr><td>33</td><td>REP</td><td>I</td><td>Read Error Pattern. A HIGH on this input activates the LP_0-LP_3 and Q_0-Q_7 outputs. This error pattern information is valid only after a HIGH is indicated on the EP output during correction operations.</td></tr>
<tr><td>9</td><td>ER</td><td>O</td><td>Error. HIGH on this output indicates that the BEP has detected an error. This output must be considered valid only after the last check byte during Read Normal or Read High Speed functions has been entered. The resulting syndrome is then contained in the register array. A non-zero syndrome indicates error; zero syndrome indicates no error. The ER output always reflects the state of this register array (zero or non-zero). The ER output is LOW after initialization.</td></tr>
</table>

PIN DESCRIPTION (Cont.)

Pin No.	Name	I/O	Description
10	EP	O	Error Pattern. HIGH on this output indicates that the error pattern has been found during the correction process. When the last check byte was entered during a Read function, the resulting syndrome is contained in the register array. The error pattern information is buried in this syndrome. To extract the error pattern, the BEP is clocked while the appropriate (Correct Normal or Correct High Speed) code is applied to the C_0-C_2 inputs until EP goes HIGH. The number of clocks required to find the error pattern is used to calucate where in the data stream the error has occurred. The EP output will be LOW after initialization by the $\overline{MR}$ input. The EP output is valid only during the correction operations and must be ignored at all other times. See Correct Normal and Correct High Speed under Detailed Description for further details.
11,12,13	PM_2-PM_4	O	Pattern Match. When using the Chinese remainder theorem for error correction, information is loaded into several feedback shift registers simultaneously. The number of registers is equal to the number of factors of the polynomial. After a high speed operation, there are as many syndromes as there are factors. For correction, the register corresponding to the first factor must be shifted until the EP output indicates HIGH. Then each register corresponding to the remaining factors must be shifted until a match occurs in each register with the error pattern contained in the first register. HIGH on PM_2, PM_3 or PM_4 outputs indicates that corresponding registers match. The PM_2 corresponds to the second factor, PM_3 corresponds to the third and PM_4 corresponds to the fourth factor. PM_3 corresponds to the third and PM_4 corresponds to the fourth factor. If a polynomial has only two factors, then PM_3 and PM_4 outputs have no meaning. Indications on the PM_2-PM_4 outputs must be considered valid only during high-speed correct function and should be ignored at all other times.
6,5,4,3	P_0-P_3	I	Polynomial Shift Control. Correction procedure using the Chinese remainder theorem method requires that each syndrome obtained from the High-Speed Read function be shifted individually. The P_0-P_3 inputs provide this capability: P_0 corresponds to the first factor, P_1 corresponds to the second factor and so on. HIGH on an input allows the corresponding register to shift and LOW causes it to hold. These inputs have an effect only during the Correct High-Speed function. Any change on these inputs must occur only when the CP input is HIGH.
8	AE	O	Alignment Exception. The devices use an 8-bit parallel mechanization of the feedback shift register configurations. Under certain conditions, the error pattern will not, therefore, automatically line up in predetermined positions of the register array during the correction operations. HIGH on the AE output indicates that such a condition is detected. The Am9520 automatically switches into the one-bit shift mode. The number of clocks for which the AE output is HIGH is used in the error location calculation. See Detailed Description for further details.

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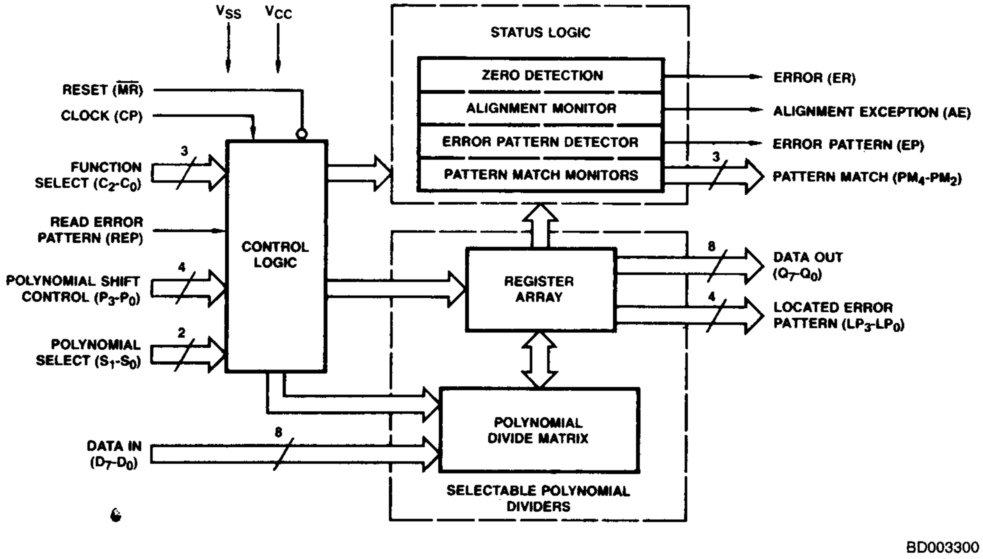

Figure 1. Am9520/Am9521/AmZ8065 Burst Error Processor

ARCHITECTURE

Figure 1 is a conceptual block diagram. It consists of four major sections – Register Array, Polynomial Divide Matrix, Status Logic and Control Logic.

Register Array

This section consists of 56 flip-flops used for check bit computation during write operation, syndrome computation during read operation and error pattern extraction during error correction operation. In general, the Polynomial Divide Matrix provides the bit patterns required for the Register Array. The combination of Register Array and Polynomial Divide Matrix mechanizes the familiar serial form of feedback shift register arrangement in an 8-bit parallel form. The Q_0–Q_7 outputs of the Am9520 are obtained from the Register Array. When correction operations are complete, the error pattern is available on 12 outputs: eight bits on the Q_0–Q_7 outputs and the remaining four bits on the LP_0–LP_3 outputs. The Read Error Pattern (REP) input must be HIGH for the error pattern to be available. The Control Logic generates Clock signals for the Register Array.

Status Logic

This section monitors the register arrays to generate the various error detection outputs of the BEP, including ER, AE, PM_2, PM_3, PM_4 and EP.

Polynomial Divide Matrix

Polynomial Divide Matrix is the heart of the BEP. The Control Logic decodes the Polynomial Select (S_0–S_1) and Function Select (C_0–C_2) inputs to generate the necessary gating signals to the matrix. The matrix establishes connections such that a byte of data presented on the D_0–D_7 inputs will be suitably divided by the selected generator polynomial. Four different polynomials are selected by logic levels on the S_0–S_1 inputs (Table 1).

These devices can be used in three fundamentally different types of operations: write, read and correct. The various functions are selected by the C_0–C_2 control inputs.

Write

While data is being written on the disk, the BEP is in the Compute Check Bits mode looking at the data bytes without affecting the flow of data to the disk. After the last data byte, the BEP is switched into the Write Check Bits function, outputting the 4, 5, 6 or 7 check bytes. This is the additional information appended to the data stream that allows the detection and correction of possible read errors.

Read

When information (data plus appended check bits) is being read, the BEP must be in either Read Normal mode or Read High Speed mode. These modes differ only in the correction algorithm that will be used if an error has occurred. In both modes parallel bytes are read into the device. After the last information byte has been entered, the ER output is checked. If it is LOW, there is no error; if it is HIGH, there is an error.

Correction

After the read operation, the syndrome held in the Register Array contains all the information necessary to find the error location and the error pattern, i.e., to allow error correction. In the Correct Normal mode, the error location is found by counting the number of clock pulses required to make the EP output go HIGH. The error pattern is then available on the LP_0–LP_3 and Q_0–Q_7 outputs and can be used to Exclusive OR with data.

In Correct High Speed mode, the error location is also found by counting clock pulses, but they are routed in succession to the different sections of the Register Array. This results in slightly more complicated but substantially faster operation.

TABLE 1. POLYNOMIALS

Polynominal	Number of Check Bits	Period (Bits)	Correctable Burst Error Length (Bits)
$(X^{22}+1)\cdot(X^{11}+7^{7}+X^{6}+X+1)\cdot$ $(X^{12}+X^{11}+X^{10}+\ldots+X+1)\cdot$ $(X^{11}+X^{9}+X^{7}+X^{6}+X^{5}+X+1)$	56	585,442	11
$(X^{21}+1)\cdot(X^{11}+X^{2}+1)$	32	42,987	11
$(X^{23}+1)\cdot(X^{12}+X^{11}+X^{8}+X^{7}+X^{3}+X+1)$	35	94,185	12
$(X^{13}+1)\cdot(X^{35}+X^{23}+X^{8}+X^{2}+1)$	48	$13\cdot(2^{35}-1)$	7

DETAILED DESCRIPTION

Compute Check Bits

The check bits to be appended to the data are computed using this function. The S_0–S_1 inputs select the desired polynomial. The Polynomial Matrix will be configured such that the generator polynomial is in the expanded form. The expanded form of a polynomial is obtained by multiplying out its factors and combining proper terms using modulo-2 arithmetic. Assume that the 32-bit polynomial is selected: the factored form of the 32-bit polynomial in Table 1 is $(X^{21}+1)$ $(X^{11}+X^{2}+1)$. The corresponding expanded form is $X^{32}+X^{23}+X^{21}+X^{11}+X^{2}+1$.

The sequence of events to compute the check bits is as follows:

1. The CP input is in quiescent HIGH state.
2. Initialize by activating the $\overline{MR}$ input LOW and return it to HIGH.
3. Through appropriate logic levels on the S_0–S_1 inputs, specify the desired polynomial. Also, select Compute Check Bits code through the C_0–C_2 inputs.
4. Establish a byte of data on the D_0–D_7 inputs.
5. Make CP input LOW and then HIGH. See timing diagram for detailed timing specifications.
6. Keep repeating from step 4 until all data bytes are entered.

Write Check Bits

In Compute Check Bits mode, the polynomial matrix and the Register Array are mechanizing a feedback shift register configuration. However, when Write Check Bits Code is established on the C_0–C_2 inputs, the feedback paths are disabled such that the Register Array will behave as a simple shift register. When the last data byte is entered in the Compute Check Bits mode, the Register Array holds the check bits. These check bits will be available on the Q_0–Q_7 outputs, one byte at a time.

The sequence of events to obtain the check bits is as follows:

1. The CP is in quiescent HIGH state.
2. Establish appropriate code on the S_0–S_1 inputs. This code must be the same as that used for Compute Check Bits function.
3. Establish Write Check Bits code on the C_0–C_2 inputs.
4. After a propagation delay, the Q_0–Q_7 outputs will contain the first check byte.
5. Make CP input LOW and then HIGH. The next check byte will be available on the Q_0–Q_7 outputs.
6. Keep repeating from step 5 until all check bytes that correspond to the selected polynomial are read out.

Read Normal

Two methodologies are available for error correction with these devices: (a) Full period clock around (normal method) and (b) Chinese remainder theorem (high-speed method). The Read Normal function must be used for reading data from the disk if the normal method is used for error correction. When Read Normal is selected, the Polynomial Matrix establishes the polynomial in the expanded form. In this mode, the input stream consisting of data and check bytes is divided by the selected polynomial to obtain the syndrome. If the resulting syndrome is not zero, an error is detected. The ER output indicates whether the syndrome is zero or not. HIGH on the ER output indicates non-zero syndrome.

The sequence of events for Read Normal is as follows:

1. The CP input is in quiescent HIGH state.
2. Initialize the Am9520 by activating the $\overline{MR}$ input LOW and then return it to HIGH.
3. Establish proper code on the S_0–S_1 inputs. The polynomial selected for the read operation must be the same as the one originally used for generating the check bits.
4. Establish Read Normal code on the C_0–C_2 inputs.
5. Present a byte of information read from the disk on the D_0–D_7 inputs.
6. Make the CP input LOW and then HIGH.
7. Keep repeating from step 5 until the last check byte read from the disk is processed.
8. After entering last check byte, test the ER output. HIGH on this output is indicative of an error and LOW means no error detected.

Read High Speed

This function must be used for reading data if the Chinese remainder theorem method is to be used for error correction. In general, the Chinese remainder method accomplishes error correction in fewer clock cycles than the normal method. This method of correction, however, is not available for the 48-bit polynomial due to the nature of the factors that make up this polynomial. As explained later, the reciprocal polynomial technique is used for error correction when the 48-bit polynomial is selected.

The only difference between Read Normal and Read-High Speed Modes is as follows: in the Read Normal, the input stream is divided by the expanded version of the polynomial; whereas, in the Read High-Speed Mode, the input stream is simultaneously divided by all factors of the polynomial. Thus, the high-speed mode results in as many syndromes as the number of factors of the polynomial. If all syndromes are zero after entering the last check byte, the ER output will be LOW, indicating error-free operation. If there was an error, the ER will be HIGH.

The sequence of events in this mode are as follows:

1. The CP input is in its quiescent HIGH state.
2. Specify the polynomial on the S_0–S_1 input. This must obviously be the same polynomial that generated the check bits originally.
3. Specify Read High-Speed function on the C_0–C_2 inputs.

4. Initialize by activating the $\overline{MR}$ input LOW and then return it to HIGH.
5. Present a byte read from the disk on the D_0–D_7 inputs.
6. Make the CP input LOW and then HIGH.
7. Keep repeating from step 5 until all data and check bytes are entered.
8. Test the ER output after entering the last check byte. HIGH on this output is indicative of an error, and LOW signifies no error.

Correct Normal

The syndrome obtained from Read Normal operation is manipulated to extract the error pattern as well as its location using the Correct Normal function. Of the four polynomials listed in Table 1, the 48-bit version requires a separate explanation. For all cases except the 48-bit version, the polynomial is established in the expanded form.

In the Correct Normal, the syndrome is repeatedly divided by the polynomial until the error pattern is located. This division is accomplished by repeated clocking while ignoring the D_0–D_7 inputs. HIGH on the EP output signifies that the error pattern is found. The error pattern is always characterized by a known number of consecutive zeros at specified Register Array locations. The exact number of zeros and their location is a function of the select polynomial. The status logic detects this unique combination to generate the EP output. The number of clock cycles needed to locate the error pattern is a measure of the error location. If the number of clock cycles has exceeded the natural period of the selected polynomial without finding the error pattern, then an uncorrectable error has occurred. The AE output must also be considered in the Correct Normal mode of operation.

The polynomial matrix is an 8-bit parallel mechanization of the familiar serial polynomial division scheme. Because of this, there are certain conditions under which the error pattern will not line up automatically. The Status Logic also monitors this condition. When such an alignment exception is detected, the AE output of the device goes HIGH.

Internally, the device switches automatically into the one-bit shift mode. Let R_1 be the number of clock cycles for the AE output to go HIGH. Let R_2 be the number of clock cycles from the AE output going High to the EP output going HIGH. Let N be the natural period of the selected polynomial. Then $N \bullet K - 8R_1 - R_2$ is the first bit in the error burst counting from the last check bit of the record, where K is the smallest positive integer to make this expression positive. If there is no alignment exception, then $R_2 = 0$. See Table 1 for periods of the polynomials.

The error pattern provided is used externally to correct the error. The error pattern is available on the Q_0–Q_7 and LP_0–LP_3 outputs when the REP input is HIGH. Q_7 corresponds to the first bit in error. When an error pattern bit is HIGH, then the corresponding bit in the data stream must be complemented to accomplish correction.

The Correct Normal discussed so far can be summarized by the following sequence of events.

1. The CP input is in the quiescent HIGH state.
2. The ER output is HIGH, indicating error from the previous Read Normal operation.
3. Select appropriate polynomial (S_0–S_1).
4. Select Correct Normal Code (C_0–C_2).
5. Let R_1 and R_2 be two external counters both initialized to zero.
6. Check if the EP output is HIGH. If HIGH, the error pattern is found. The error location is given by $L = N \cdot K - (8R_1 + R\ _2)$, except for the 35-bit polynomial where $L = N \cdot K - (8R_1 + R_2 + 5)$. ($R_2$ is always zero for this case.)
7. If the EP output is LOW, test the AE output. If the AE output is HIGH, make the CP input LOW and then HIGH. Increment R_2. If the AE output is LOW, make the CP input LOW and then HIGH. Increment R_1 instead.
8. If $R_1 + R_2$ is greater than N (N is the natural period of the selected polynomial), then an uncorrectable error occurred. Abort the correction process.
9. If the error is correctable, repeat from step 6.

The flowchart in Figure 2 explains the correction process.

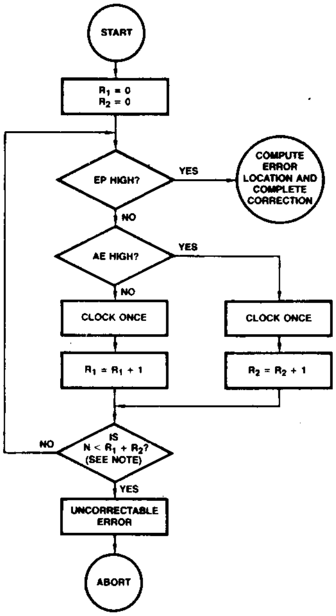

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Figure 2. Flowchart

Note: For the 48-bit polynomial, N = number of actual data bits + 48 check bits.

Now consider the Correct Normal Mode of operation with the 48-bit polynomial. The period of the 48-bit polynomial is so large that ordinary division is not practical. In this case the Polynomial Matrix establishes the reciprocal of the expanded polynomial. If G(X) is a polynomial of degree K, then its reciprocal $G^*(X) = X^K G(1/X)$. Because of this, the syndrome obtained using Read Normal Mode with the 48-bit polynomial is not used directly for extracting the error pattern and calculating its location. Instead, the reciprocal of the syndrome must be used.

The procedure for forming the reciprocal must be accomplished externally as follows. Assume that the Read Normal operation using the 48-bit polynomial was finished and an error was detected. Read out the syndrome using Write Check Bits function. Now reverse all these syndrome bits such that the previously most significant bit becomes the least significant bit and vice versa. The result is the reciprocal syndrome.

Now load this reciprocal syndrome into the device using the Load function (see description of Load). Once the reciprocal syndrome is loaded, Correct Normal function is established on the C_0–C_2 inputs, and the correction process can be started.

The actual correction process is exactly the same as before, except the error location in this case is given by $8R_1 + R_2 - 48$.

The sequence of events can be summarized as follows:

1. Read out the syndrome using the Write Check Bits function.
2. Form the reciprocal syndrome externally and enter it using the Load function.
3. The CP input is in its quiescent HIGH state.
4. Select the 48-bit polynomial on the S_0–S_1 inputs.
5. Select Correct Normal mode on the C_0–C_2 inputs.
6. Let R_1 and R_2 be two external counters initialized to zero.
7. Test EP output. If it is HIGH, error pattern has already been found. The error location is $8R_1 + R_2 - 48$.
8. If EP output is LOW, test the AE output. If AE is HIGH, make CP input LOW and then HIGH. Increment R_2. If the AE output is LOW, make the CP input LOW and then HIGH. Increment R_1.
9. If $R_1 + R_2 - 48$ is greater than the record length, the error is uncorrectable, so abort the correction process.
10. Keep repeating from step 7 until the error is located.

Correct High Speed

The maximum number of clock cycles needed to find the error pattern using the normal correction method is N where N is the period of the polynomial. Thus a polynomial with a large period may require a large number of clock cycles for error correction not acceptable in some applications. The BEP has facilities for high-speed correction using the Chinese remainder theorem method.

Let a polynomial consist of m factors with periods P_1, $P_2 ... P_m$. The period N of the composite polynomial is the product of the periods of the individual factors; i.e., $N = P_1 \bullet P_2 \bullet P_3 ... P_m$. If the Chinese remainder theorem is used for correction, the maximum number of clock cycles needed is $(P_1 + P_2 ... P_m)$. This number is usually much smaller than N. Thus, the Chinese remainder theorem method is faster than the normal method for error correction.

To employ the Chinese remainder theorem method, the syndromes must be obtained first using the Read High-Speed function. This function gives as many syndromes as the number of factors in the polynomial. In other words, the Register Array is divided into a number of sections; each section implementing one factor of the polynomial. The first factor of every polynomial is of the form $(X^C + 1)$. This factor is sometimes called the error pattern polynomial. The Chinese remainder theorem method requires that the syndrome obtained by the error pattern polynomial be repeatedly divided by the error pattern polynomial until the error pattern is found. This is done in a fashion similar to the Correct Normal method described before. The register section corresponding to the error pattern polynomial is repeatedly clocked. The error pattern is always characterized by a known number of consecutive zeros at predetermined bit positions. (There can be alignment exceptions while finding the error pattern, but for the purpose of this explanation, assume that alignment exceptions do not occur.)

After locating the error pattern, the error pattern register is prevented from clocking. Next, the register corresponding to the second factor is repeatedly clocked until it matches the error pattern and then this register is prevented from further clocking. This procedure is repeated for all remaining factors. As mentioned earlier, the P_0–P_3 inputs are provided to control clocking of the individual registers, and the PM_2–PM_4 outputs are provided to indicate matching of each register with the error pattern.

Let M_1 be the number of clock cycles required to find the error pattern and M_2, M_3, etc. be the number of clock cycles required to match subsequent factors as described above. The error location can then be computed by a formula of the form:

$$L = N \cdot K - (A_1M_1 + A_2M_2 + A_3M_3 + A_4 + ...).$$

Where A_1, A_2, etc. are predetermined constants for a given polynomial and K is the smallest integer that makes the right hand side of the equation positive, A_0, A_1 etc. are called Chinese remainder theorem coefficients. The number of coefficients equals the number of factors in the polynomial. Table 3 lists the coefficients for the polynomials. There is one additional adjustment for the 35-bit polynomial – the error location for this polynomial is computed by using the formula $L = N \cdot K - (A_1M_1 + A_2M_2 + 5)$. This modification is required because 35 bits are really five bytes with the last five bits being unused.

TABLE 2. POLYNOMIAL PERIODS

Polynomial	Period Factor 1	Period Factor 2	Period Factor 3	Period Factor 4	Composite Period (N)
56-Bit	22	13	89	23	585442
32-Bit	21	2047	–	–	42987
35-Bit	23	4095	–	–	94185

As in the normal method, every error detected may not necessarily be correctable. If the number of clock cycles to find the error pattern exceeds the period of the error pattern polynomial, or the number of clock cycles required to match a register exceeds the period of the polynomial corresponding to that register, the correction process must be aborted. Table 2 lists the applicable periods for polynomials.

TABLE 3. CHINESE REMAINDER THEOREM COEFFICIENTS

Polynomial	A_1	A_2	A_3	A_4
56-bit	452,387	2,521,904	578,864	2,647,216
32-bit	38,893	32,760	–	–
35-bit	4,095	720,728	–	–

The sequence of events is as follows:

1. The CP input is in the quiescent HIGH state. The ER output is HIGH indicating an error from the Read High Speed operations.
2. Select the polynomial using the S_0–S_1 inputs and specify Correct High Speed code on the C_0–C_2 inputs.
3. Set $P_1 = P_2 = P_3 =$ LOW, $P_0 =$ HIGH.
4. R_1 and R_2 are two external counters, initialized to zero.
5. Test the EP output. If the EP output is HIGH, error pattern is already found and $M_1 = 8R_1 + R_2$. Bring P_0 input LOW and go to step 10.
6. Establish HIGH on the P_0 input.
7. If the EP output is LOW, test the AE output. If the AE output is LOW, make the CP input LOW and then HIGH. Increment R_1. If the AE output is HIGH, make CP LOW and then HIGH. Increment R_2.
8. If $R_1 + R_2$ is greater than the period of the first factor, abort the correction process; the error is not correctable.
9. If the error is correctable, repeat from step 5.

10. Establish HIGH on the P_1 input.
11. M_2 is an external counter initialized to zero.
12. Test the PM_2 output. If the PM_2 output is HIGH, the second factor located the matching error pattern. Bring P_1 LOW and go to step 16.
13 If the PM_2 output is LOW, make the CP input LOW and then HIGH. Increment M_2.
14 If M_2 is greater than the period of the second factor, abort the correction process; the error is not correctable.
15. If the error is correctable, repeat from step 12.

The following additional steps are performed only for the 56-bit polynomial. In case of the 32-bit or 35-bit polynomial, proceed with computations for error location.

16. Establish HIGH on the P_2 input.
17. M_3 is an external counter initialized to zero.
18. Test the PM_3 output. If it is HIGH, the third factor located the matching error pattern. Bring P_2 input back LOW and go to step 22.
19. If the PM_3 output is LOW, make the CP input LOW and then HIGH. Increment M_3.
20. If M_3 is greater than the period of the third factor, abort the correction process; the error is not correctable.
21. If the error is correctable, repeat from step 18.
22. Establish HIGH on the P_3 input.
23. M_4 is an external counter initialized to zero.
24. Test the PM_4 output. If it is HIGH, the matching error pattern is found by the fourth factor. Compute the error location.
25. If the PM_4 output is LOW, make CP input LOW and then HIGH. Increment M_4. If M_4 is greater than the period of the fourth factor, abort the correction process; the error is not correctable.
26. If the error is correctable, repeat from step 24.

The following flowchart (Figure 3) summarizes the Correct High Speed function.

Load

This function enters the reciprocal of the syndrome into the Am9520. In the case of the 48-bit polynomial, the reciprocal of the syndrome must be formed externally and then entered into the Am9520 before error correction can start.

When the Load function is selected, the Register Array is configured as a simple 8-bit wide 7 deep shift register. The $D_0 - D_7$ are the inputs to this shift register. Before starting the correction process, seven bytes must be shifted in using the Load function – the first six bytes are the reciprocal of the syndrome, and the last byte is an all-zero fill byte.

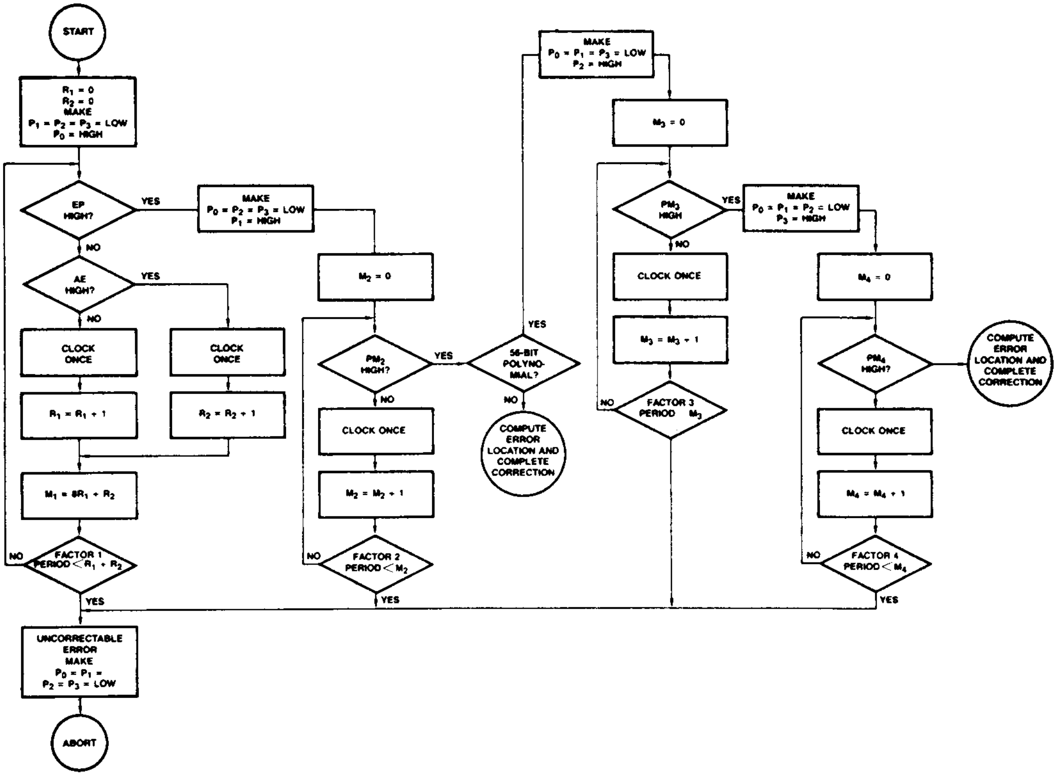

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Figure 3. Correct High-Speed Function

The sequence of events for accomplishing the Load function is as follows:

1. The CP input is in its quiescent HIGH state.
2. Select 48-bit polynomial on the S_0–S_1 inputs.
3. Select Load function on the C_0–C_2 inputs.
4. Set $\overline{MR}$ LOW, and then HIGH.
5. Present a byte to be loaded on the D_0–D_7 inputs.
6. Make CP input LOW and then HIGH.
7. Repeat from step 5 until all six bytes of the reciprocal are entered.
8. Make D_0–D_7 input LOW for the all-zero dummy fill byte.
9. Make CP input LOW and then HIGH.

Error Pattern Information

The discussion of Correct Normal and Correct High Speed functions described the procedure for finding the error pattern and calculating the location of the error burst. The devices provide the error pattern on 12 outputs – eight bits on the Q_0–Q_7 outputs and four bits on the LP_0–LP_3 outputs. It was also mentioned that the REP input must be HIGH to read the error pattern.

The error location calculated using the formulas given is always in number of bits. In case of 56-bit, 35-bit and 32-bit polynomials, the calculated error location value corresponds to the beginning of the error burst counting from the last check bit. The calculated error location is such that when 12 consecutive bits of the record are exclusive ORed into the error pattern, then the error burst is corrected (see Figure 4).

Figure 5 depicts error pattern information for the 48-bit polynomial. In this case, the computed error location refers in bits to the first bit in the burst. However, the burst goes towards the beginning of the data. In the case of 56-, 32- and 35-bit, the burst was towards the check bits. This difference is caused by using the reciprocal of the syndrome.

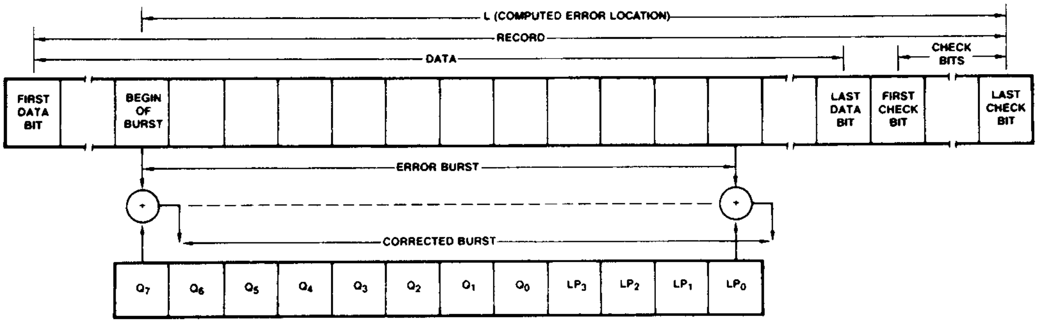

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Figure 4. Error Pattern Format for 56-Bit, 35-Bit and 32-Bit Polynomials

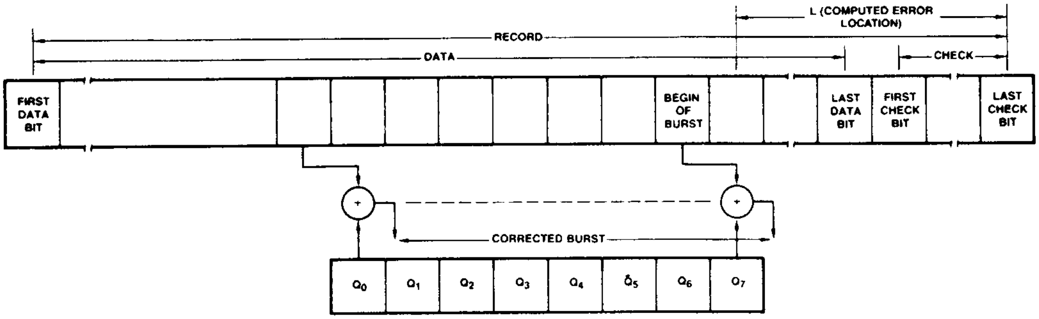

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Figure 5. Error Pattern Format for 48-Bit Polynomial

TYPICAL APPLICATION DIAGRAM

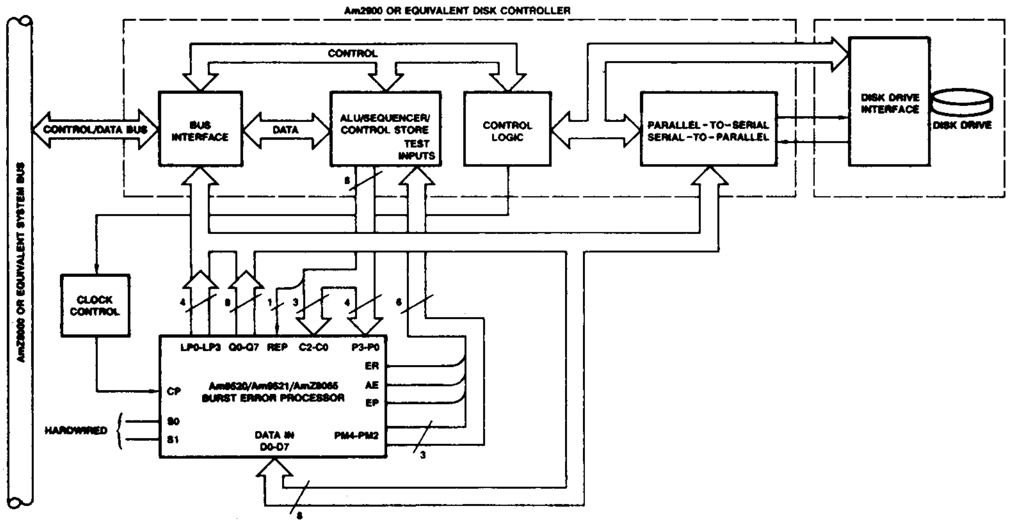

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Figure 6. Am9520/Am9521/AmZ8065 Burst Error Processor

APPLICATIONS

The BEP is designed for use in both microprogrammed and microprocessor disk controller systems. Figure 6 shows the BEP interfacing to an Am2900 bipolar bit-slice microprogrammed disk controller. The BEP can be interfaced to microprocessor-driven disk controller systems as well.

The controller in these designs would implement the control and clocking signals for the BEP necessary to execute the write, read and correction functions for a given polynomial selection. The operational flow for the methods available is shown in Figure 7.

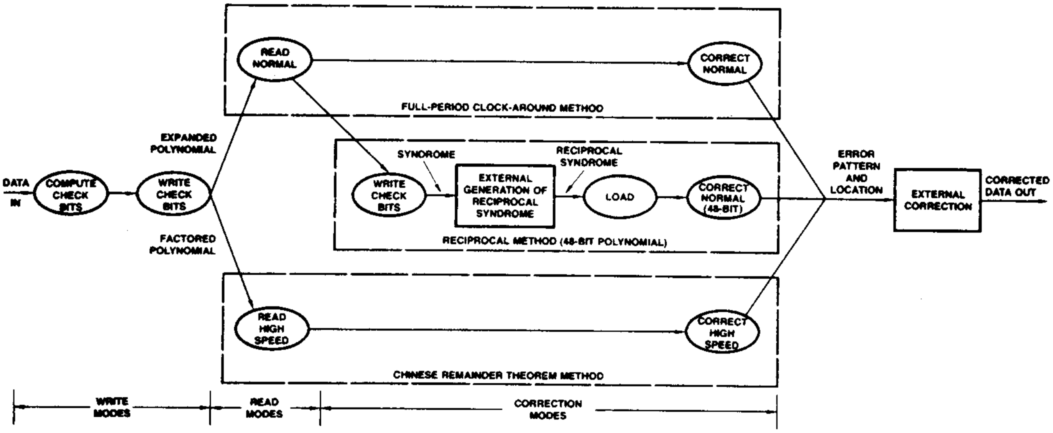

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Figure 7. BEP Operational Flow Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Voltage at any pin relative to V_{SS} .... −0.5 to +7.0V
Power Dissipation 1.5W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Grade	T_A	V_{CC}	V_{SS}
Commercial	0°C to 70°C	5V ±5%	0V
Industrial	−40°C to 85°C	5V ±10%	0V

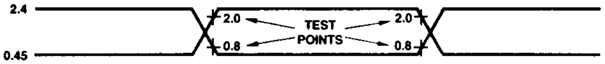
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input LOW Voltage		−0.5		+.8	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA			0.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −400μA	2.4			Volts
I_{OL}	Output Leakage Current	V_{OUT} = 0.4V			10	μA
I_{LOH}	Output Leakage Current	V_{OUT} = V_{CC}			10	μA
C_{IN}	Input Capacitance				15	pF
$C_{I/O}$	I/O Capacitance				25	pF
I_{LL}	Input Leakage Current				±10	μA
I_{CC}	Power Supply Current				275	mA

Note 1. Typical values apply at T_A = 25°C and V_{CC} = 5.0V. See table above for Operating Ranges.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



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Am9520/Am9521/AmZ8065 SWITCHING CHARACTERISTICS

The table below specifies the guaranteed performance of this device over the commercial operating range of 0 to +70°C with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds. Switching tests are made with inputs and outputs measured at 0.8V for a LOW and 2.0V for a HIGH. Outputs are fully loaded with $C_L \geqslant 50pF$. See Switching Waveform figures for graphic illustration of timing parameters.

SWITCHING CHARACTERISTICS

			Am9520 Am9521 AmZ8065		Am9520-1 Am9521-1 AmZ8065-1		
Number	**Parameters**	**Description**	**Min**	**Max**	**Min**	**Max**	**Units**
1	TWCPL	CP Width LOW	180		105		ns
2	TCYCP	CP Cycle Time	400		250		ns
3	TWCPH	CP Width HIGH	180		105		ns
4	TWMRL	$\overline{MR}$ Width LOW	800		500		ns
5	TREC	$\overline{MR}$↑ to CP↓ Time (Recovery)	250		250		ns
6	TSDCP	D_0-D_7 to CP↑ Setup Time	350		200		ns
7	THDCP	CP↑ to D_0-D_7 Hold Time	0		0		ns
8	TSCCP	C_0-C_2 or S_0-S_1 to CP↑ Setup Time	400		200		ns
9	THCCP	CP↑ to C_0-C_2, S_0-S_1, P_0-P_3 Hold time	0		0		ns
10	TSCCPL	C_0-C_2 or S_0-S_1 to CP↓ Setup Time	180		95		ns
11	TVCQ	C_0-C_2, S_0-S_1 to Q_0-Q_7 Valid Delay		200		150	ns
12	TIVCPQ	CP↑ to Q_0-Q_7 Invalid Delay	0		0		ns
13	TVCPQ	CP↑ to Q_0-Q_7 Valid Delay		200		150	ns
14	TIVCQ	C_0-C_2 to Q_0-Q_7 Three-State Delay		100		100	ns
15	TMRERL	$\overline{MR}$↓ to ER↓ Delay		200		200	ns
16	TCPER	CP↑ to ER Valid Delay		200		200	ns
17	TWCPCL	CP Width $\overline{LOW}$ for Correct Functions	450		450		ns
18	TWCPCH	CP Width $\overline{HIGH}$ for Correct Functions	450		450		ns
19	TCYCPC	CP Cycle Time for Correct Functions	1000		1000		ns
20	TCEP	C_0-C_2 to EP or AE Valid Delay		250		250	ns
21	TCPEP	CP↓ to EP, AE, or PM_2-PM_4 Valid Delay		400		400	ns
22	TSCPS	P_0, P_1, P_2, P_3 to CP↓ Setup Time	400		400		ns
23	TCEP	P_0 to EP or AE Delay		250		250	ns
24	TCPC	C_0-C_2, S_0-S_1 to CP↓ Setup Time for Correct Functions	400		400		ns
25	TPPM	P_1, P_2, P_3 to Corresponding PM Output Delay		250		250	ns
26	TCPEPI	CP↓ to EP, AE, PM_2, PM_3, and PM_4 Invalid Delay	0		0		ns
27	TPEPI	P_0↓ to EP, AE Invalid Delay	0		0		ns
28	TWREP	REP Pulse Width $\overline{HIGH}$	250		250		ns
29	TREPQ	REP↑ to Q_0-Q_7 and LP_0-LP_3 Delay		150		150	ns
30	TREPQI	REP↓ to Q_0-Q_7 and LP_0-LP_3 Three-State Delay		100		100	ns
31	TPPM	P_1, P_2, P_3↓ to PM_2, PM_3, PM_4 Invalid	0		0		ns
32	TCPM	C_0-C_2 to EP, AE, PM_2-PM_4 Invalid	0		0		ns

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SWITCHING WAVEFORMS

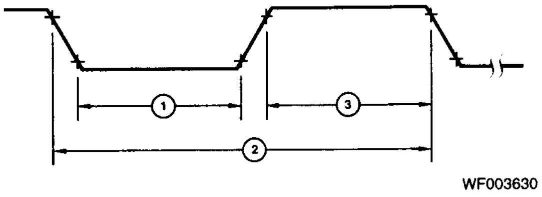

Figure 8. Clock Waveform for All Functions Except Correct Normal or Correct High-Speed

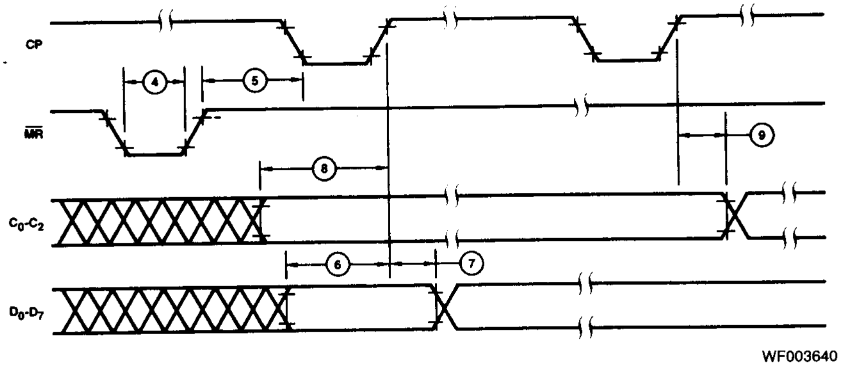

Figure 9. Timing for Compute Check Bits or Load Function

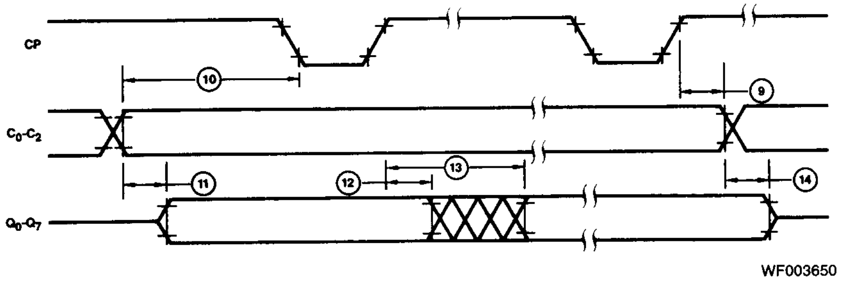

Figure 10. Timing for Write Check Bits Function

Notes: 1. REP input assumed low.

2. Q_0–Q_7 outputs will be high impedance if C_0–C_2 inputs do not specify Write Check Bits function.

SWITCHING WAVEFORMS (Cont.)

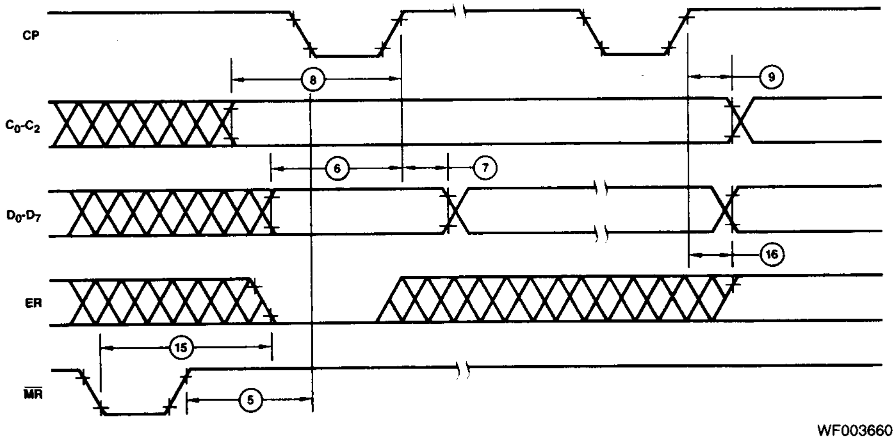

Figure 11. Timing for Read Normal or Read High-Speed Function
Note: ER output is a function of the contents in the register array flip-flops.

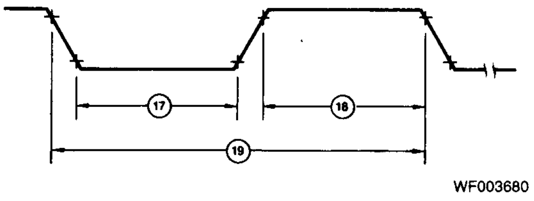

Figure 12. Clock Waveform for Correct Normal or Correct High-Speed Functions

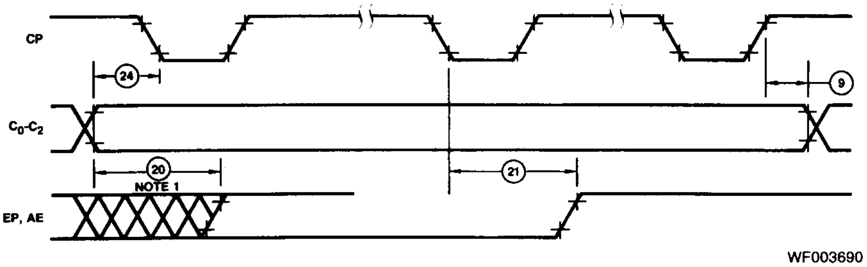

Figure 13. Timing for Correct Normal Function
Note 1: Assumes AE or EP output becomes active without any clocking.

SWITCHING WAVEFORMS (Cont.)

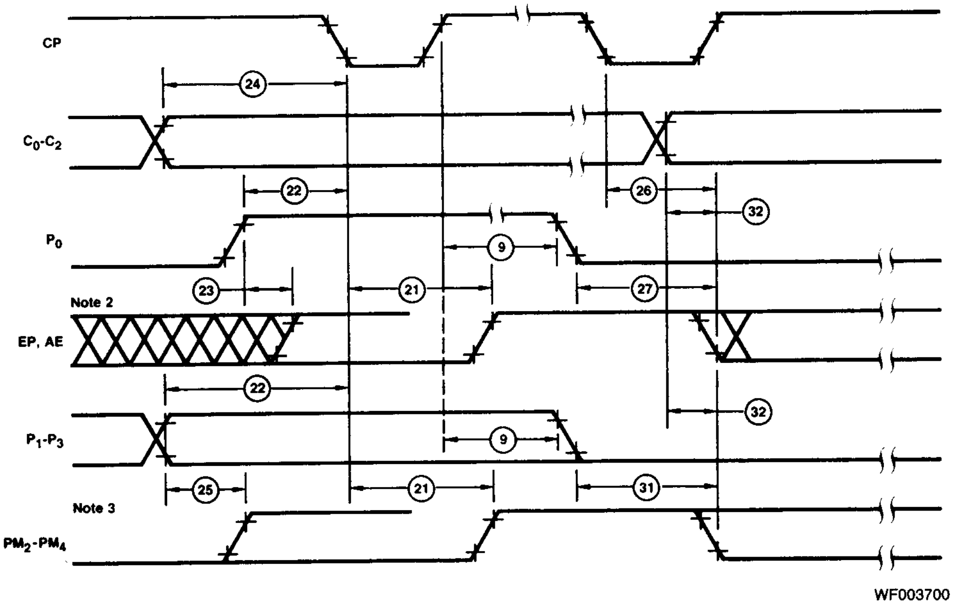

Figure 14. Timing for Correct High-Speed Function

Note 2: Assumes EP, AE becomes active without clocking.
Note 3: Assumes corresponding PM output becomes active without clocking.

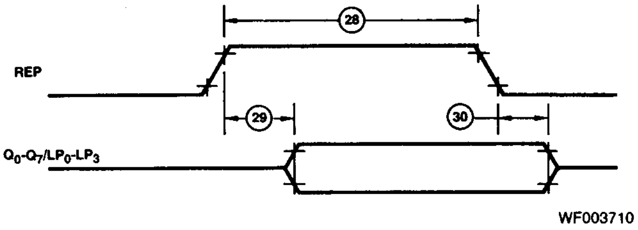

Figure 15. Read Error Pattern Timing