Am2904

Status and Shift Control Unit

- add ×C
- take off P & note "added from P/L)

DISTINCTIVE CHARACTERISTICS

- **Replaces most MSI used around any ALU**
  - Including the Am2901, Am2903A, Am29203 and MSI ALUs.
- **Generates Carry-in to the ALU**
  - Carry signal is selectable from 7 different sources.
- **Contains shift linkage multiplexers**
  - Connects to shift lines at the ends of an Am2901, Am2903A, or Am29203 array to implement single and double length arithmetic and logical shifts and rotates — 32 different modes in all.

- **Contains two edge-triggered status registers**
  - Use for foreground/background registers in controllers or as microlevel and machine level status registers. Bit manipulating instructions are provided.
- **Condition Code Multiplexer on chip**
  - Single cycle tests for any of 16 different conditions. Tests can be performed on either of the two status registers or directly on the ALU output.

GENERAL DESCRIPTION

The Am2904 is designed to perform all the miscellaneous functions which are usually performed in MSI around an ALU. These include the generation of the carry-in signal to the ALU and carry lookahead unit; the interconnection of the data path, auxiliary register, and carry flip-flop during shift operations; and the storage and testing of ALU status flags. These tasks are accomplished in the Am2904 by three nearly independent blocks of logic. The carry-in is

generated by a multiplexer. The shift linkages are established by four three-state multiplexers. There are two registers for storing the carry, overflow, zero, and negative status flags. The condition code multiplexer on the Am2904 can look at true or complement of any of the four status bits and certain combinations of status bits from either of the two storage registers or directly from the ALU.

SIMPLIFIED BLOCK DIAGRAM
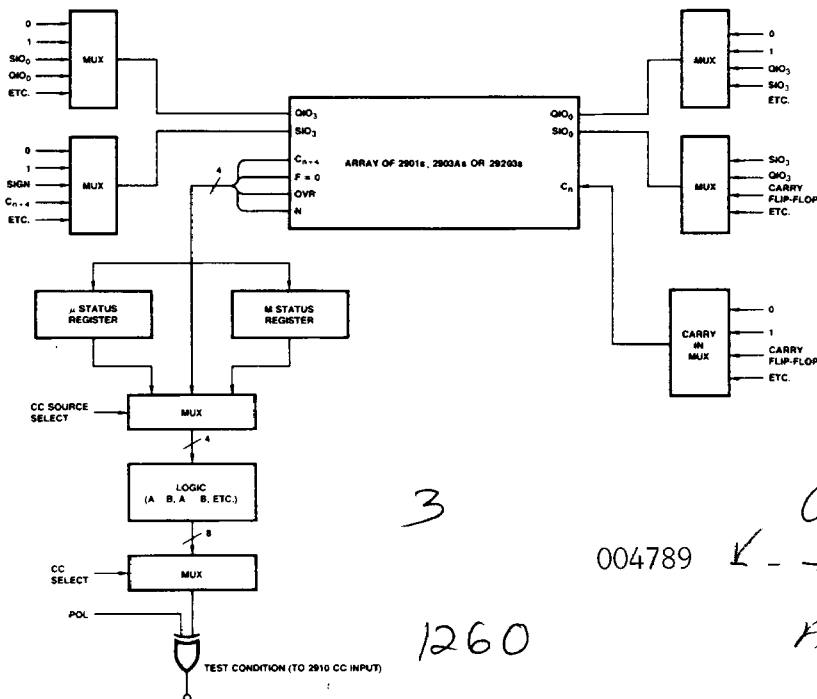
BASIC FEATURES OF Am2904

All the logic shown except the array of 2901s, 2903As, or 29203s is contained in the Am2904.

BD001853

3

004789 *Orig*

1260 *Amp*

RELATED AMD PRODUCTS

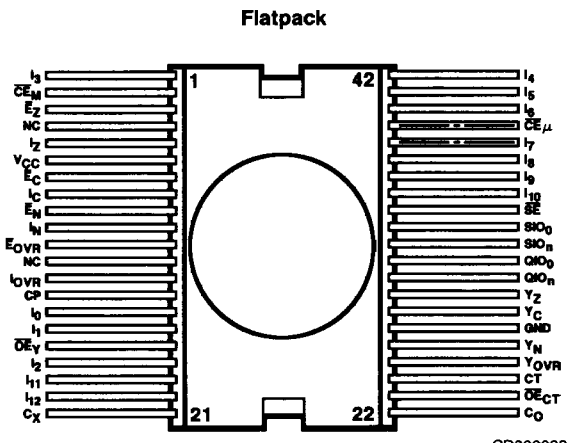| Part No.	Description
Am2901	4-Bit Microprocessor Slice
Am2903A	Advanced 4-Bit Bipolar Microprocessor Slice
Am29203	4-Bit Bipolar Microprocessor Slice
Am2910A	Microprogram Controller
Am29811	Next Address Control Unit for 2909A/11A

For additional applications refer to Chapter 4 of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

CONNECTION DIAGRAMS
Top View

DIP

|			
I_7	1 ●	40	I_8
$\overline{CE}_\mu$	2	39	I_9
I_6	3	38	I_{10}
I_5	4	37	SE
I_4	5	36	SIO_0
I_3	6	35	SIO_n
$\overline{CE}_M$	7	34	QIO_0
$\overline{E}_Z$	8	33	QIO_n
I_Z	9	32	Y_Z
V_{CC}	10	31	Y_C
$\overline{E}_C$	11	30	GND
I_C	12	29	Y_N
E_N	13	28	Y_{OVR}
I_N	14	27	CT
$\overline{E}_{OVR}$	15	26	$\overline{OE}_{CT}$
I_{OVR}	16	25	C_0
CP	17	24	C_X
I_0	18	23	I_{12}
I_1	19	22	I_{11}
$\overline{OE}_Y$	20	21	I_2

CD004131

Flatpack

I_3			I_4
$\overline{CE}_M$			I_5
$\overline{E}_Z$			I_6
NC	1	42	$\overline{CE}_\mu$
I_Z			I_7
V_{CC}			I_8
$\overline{E}_C$			I_9
I_C			I_{10}
E_N			SE
I_N			SIO_0
$\overline{E}_{OVR}$			SIO_n
NC			QIO_0
I_{OVR}			QIO_n
CP			Y_Z
I_0			Y_C
I_1			GND
$\overline{OE}_Y$			Y_N
I_2			Y_{OVR}
I_{11}			CT
I_{12}	21	22	$\overline{OE}_{CT}$
C_X			C_0
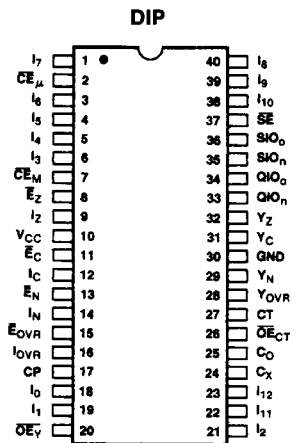
CD008033

Note: Pin 1 is marked for orientation.

NC = No Connection.

LOGIC SYMBOL
(DIP)

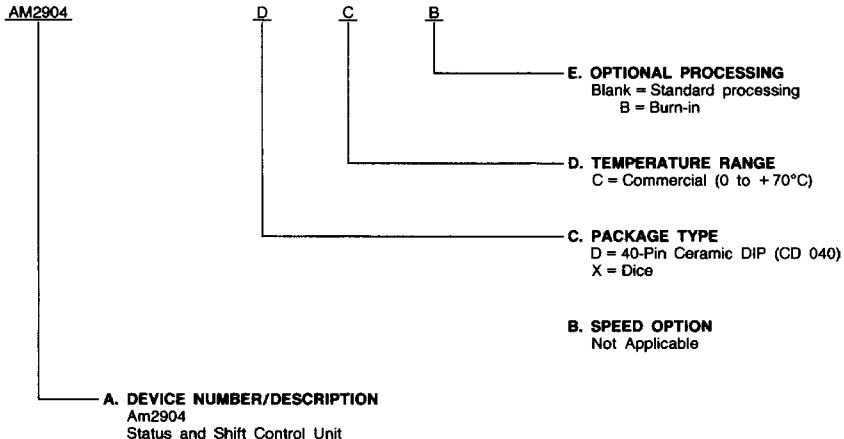Am2904
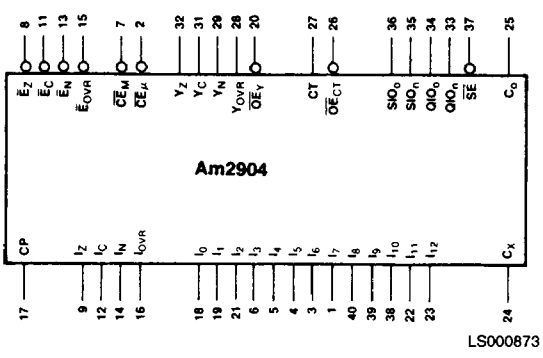
LS000873

METALLIZATION AND PAD LAYOUT
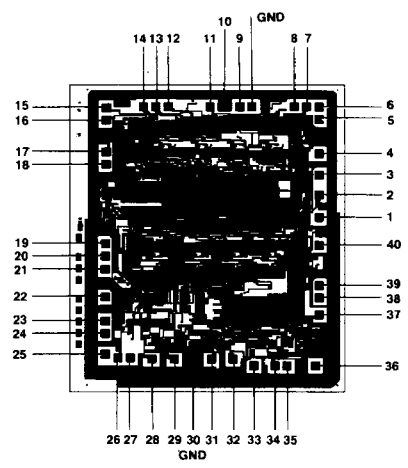
DIE SIZE 0.140″ x 0.161″
Pad Numbers correspond to DIP pinout

3

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
                           B. Speed Option (if applicable)
                           C. Package Type
                           D. Temperature Range
                           E. Optional Processing

AM2904   D   C   B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
D = 40-Pin Ceramic DIP (CD 040)
X = Dice

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am2904
Status and Shift Control Unit

Valid Combinations	
AM2904	DC, DCB, XC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.
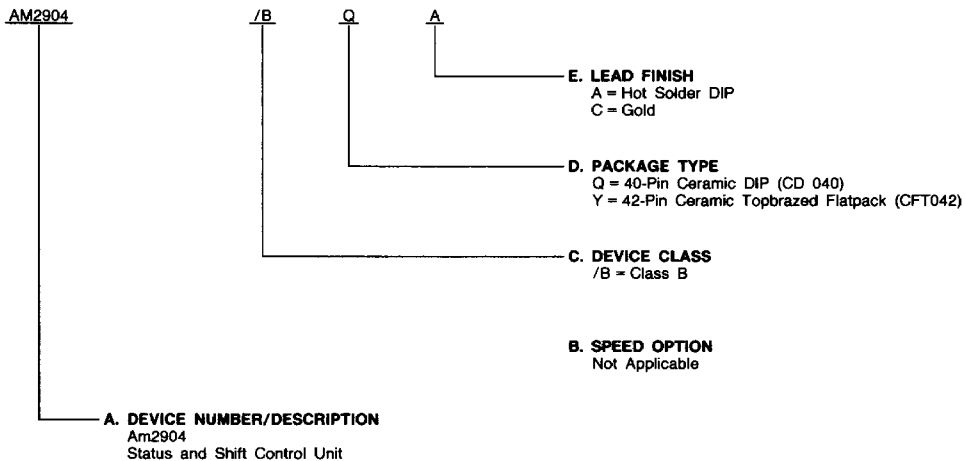
ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

          B. Speed Option (if applicable)
          C. Device Class
          D. Package Type
          E. Lead Finish

```
AM2904            /B    Q    A
```

E. LEAD FINISH
A = Hot Solder DIP
C = Gold

D. PACKAGE TYPE
Q = 40-Pin Ceramic DIP (CD 040)
Y = 42-Pin Ceramic Topbrazed Flatpack (CFT042)

C. DEVICE CLASS
/B = Class B

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am2904
Status and Shift Control Unit

Valid Combinations	
AM2904	/BQA, /BYC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

PIN DESCRIPTION

$\overline{CE}_M$ **Machine Status Register Enable (Input; Active LOW)**

This pin, used in conjunction with $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, and $\overline{E}_{OVR}$, acts as the overall enable for the Machine Status Register (MSR). When this pin is LOW, MSR bits may be modified, according to the states of $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, and $\overline{E}_{OVR}$. When HIGH, the MSR will retain the present state, regardless of the state of $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, and $\overline{E}_{OVR}$.

$\overline{CE}\mu$ **Micro Status Register Enable (Input; Active LOW)**

This pin, when LOW, enables all four bits of the Micro Status Register (μSR). When this pin is HIGH, the μSR will not change state.

C_O **Carry Multiplexer Out (Output)**

This is the output of the Carry-In Control Multiplexer. It connects to the C_n input of the least significant ALU slice, and the C_n input of the Am2902A.

CP **Clock Pulse (Input)**

The clock input to the device. The μSR and MSR are modified on the LOW-to-HIGH transition of the clock input. All other portions of the Am2904 are combinational and are unaffected by CP.

CT **Conditional Test (Output)**

The output of the Condition Code Multiplexer appears here.

C_X **Carry Multiplexer In (Input)**

This pin is used as an input to the Carry-In Control Multiplexer and can route it to the C_O pin. The C_X pin is intended for connection to the Z output of the Am2903A to facilitate some of the Am2903A special instructions.

$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, and $\overline{E}_{OVR}$ **Zero, Carry, Sign, and Overflow Status Enable (Input; Active LOW)**

These pins, when LOW, enable the corresponding bits in the MSR. When HIGH, they will prevent the corresponding bits from changing state. By using these pins together with the $\overline{CE}_M$ pin, MSR bits can be selectively modified.

$I_0 - I_{12}$ **Instruction Pins (Input)**

The thirteen instruction pins that select the operation the Am2904 is to perform.

I_C **Carry Status (Input)**

Intended for connection to the C_{n+4} output of the most significant ALU slice.

I_{OVR} **Overflow Status (Input)**

Intended for connection to the OVR pin on the most significant ALU slice.

I_N **Sign Status (Input)**

Intended for connection to the most significant ALU slice. The connection is to the N pin on the Am2903A, and the F_3 pin on the Am2901.

I_Z **Zero Status (Input)**

Intended for connection to the Z outputs of the Am2903A or the F = 0 outputs of the Am2901.

$\overline{OE}_{CT}$ **CT Output Enable (Input; Active LOW)**

When this pin is LOW, the CT pin is active. When HIGH the CT pin is in the high-impedance state.

$\overline{OE}_Y$ **Y Output Enable (Input; Active LOW)**

When LOW, this pin enables the Y pins as outputs. When HIGH, the Y outputs are in the high-impedance state.

$\overline{SE}$ **Shift Enable (Input; Active LOW)**

This pin controls the state of the shift outputs. When LOW, the shift outputs are enabled. When HIGH, the shift outputs are in the high-impedance state.

SIO_0, SIO_n, QIO_0, QIO_n **Serial Shift (Input/Output)**

These pins complete the linking for the various shift and rotate conditions. SIO_0 is intended for connection to the SIO_0 pin of the least significant Am2903A slice (RAM_0 for Am2901). SIO_n connects to the SIO_3 pin of the most significant Am2903A slice (RAM_3 for Am2901). QIO_0 connects to the QIO_0 pin of the least significant Am2903A slice (QIO_0 for Am2901) and QIO_n connects to the QIO_3 pin of the most significant Am2903A slice (Q_3 for Am2901).

Y_Z, Y_C, Y_N, and Y_{OVR} **Zero, Carry, Negative and Overflow Status (Input/Output; Three State)**

These pins form a three-state bidirectional bus over which MSR and μSR status can be read out or the MSR can be loaded in parallel.

FUNCTIONAL DESCRIPTION

Am2904 Architecture

The Am2904 Status and Shift Control Unit provides four functions which are included in all processors. These are: a) Status Register, b) Condition Code Multiplexer, c) Shift Linkages and d) Carry-in Control. The architecture and instruction codes have been designed to complement the flexibility of the 2900 Family.

Status Register

The Am2904 contains two four-bit registers which can store the status outputs of an ALU: Carry (C), Negative (N), Zero (Z), and Overflow (OVR). They are designated Micro Status Register (μSR) and Machine Status Register (MSR). Each register can be independently controlled. The registers use edge-triggered D-type flip-flops which change state on the LOW to HIGH transition of the Clock Input.

The μSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}) or from the MSR under instruction control (I_{0-5}). The bits in the μSR can also be individually set or reset under instruction control (I_{0-5}). When the $\overline{CE}\mu$ input is HIGH, the μSR is inhibited from changing, independent of the I_{0-5} inputs.

The MSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}), from the μSR, and from the four parallel input/output pins (Y_C, Y_N, Y_Z, Y_{OVR}) under instruction control (I_{0-5}). The MSR can also be set, reset or complemented under instruction control (I_{0-5}). The bits in the MSR can be selectively updated by controlling the four bit-enable inputs ($\overline{E}_Z$, $\overline{E}_N$, $\overline{E}_C$, $\overline{E}_{OVR}$) and the $\overline{CE}_M$ input. A LOW on both the $\overline{CE}_M$ input and the bit enable input for a specific bit enables updating that bit. A HIGH on a given bit enable input prevents the corresponding bit changing in the MSR. A HIGH on $\overline{CE}_M$ prevents any bits changing in the MSR.

The four parallel bidirectional input/output pins (Y_Z, Y_N, Y_C, Y_{OVR}) allow the contents of both the μSR and the MSR to be transferred to the system data bus and also allows the MSR to be loaded from the system data bus. This capability is used to save and restore the status registers during certain subroutines and when servicing interrupts.

Condition Code Multiplexer

The Condition Code Multiplexer output, CT, can be selected from 16 different functions. These include the true and complemented state of each of the status bits and combinations of these bits to detect such conditions as "greater than", "greater than or equal to", "less than" or "less than or equal to" for unsigned or two's complement numbers.

The Am2904 can perform these tests on the contents of the μSR, the MSR or the direct status inputs, (I_Z, I_N, I_C, I_{OVR}). The CT output is used as the test ($\overline{CC}$) input of the Am2910A and is provided with an output enable, $\overline{OE}_{CT}$ to make the addition of other condition inputs to this point easy.

Shift Linkage Multiplexer

The Shift Linkage Multiplexer generates the necessary linkages to allow the ALU to perform 32 different shift and rotate functions. Both single length and double length shifts and rotates, with and without carry (M_C), are provided. When the $\overline{SE}$ input is HIGH, the four input/output pins (SIO_0, SIO_n,

QIO_0, QIO_n) are disabled. The SIO_0, SIO_n, QIO_0, QIO_n pins of the Am2904 are intended to be directly connected to the RAM_0, RAM_3, Q_0 and Q_3 pins of the Am2901 or the SIO_0, SIO_3, QIO_0, QIO_3 pins of the Am2903A.

Carry-In Control Multiplexer

The Carry-In Control Multiplexer generates the C_0 output which can be selected from 7 functions (0, 1, C_X, μ_C, M_C, $\overline{\mu_C}$, $\overline{M_C}$). These functions allow easy implementation of both single length and double length addition and subtraction. The C_X input is intended to be connected to the Z output of the Am2903A to facilitate execution of some of the Am2903A special instructions. The C_0 pin is to be connected to the C_n pin of the least significant Am2901 or Am2903A and the C_n pin of the Am2902A.

Am2904 Instruction Set

The Am2904 is controlled by manipulating the 13 instruction lines, I_{0-12}, together with the nine enable lines, $\overline{CE}_M$, $\overline{CE}_\mu$, $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$, $\overline{OE}_Y$, $\overline{OE}_{CT}$, $\overline{SE}$. Most systems will save on microword bits by tying some of these lines to a fixed level or by connecting certain lines together, or by decoding microinstructions to generate appropriate Am2904 controls.

Status Registers

Instruction lines I_5, I_4, I_3, I_2, I_1, I_0 control the Status Registers. Below, these lines are referred to as two octal digits.

Micro Status Register (μSR)

The instruction codes for the Micro Status Register fall into three groups: Bit Operations, Register Operations and Load Operations (See Table 1 and Map 1). All operations require that $\overline{CE}_\mu$ be LOW to operate.

TABLE 1. MICRO STATUS REGISTER INSTRUCTION CODES

Bit Operations		
I_{543210} Octal	μSR Operation	Comments
10	$0 \to \mu_Z$	RESET ZERO BIT
11	$1 \to \mu_Z$	SET ZERO BIT
12	$0 \to \mu_C$	RESET CARRY BIT
13	$1 \to \mu_C$	SET CARRY BIT
14	$0 \to \mu_N$	RESET SIGN BIT
15	$1 \to \mu_N$	SET SIGN BIT
16	$0 \to \mu_{OVR}$	RESET OVERFLOW BIT
17	$1 \to \mu_{OVR}$	SET OVERFLOW BIT

Register Operations		
I_{543210} Octal	μSR Operation	Comments
00	$M_X \to \mu_X$	LOAD MSR TO μSR
01	$1 \to \mu_X$	SET μSR
02	$M_X \to \mu_X$	REGISTER SWAP
03	$0 \to \mu_X$	RESET μSR
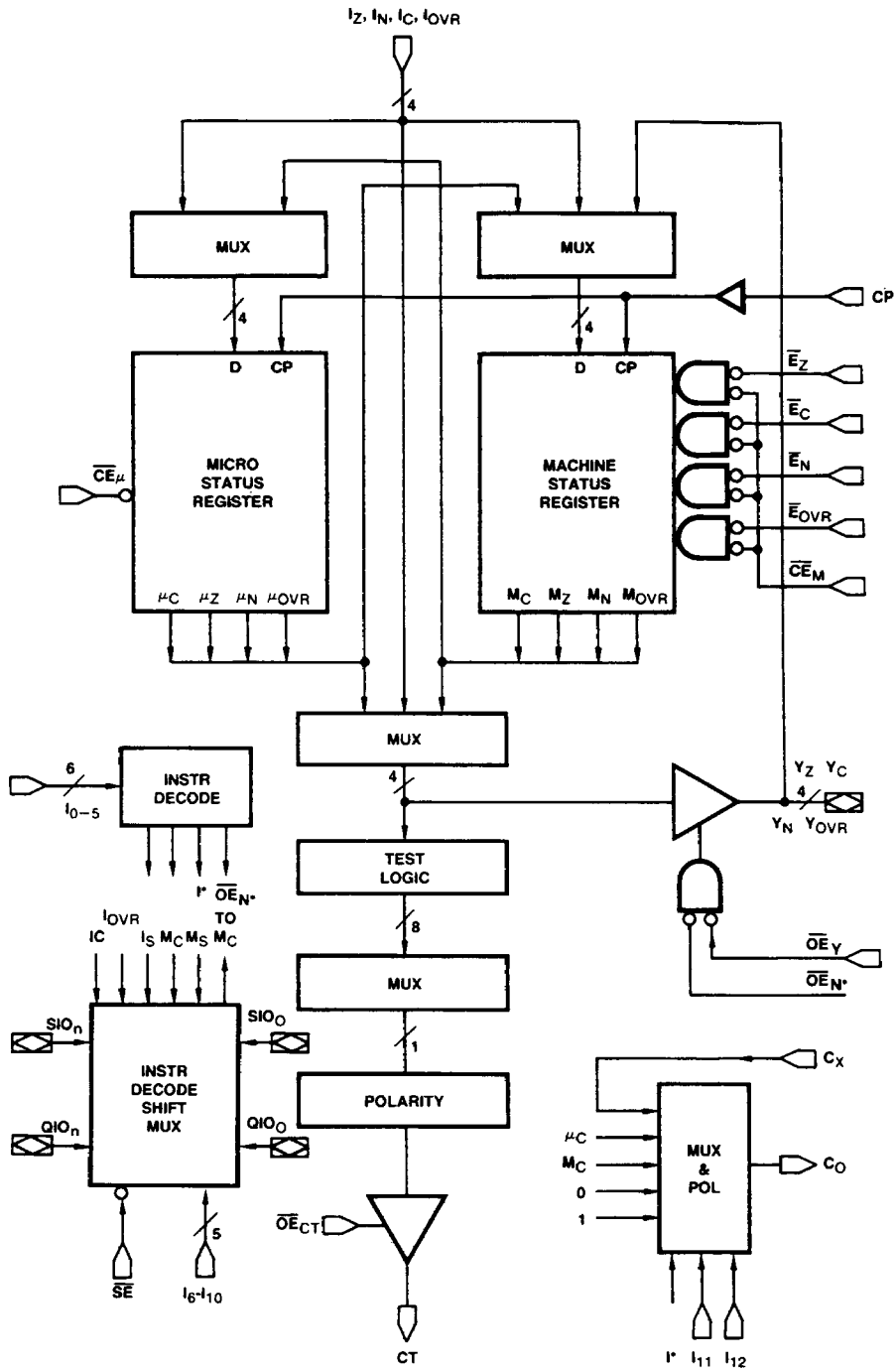
Figure 1. Detailed Block Diagram

BD001841

TABLE 1. (Cont'd.)

Load Operations		
I_{543210} Octal	μSR Operation	Comments
06, 07	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} + \mu_{OVR} \rightarrow \mu_{OVR}$	LOAD WITH OVERFLOW RETAIN
30, 31 50, 51 70, 71	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} \rightarrow \mu_{OVR}$	LOAD WITH CARRY INVERT
04, 05 20-27 32-47 52-67 72-77	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} \rightarrow \mu_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C, I_N, I_{OVR}

Note: The above table assumes $\overline{CE}\mu$ is LOW.

MAP 1. MICRO STATUS REGISTER INSTRUCTION CODES

I_{543} \ I_{210}	000	001	010	011	100	101	110	111
000	LOAD MSR TO μSR	SET μSR	REG SWAP	RESET μSR			LOAD WITH OVERFLOW RETAIN	
001	RESET μZ	SET μZ	RESET μC	SET μC	RESET μN	SET μN	RESET μOVR	SET μOVR
010								
011	LOAD WITH CARRY INVERT							
100								
101	LOAD WITH CARRY INVERT							
110								
111	LOAD WITH CARRY INVERT							
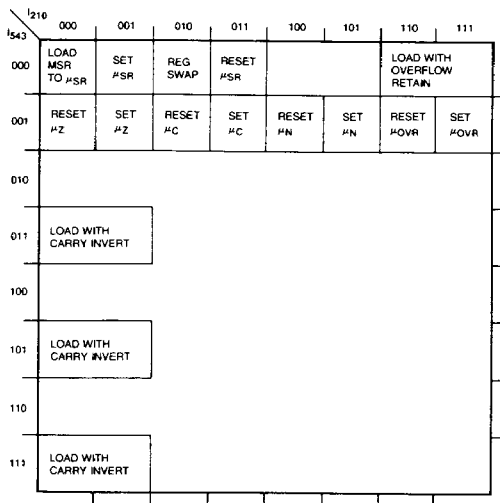
DF000890

Notes: 1. All unmarked locations are a load direct from I_Z, I_C, I_N, I_{OVR}.

Instruction Codes 10_8 to 17_8 are BIT operations. These operations set or reset the individual bits in the μSR.

Instruction Codes 00_8 to 03_8 are REGISTER operations. These operations affect all bits in the μSR.

00_8 This instruction loads the μSR with the contents of the MSR while loading the MSR from the Y inputs and is further explained under "INTERRUPTS".

01_8 This instruction SETS all μSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all μSR bits.

All instruction codes except those mentioned in the above two sections cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

06_8, 07_8 When a series of arithmetic operations are being executed sometimes it is not necessary to test for an overflow condition after *each* operation, but rather it is sufficient simply to know that an overflow occurred during any one of the operations. Use of these instructions captures the overflow condition by loading the μSR overflow bit with the LOGICAL-OR of its present state and I_{OVR}. Thus, once an overflow occurs, μ_{OVR} will remain set throughout the remaining operations.

30_8, 31_8, 50_8, 51_8, 70_8, 71_8 These instructions cause a load from the I inputs, but invert the carry bit. The reason for this is explained more fully under the "BORROW SAVE" section.

All others   The remaining instructions load the μSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

Machine Status Register (MSR)

The instruction codes for the MSR fall into two groups; REGISTER Operations and LOAD Operations. All operations require that $\overline{CE}_M$ be LOW to operate (See Table 2 and Map 2). BIT operations are accomplished by the use of Register or Load Operations with the $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$ inputs selectively set LOW.

Instruction codes 00_8-03_8 and 05_8 are REGISTER operations. They affect only those bits enabled by $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$.

00_8 This instruction loads the MSR from the Y inputs while transferring the present contents to the μSR. The use of this instruction is further explained under "INTERRUPTS".

01_8 This instruction SETS all enabled MSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all enabled MSR bits.

05_8 This instruction COMPLEMENTS all enabled MSR bits.

All instruction codes except those mentioned in the above section cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

04_8 The Am2904 Shift Linkage Multiplexer allows for shifts and rotates through the MSR CARRY bit. Some machines require a shift or rotate through the OVERFLOW bit. By using this code, which swaps the contents of the MSR CARRY bit (M_C) and OVERFLOW bit (M_{OVR}), the shift or rotate can be made to appear to take place through the OVERFLOW bit. The procedure is to swap the bits, shift or rotate (any number or positions) then swap the bits again.
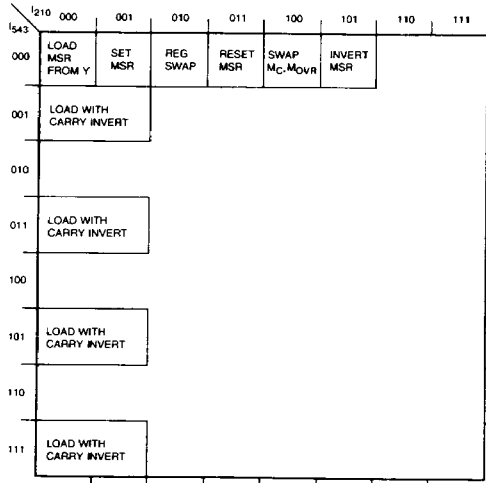
TABLE 2. MACHINE STATUS REGISTER INSTRUCTION CODES

Register Operations		
I_{543210} Octal	MSR Operation	Comments
00	$Y_X \rightarrow M_X$	LOAD Y_Z, Y_C, Y_N, Y_{OVR} TO MSR
01	$1 \rightarrow M_X$	SET MSR
02	$\mu_X \rightarrow M_X$	REGISTER SWAP
03	$0 \rightarrow M_X$	RESET MSR
05	$\overline{M}_X \rightarrow M_X$	INVERT MSR

Load Operations		
I_{543210} Octal	MSR Operation	Comments
04	$I_Z \rightarrow M_Z$ $M_{OVR} \rightarrow M_C$ $I_N \rightarrow M_N$ $M_C \rightarrow M_{OVR}$	LOAD FOR SHIFT THROUGH OVERFLOW OPERATION
10, 11 30, 31 50, 51 70, 71	$I_Z \rightarrow M_Z$ $\overline{I_C} \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD WITH CARRY INVERT
06, 07 12-27 32-47 52-67 72-77	$I_Z \rightarrow M_Z$ $I_C \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C I_N, I_{OVR}

Notes: 1. The above tables assume $\overline{CE}_M$, $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$ are LOW.
2. A shift-through-carry instruction loads M_C irrespective of I_5-I_0.

MAP 2. MACHINE STATUS REGISTER INSTRUCTION CODES

DF000900

06_8, 07_8
 12_8-27_8
 32_8-47_8
 52_8-67_8
 72_8-77_8 These instructions load the MSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

10_8, 11_8
 30_8, 31_8
 50_8, 51_8
 70_8, 71_8 These instructions cause a load from the I inputs but invert the CARRY bit. The reason for this is explained more fully under the 'BORROW SAVE' section.

Condition Code Multiplexer

The two instruction lines I_4, I_5 select whether the μSR, the MSR or the direct inputs I_Z, I_C, I_N, I_{OVR} are used as the inputs to the Y output buffer and the CT output (see Tables 3 and 4).

The four instruction lines I_3, I_2, I_1, I_0 will select one of 16 possible operations to be carried out on the input bits, the result being routed to the Conditional Test Output (CT). Eight of the operations supply an individual status bit or its complement to the CT output. Another four do more complex operations while the remaining four are the complemented results of these (See Table 4).

The more complex operations are intended to follow the calculation A-B to give an indication of which is the larger (A, B unsigned) or more positive (A, B in 2's complement form). See Table 5.

Instruction codes 16_8 and 17_8 form the EXCLUSIVE-OR and the EXCLUSIVE-NOR functions of M_N and I_N. The use of these instructions is explained under "NORMALIZING".

TABLE 3. Y OUTPUT INSTRUCTION CODES

$\overline{OE}_Y$	I_5	I_4	Y Output	Comment
H	X	X	Z	Output Off High Impedance
L	L	X	$\mu_i \rightarrow Y_i$	See Note 1
L	H	L	$M_i \rightarrow Y_i$	
L	H	H	$I_i \rightarrow Y_i$	

Notes: 1. For the conditions:
I_5, I_4, I_3, I_2, I_1, I_0 are LOW, Y is an input. $\overline{OE}_Y$ is "Don't Care" for this condition.
2. X is "Don't Care" condition.

TABLE 4. CONDITION CODE OUTPUT (CT) INSTRUCTION CODES

I_{3-0} HEX	I_3	I_2	I_1	I_0	$I_5 = I_4 = 0$	$I_5 = 0, I_4 = 1$	$I_5 = 1, I_4 = 0$	$I_5 = I_4 = 1$
0	0	0	0	0	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(M_N \oplus M_{OVR}) + M_Z$	$(I_N \oplus I_{OVR}) + I_Z$
1	0	0	0	1	$(\mu_N \oplus \mu_{OVR}) \cdot \overline{\mu}_Z$	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(M_N \odot M_{OVR}) \cdot \overline{M}_Z$	$(I_N \odot I_{OVR}) \cdot \overline{I}_Z$
2	0	0	1	0	$\mu_N \oplus \mu_{OVR}$	$\mu_N \oplus \mu_{OVR}$	$M_N \oplus M_{OVR}$	$I_N \oplus I_{OVR}$
3	0	0	1	1	$\mu_N \odot \mu_{OVR}$	$\mu_N \odot \mu_{OVR}$	$M_N \odot M_{OVR}$	$I_N \odot I_{OVR}$
4	0	1	0	0	μ_Z	μ_Z	M_Z	I_Z
5	0	1	0	1	$\overline{\mu}_Z$	$\overline{\mu}_Z$	$\overline{M}_Z$	$\overline{I}_Z$
6	0	1	1	0	μ_{OVR}	μ_{OVR}	M_{OVR}	I_{OVR}
7	0	1	1	1	$\overline{\mu}_{OVR}$	$\overline{\mu}_{OVR}$	$\overline{M}_{OVR}$	$\overline{I}_{OVR}$
8	1	0	0	0	$\mu_C + \mu_Z$	$\mu_C + \mu_Z$	$M_C + M_Z$	$\overline{I}_C + I_Z(2)$
9	1	0	0	1	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{M}_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z(2)$
A	1	0	1	0	μ_C	μ_C	M_C	I_C
B	1	0	1	1	$\overline{\mu}_C$	$\overline{\mu}_C$	$\overline{M}_C$	$\overline{I}_C$
C	1	1	0	0	$\overline{\mu}_C + \mu_Z$	$\overline{\mu}_C + \mu_Z$	$\overline{M}_C + M_Z$	$\overline{I}_C + I_Z$
D	1	1	0	1	$\mu_C \cdot \overline{\mu}_Z$	$\mu_C \cdot \overline{\mu}_Z$	$M_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z$
E	1	1	1	0	$I_N \oplus M_N$	μ_N	M_N	I_N
F	1	1	1	1	$I_N \odot M_N$	μ_N	$\overline{M}_N$	$\overline{I}_N$

NOTES: 1. $\oplus$ Represents EXCLUSIVE–OR   2. Correct code as stated.
        $\odot$ Represents EXCLUSIVE–NOR or coincidence.

TABLE 5. CRITERIA FOR COMPARING TWO NUMBERS FOLLOWING "A MINUS B" OPERATION

Relation	For Unsigned Numbers			For 2's Complement Numbers		
	Status	I_{3-0} CT = H	I_{3-0} CT = L	Status	I_{3-0} CT = H	I_{3-0} CT = L
A = B	$Z = 1$	4	5	$Z = 1$	4	5
A ≠ B	$Z = 0$	5	4	$Z = 0$	5	4
A ≥ B	$C = 1$	A	B	$N \odot OVR = 1$	3	2
A < B	$C = 0$	B	A	$N \oplus OVR = 1$	2	3
A > B	$C \cdot \overline{Z} = 1$	D	C	$(N \odot OVR) \cdot \overline{Z} = 1$	1	0
A ≤ B	$\overline{C} + Z = 1$	C	D	$(N \oplus OVR) + Z = 1$	0	1

$\oplus$ = Exclusive OR   H = HIGH   Note: For Am2910A the CC input is active LOW, so use I_{3-0} code
$\odot$ = Exclusive NOR   L = LOW   to produce CT = L for the desired test.

Shift Linkage Multiplexer

The five instruction lines $I_{10}, I_9, I_8, I_7, I_6$ control the SHIFT LINKAGE multiplexer. All instructions set up the linkages for both the ALU shifter (RAM shifter on the Am2901C) and the Q register.

UP and DOWN shifts are decided by I_{10} which should be connected to I_8 of the Am2903A's instruction lines or I_7 of the Am2901's instruction lines. A wide range of input and output connections are provided, allowing for single or double length shifting or rotating with or without the use of the MSR CARRY or SIGN bits (See Table 6).

In the following discussion of some of the shifts the instruction codes are given as two octal digits AB; A represents I_{10}, I_9, B represents I_8, I_7, I_6.

When adding and down shifting on the same microcycle, (i.e., when doing multiplication or averaging) the shifter input must be the present CARRY, I_C, rather than the carry resulting from the last cycle (M_C). Instruction Code 13_8 accomplishes this for unsigned arithmetic. For 2's complement arithmetic, the required shifter input is: $I_N \oplus I_{OVR}$. This is provided by Instruction Code 16_8.

Instruction Codes $14_8, 15_8, 17_8$ provide the RIGHT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

Instruction Codes $34_8, 35_8, 37_8$ provide the LEFT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

The shift outputs are in the high-impedance state unless $\overline{SE}$ is LOW.

Loading of the M_C bit by a shift operation overrides any loading or holding of the M_C bit by MSR Instructions (I_{0-5}, $\overline{CE}_M$ and $\overline{E}_C$).

"CARRY-IN" Control Multiplexer

The two instruction lines I_{12}, I_{11} control the source of the CARRY output (C_0).

When $I_{12} = 0$ $C_0 = I_{11}$

When $I_{12} = 1$ and $I_{11} = 0$, the external carry input C_X is presented to the carry output.

When $I_{12} = I_{11} = 1$ the carry output is selected from μ_C, $\overline{\mu}_C$, M_C or $\overline{M}_C$ as defined by I_5, I_3, I_2, I_1 (See Table 7).

APPLICATIONS

Borrow – Save

One of the capabilities of the Am2900 Family is the complete emulation of other processing machines. One requirement of an emulator is that, when a calculation is being performed, not only must the answer obtained from the Am2900 chips be the same as that from the machine being emulated, but after each machine level instruction, the status bits must be identical.

TABLE 6. SHIFT LINKAGE MULTIPLEXER INSTRUCTION CODES

I_{10}	I_9	I_8	I_7	I_6	M_C RAM Q	SIO_0	SIO_n	QIO_0	QIO_n	Loaded into M_C
0	0	0	0	0		Z	0	Z	0	
0	0	0	0	1		Z	1	Z	1	
0	0	0	1	0		Z	0	Z	M_n	SIO_0
0	0	0	1	1		Z	1	Z	SIO_0	
0	0	1	0	0		Z	M_C	Z	SIO_0	
0	0	1	0	1		Z	M_N	Z	SIO_0	
0	0	1	1	0		Z	0	Z	SIO_0	
0	0	1	1	1		Z	0	Z	SIO_0	QIO_0
0	1	0	0	0		Z	SIO_0	Z	QIO_0	SIO_0
0	1	0	0	1		Z	M_C	Z	QIO_0	SIO_0
0	1	0	1	0		Z	SIO_0	Z	QIO_0	
0	1	0	1	1		Z	I_C	Z	SIO_0	
0	1	1	0	0		Z	M_C	Z	SIO_0	QIO_0
0	1	1	0	1		Z	QIO_0	Z	SIO_0	QIO_0
0	1	1	1	0		Z	$I_N \oplus I_{OVR}$	Z	SIO_0	
0	1	1	1	1		Z	QIO_0	Z	SIO_0	
1	0	0	0	0		0	Z	0	Z	SIO_n
1	0	0	0	1		1	Z	1	Z	SIO_n
1	0	0	1	0		0	Z	0	Z	
1	0	0	1	1		1	Z	1	Z	
1	0	1	0	0		QIO_n	Z	0	Z	SIO_n
1	0	1	0	1		QIO_n	Z	1	Z	SIO_n
1	0	1	1	0		QIO_n	Z	0	Z	
1	0	1	1	1		QIO_n	Z	1	Z	
1	1	0	0	0		SIO_n	Z	QIO_n	Z	SIO_n
1	1	0	0	1		M_C	Z	QIO_n	Z	SIO_n
1	1	0	1	0		SIO_n	Z	QIO_n	Z	
1	1	0	1	1		M_C	Z	0	Z	
1	1	1	0	0		QIO_n	Z	M_C	Z	SIO_n
1	1	1	0	1		QIO_n	Z	SIO_n	Z	SIO_n
1	1	1	1	0		QIO_n	Z	M_C	Z	
1	1	1	1	1		QIO_n	Z	SIO_n	Z	

Notes: 1. Z = High-impedance (outputs off) state.
2. Outputs enabled and M_C loaded only if $\overline{SE}$ is LOW.
3. Loading of M_C from I_{10-6} overrides control from $I_{5-0}, \overline{CE}_M, \overline{E}_C$.

TABLE 7. CARRY-IN CONTROL MULTIPLEXER INSTRUCTION CODES

I_{12}	I_{11}	I_5	I_3	I_2	I_1	C_0
0	0	X	X	X	X	0
0	1	X	X	X	X	1
1	0	X	X	X	X	C_X
1	1	0	0	X	X	μC
1	1	0	X	1	X	μC
1	1	0	X	X	1	μC
1	1	0	1	0	0	$\overline{\mu C}$
1	1	1	0	X	X	M_C
1	1	1	X	1	X	M_C
1	1	1	X	X	1	M_C
1	1	1	1	0	0	$\overline{M_C}$

There are alternative methods for subtracting in a digital machine and the state of the CARRY after the calculation depends on the method. For instance, the subtraction of 0100 from 1010 by the 2's complement add method generates a result of 0110 with a CARRY. Direct subtraction however, yields an answer of 0110 with no BORROW.

Many machines store the state of the CARRY for subtract operations, and this is the recommended method for maximum effective use of the Am2904 but, to allow those machines which store the BORROW to be efficiently emulated, the Am2904 has allocated special instructions. Using these codes causes the CARRY bit to be inverted before storage in the status registers and also re-inverts these status bits before using them as carry inputs. These codes are 10_8, 11_8, 30_8, 31_8, 50_8, 51_8, 70_8, 71_8 (I_{5-0}).

Notice that when these codes are used to load the inverted CARRY to either of the status registers, the CT output selected by the Condition Code Multiplexer assumes the CARRY is inverted and still defines whether A > B or A ≤ B (See Table 4).

Similarly, when doing a compare on a machine which saves the BORROW, testing for A > B, A ≤ B forces the complement of the CARRY to be stored in the status registers (See Tables 1 and 2).

Normalizing

Normalizing is the process of stripping off all leading sign bits until the two most significant bits are complementary. The Am2904 facilitates both single and double length normalization in the Am2901 and the Am2903A. When using the NORMALIZE special instructions with the Am2903A, the EXCLUSIVE–OR of the most significant two bits is generated at the C_{n+4} pin of the most significant Am2903A. The EXCLUSIVE–OR of the two bits next to the most significant bit is also generated at the OVR pin. The procedure for normalizing then is to loop on the normalize instruction with a branch condition on the C_{n+4} state or the OVR state, depending on the architecture employed. The C_{n+4} or OVR output is routed to the Am2910 CC input through the Am2904 Condition Code multiplexer. As the contents of the status registers always refer to the last cycle, not the present one, the last operation in normalizing is to downshift, bringing the sign bit (M_N) back into the most significant bit position. This is achieved using the shift operations 05_8 (I_{10-6}) for double length normalizing, and 02_8 for single length normalizing. For more details regarding normalizing with the Am2903A see the Am2903A data sheet.

The Am2901 does not have the EXCLUSIVE–OR gates to help with normalizing, so the Am2904 includes in the Condition Code multiplexer the EXCLUSIVE–OR and EXCLUSIVE–NOR functions of M_N (the sign bit resulting from the last operation) and I_N (the sign bit resulting from the present operation). Instruction codes 16_8 and 17_8 (I_{5-0}) form the EXCLUSIVE–OR and EXCLUSIVE–NOR functions of M_N and I_N.

Interrupts

Some machines allow interrupts only at the machine instruction level while others allow them at the microinstruction level. The Am2904 is designed to handle both cases.

When the machine is interrupted, it is necessary to store the contents of either the MSR (machine instruction level interrupts) or both the status registers (micro instruction level interrupts) into an external store. This transfer is intended to take place over the Y input/output pins (See Table 3).

After the interrupt has been serviced the registers must be restored to their pre-interrupt state. This is accomplished by two operations of instruction 00_8 (I_{5-0}) which loads the MSR from the Y inputs while loading the μSR from the MSR. Thus, the pre-interrupt contents of the μSR are first loaded to the MSR (first instruction 00_8), then this data is transferred to the μSR while the MSR is restored to its pre-interrupt state (second instruction 00_8).

In controllers and some other microprogrammed machines the applications program itself is often in the microprogram memory; that is, there is no macroinstruction set. These machines require only a microstatus register since there is no separate machine status. The MSR in the Am2904 can be used as a one-level stack on the microstatus register. When an interrupt occurs, the μSR and the MSR are simply swapped ($I_{5-0} = 02_8$).
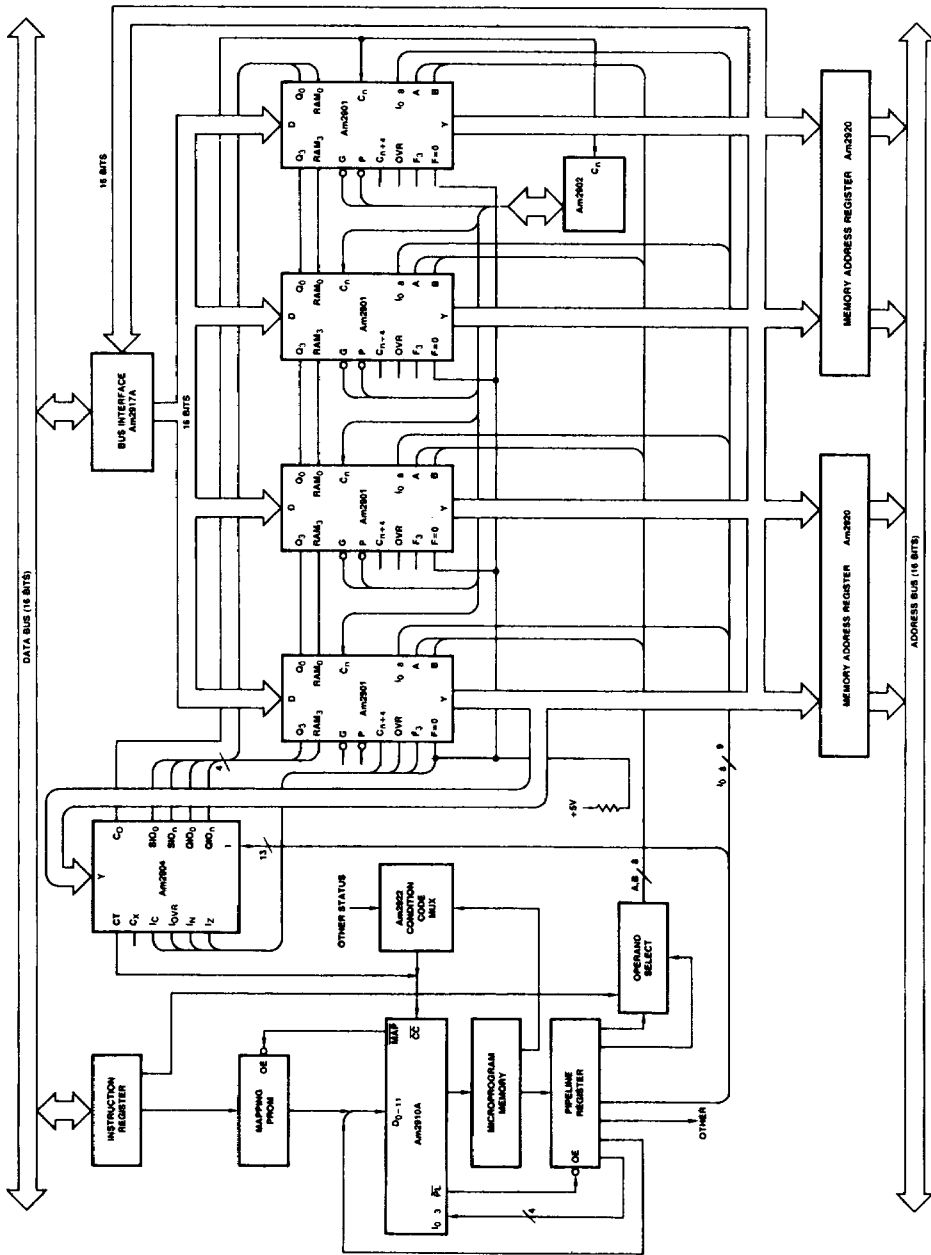
AF001481

Figure 2. Typical Application of Am2904 with Am2901

AF001472

Figure 3. Typical Application of Am2904 with Am2903A

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... -65 to $+150°C$
(Case) Temperature Under Bias .... -55 to $+125°C$
Supply Voltage to Ground Potential
  Continuous .... -0.5 V to $+7.0$ V
DC Voltage Applied to Outputs for
  High Output State .... -0.5 V to $+V_{CC}$ Max.
DC Input Voltage .... -0.5 V to $+5.5$ V
DC Output Current, Into Outputs .... 30 mA
DC Input Current .... -30 mA to $+5.0$ mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature (T_A).................................. 0 to $+70°C$
  Supply Voltage (V_{CC}) .... $+4.75$ V to $+5.25$ V

Military (M) Devices
  Temperature (T_C)............................. -55 to $+125°C$
  Supply Voltage (V_{CC}) .... $+4.5$ V to $+5.5$ V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified; Included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted for APL products.

Parameter Symbol	Parameter Description	Test Conditions (Note 2)			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.6$ mA Y_Z, Y_C, Y_N, Y_{OVR}		2.4			Volts
			$I_{OH} = -0.8$ mA SIO_0, SIO_n, QIO_0 QIO_n, CT, CO		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	Y_Z, Y_C Y_N, Y_{OVR}	I_{OL} = 24 mA (COM'L)			0.5	Volts
				I_{OL} = 16 mA (MIL)			0.5	
			$SIO_0, QIO_0, CT,$ SIO_n, QIO_n, CO	I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., $I_{IN} = -18$ mA					-1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., $V_{IN} = 0.5$ V	CP				-0.7	mA
			$\overline{CE}_M, \overline{CE}_\mu$				-1.8	
			I_Z, I_C, I_N, I_{OVR}				-1.2	
			$I_0\text{-}I_{12}, \overline{E}_Z, \overline{E}_C, \overline{E}_N$ $\overline{E}_{OVR}, \overline{OE}_Y, \overline{OE}_{CT},$ $C_X, Y_Z, Y_C, Y_N, Y_{OVR}$				-0.45	
			$\overline{SE}, SIO_0, SIO_n$ QIO_0, QIO_n				-1.35	
I_{IH}	Input HIGH Current	V_{CC} = Max., $V_{IN} = 2.7$ V	$CP, I_0\text{-}I_{12}, \overline{E}_Z, \overline{E}_C,$ $\overline{E}_N, \overline{E}_{OVR}, \overline{OE}_Y, \overline{OE}_{CT}, C_X$				20	μA
			$\overline{CE}_M, \overline{CE}_\mu$				80	
			$I_Z, I_C, I_N, I_{OVR}, \overline{SE}$				60	
			$SIO_0, SIO_n, QIO_0, QIO_n$				110	
			Y_Z, Y_C, Y_N, Y_{OVR}				70	
I_I	Input HIGH Current	V_{CC} = Max., $V_{IN} = 5.5$ V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = Max.	CT	$V_O = 2.4$			50	μA
				$V_O = 0.5$			-50	
			$SIO_0, SIO_n, QIO_0, QIO_n$ (Note 4)	$V_O = 2.4$			110	
				$V_O = 0.5$			-1350	
			Y_Z, Y_C, Y_N, Y_{OVR} (Note 4)	$V_O = 2.4$			70	
				$V_O = 0.5$			-450	
I_{OS}	Output Short-Circuit Current (Note 3)	V_{CC} = 5.75 V, $V_O = 0.5$ V			-30		-85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = Max.	COM'L	$T_A = 0°C$ to $+70°C$			318	mA
				$T_A = +70°C$			262	
			MIL	$T_C = -55°C$ to $+125°C$			348	
				$T_C = +125°C$			222	

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
    2. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
    3. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
    4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
    5. Worst-case I_{CC} is at minimum temperature.
    6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested.)

SWITCHING CHARACTERISTICS

The following tables define the Am2904 switching characteristics. Tables A are setup and hold times relative to the clock LOW-to-HIGH transition; Tables B are combinational delays; Tables C are clock requirements. All measurements are made at 1.5 V with input levels at 0 V or 3 V. All values are in ns. All outputs have maximum DC loading.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

A. Setup and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	14	5
I_C (I_1 I_2 I_3 = 001)	27	5
I_C (I_1 I_2 I_3 ≠ 001)	14	5
$\overline{CE}\mu$	18	3
$\overline{CE}_M$	23	3
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$	22	3
$I_0 - I_5$	41	1
$I_6 - I_{10}$	40	1
$\overline{SE}$	36	0
Y_Z, Y_C, Y_N, Y_{OVR} (I_{0-5} = LOW)	15	5
SIO_0, SIO_n, QIO_0, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z, I_C, I_N, I_{OVR}	Y_Z, Y_C, Y_N, Y_{OVR}	38
CP	Y_Z, Y_C, Y_N, Y_{OVR}	41
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	35
I_Z, I_C, I_N, I_{OVR}	CT	33
CP	CT	36
$I_0 - I_5$	CT	33
C_X	C_O	20
CP	C_O	27
$I_{1, 2, 3, 5, 11, 12}$	C_O	39
SIO_n, QIO_n	SIO_0	19
SIO_0, QIO_0	SIO_n	19
I_C, I_N, I_{OVR}	SIO_n	26
SIO_n, QIO_n	QIO_0	19
SIO_0, QIO_0	QIO_n	19
CP	SIO_0, SIO_n, QIO_0, QIO_n	30
I_6-I_{10}	SIO_0, SIO_n, QIO_0, QIO_n	26

C. Clock Requirements (ns)

| Minimum Clock LOW Time	20
Minimum Clock HIGH Time	20

D. Enable/Disable Times (ns)

C_L = 5.0 pF for output disable tests measured to 0.5 V change of output voltage level.

From (Input)	To (Output)	Enable	Disable
$\overline{OE}_{CT}$	CT	23	18
$\overline{SE}$	SIO_0, SIO_n QIO_0, QIO_n	30	16
I_{10}	SIO_0, SIO_n QIO_0, QIO_n	39	29
$\overline{OE}_Y$	Y_Z, Y_C, Y_N, Y_{OVR}	26	21
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	28	40

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE
(Included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted)

A. Setup and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	15	5
I_C (I_1 I_2 I_3 = 001)	28	5
I_C (I_1 I_2 I_3 ≠ 001)	15	5
$\overline{CE}\mu$	20	3
$\overline{CE}_M$	23	4
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$	23	4
$I_0 - I_5$	48	2
$I_6 - I_{10}$	44	2
$\overline{SE}$	40	0
Y_Z, Y_C, Y_N, Y_{OVR} (I_{0-5} = LOW)	16	6
SIO_0, SIO_n, QIO_0, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z, I_C, I_N, I_{OVR}	Y_Z, Y_C, Y_N, Y_{OVR}	40
CP	Y_Z, Y_C, Y_N, Y_{OVR}	45
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	38
I_Z, I_C, I_N, I_{OVR}	CT	44
CP	CT	40
$I_0 - I_5$	CT	41
C_X	C_O	22
CP	C_O	28
$I_{1, 2, 3, 5, 11, 12}$	C_O	42
SIO_n, QIO_n	SIO_0	20
SIO_0, QIO_0	SIO_n	20
I_C, I_N, I_{OVR}	SIO_n	29
SIO_n, QIO_n	QIO_0	20
SIO_0, QIO_0	QIO_n	20
CP	SIO_0 SIO_n, QIO_0, QIO_n	32
I_6-I_{10}	SIO_0, SIO_n, QIO_0, QIO_n	31

C. Clock Requirements (ns)

Minimum Clock LOW Time	25
Minimum Clock HIGH Time	25

D. Enable/Disable Times (ns)

C_L = 5.0 pF for output disable tests measured to 0.5 V change of output voltage level.

From (Input)	To (Output)	Enable	Disable
$\overline{OE}_{CT}$	CT	25	18
$\overline{SE}$	SIO_0, SIO_n QIO_0, QIO_n	35	20
I_{10}	SIO_0, SIO_n QIO_0, QIO_n	43	32
$\overline{OE}_Y$	Y_Z, Y_C, Y_N, Y_{OVR}	28	23
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	30	41

SWITCHING TEST CIRCUITS

TC001120

TC001130
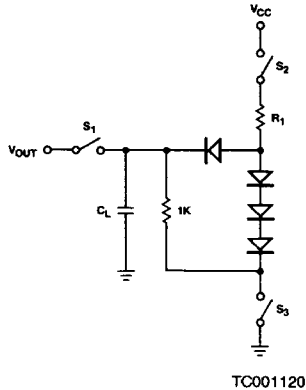
A. Three-State Outputs

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$
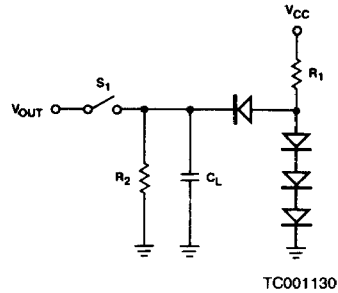
B. Normal Outputs

$$R_2 = \frac{2.4 \text{ V}}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. S_1, S_2, S_3 are closed during function all tests and AC tests except output enable tests.
3. S_1 and 3_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.

TEST OUTPUT LOADS FOR Am2904

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
25	C_0	B	470	3K
27	CT	A	430	1K
28	Y_{OVR}	A	220	1K
29	Y_N	A	220	1K
31	Y_C	A	220	1K
32	Y_Z	A	220	1K
33	QIO_n	A	430	1K
34	QIO_0	A	430	1K
35	SIO_n	A	430	1K
36	SIO_0	A	430	1K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.

4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.

6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

SWITCHING WAVEFORMS
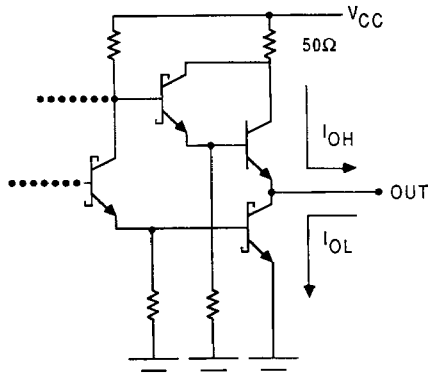
KEY TO SWITCHING WAVEFORMS

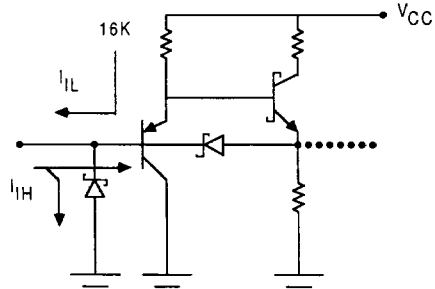| WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010
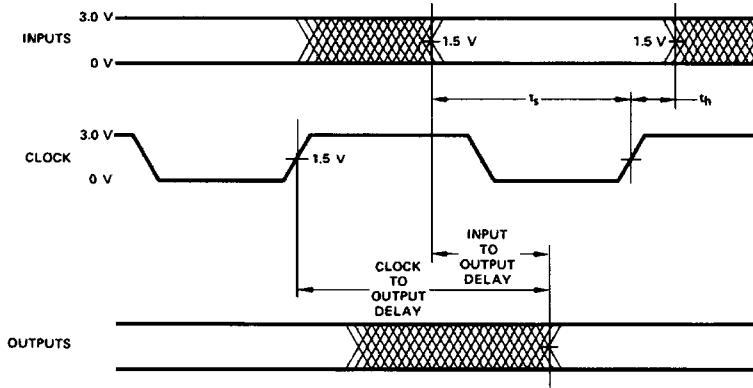
WFR02990
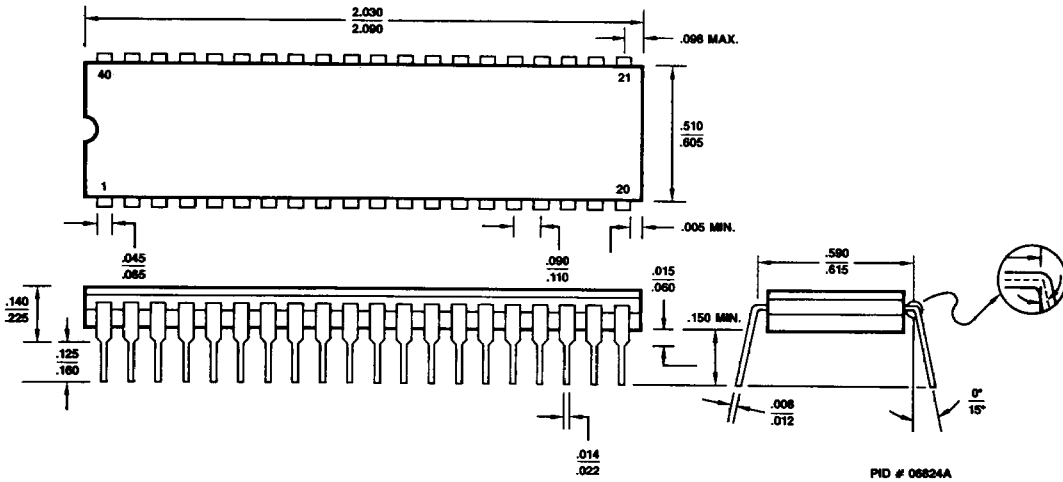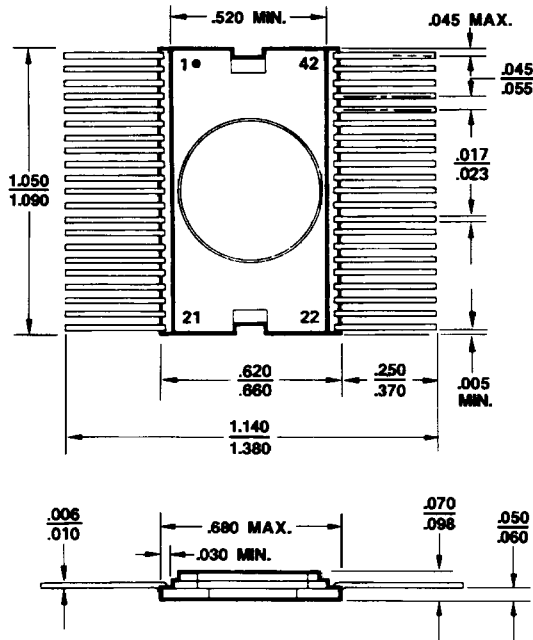
INPUT/OUTPUT CIRCUIT DIAGRAM

IC000940

A. Driving Output

IC000950

B. Driven Input

PHYSICAL DIMENSIONS*

CD 040

2.030 / 2.090
.096 MAX.
40
21
.510 / .605
1
20
.005 MIN.
.045 / .065
.090 / .110
.015 / .060
.150 MIN.
.140 / .225
.125 / .160
.590 / .615
.008 / .012
0° / 15°
.014 / .022

PID # 06824A

CFT042

.520 MIN.
.045 MAX.
1
42
.045 / .055
.017 / .023
1.050 / 1.090
21
22
.620 / .660
.250 / .370
.005 MIN.
1.140 / 1.380
.006 / .010
.680 MAX.
.030 MIN.
.070 / .098
.050 / .060

PID # 07415B

*For reference only.

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