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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E35RG73248LW6M250-C

Overview:

- 3.5-inch TFT: 320x480 (61.90x91.04)
- 3/4 SPI+16/18- bit RGB
- 8/9/16/18-bit MCU
- CTP Interface I2C
- White LED back-light

- Transmissive/ Normally White
- Capacitive Touch Screen
- 250 NITS
- Controller: ILI9488, FT6236
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5" TFT-LCD contains 320X480 pixels, and can display up to 65K/262K colors.

Features

Low Input Voltage: 3.3V (TYP)

Display Colors of TFT LCD: 65K/262K colors

TFT Interface: 8/9/16/18-bit RGB

                   3/SPI/4SPI+16bit/18bit RGB

CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	48.96(H)*73.44(V) (3.5inch)	mm	-
CTP view area	49.96(H)*74.44(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*480	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	6:00	o'clock	-
TFT Controller IC	ILI9488	-	-
CTP Driver IC	FT6236	-	-
Display mode	Transmissive/Normally White	-	-
Touch mode	Single point and gestures	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Horizontal(H)		61.90		mm	-
	Vertical(V)		91.04		mm	-
	Depth(D)		4.33		mm	-
Weight			TBD		g	-

1. Block Diagram
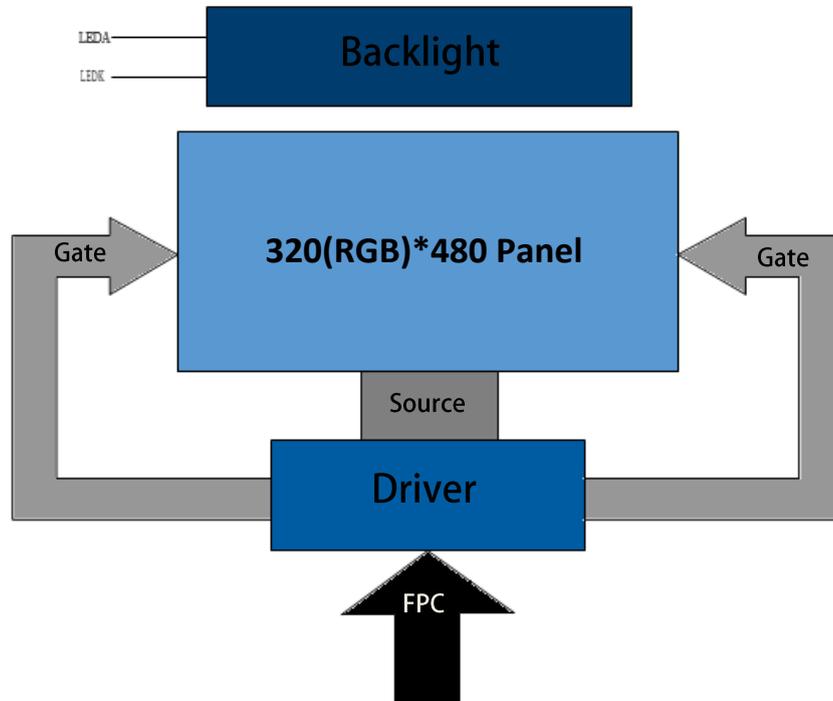
2. Outline Dimensions

2.1 LCM

NO.	Pin Name
1	GND
2	IOVCC
3	IOVCC
4	VCI
5	VCI
6	IM0/ID
7	IM1
8	IM2
9	RESX
10	VSYNC
11	HSYNC
12	PCLK
13	DE
14	DB17/R5,MSb
15	DB16/R4
16	DB15/R3
17	DB14/R2
18	DB13/R1
19	DB12/R0,LSb
20	DB11/G5,MSb
21	DB10/G4
22	DB09/G3
23	DB08/G2
24	DB07/G1
25	DB06/G0,LSb
26	DB05/B5,MSb
27	DB04/B4
28	DB03/B3
29	DB02/B2
30	DB01/B1
31	DB0/B0,LSb
32	GND
33	DOUT
34	DIN_SDA
35	RDX
36	WRX_SCL
37	DCX
38	CSX
39	XR(X+)
40	YD(Y-)
41	XL(X-)
42	YU(Y+)
43	LEDA
44	LEDK1
45	LEDK2
46	LEDK3
47	LEDK4
48	LEDK5
49	LEDK6
50	GND

320(RGB)*480
3.5"TFT LCD

FRONT BACK

T:0.2mm

FPC

CONTACT SIDE

LED(B/L) CIRCUIT

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0
0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0
0	1	1	DBI Tyb_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

NOTE:
1. If not use PIN, fix to the GND, IOVCC or NC.
2. If use RGB interface must select serial interface

NOTES:
1. DISPLAY TYPE: 3.5", TFT-LCD, 262K COLORS
2. DISPLAY MODE: T/N NORMALLY WHITE
3. VIEWING DIRECTION: 6:00
4. DRIVER IC: ILI9488 (COG)
5. VCI: 3.3V,
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 6 LED, 90-120mA, 3.2V±0.3V
8. RoHS COMPLIANT.

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TOLERANCE( )		DRAWING NAME	E35RG73248LW6M250-C
		PARTS NO.	
TOLERANCE UNLESS	X.X±0.3	Drawn	Unit
OTHERWISE SPECIFIED	X.XX±0.2	Checked	mm
Scale 1:1		Approve	Page 1/1

ReV.	Revision content description	Date

2.2 CTP

FRONT

61.90±0.2 LENS OD
49.96 LENS VA
5.97
9.24
96.04±0.2 LENS OD
74.44 LENS VA
8.08±0.5
53.00±0.5
21.02
3.50
0.30±0.05
0.50
P0.5*(8−1)=3.50±0.05
4.50±0.1
Component area
4*R2.00

SIDE

2.00MAX
0.55 LENS
0.175 OCA
0.55 SENSOR
0.50 FOAM
FRONT
BACK
0.13±0.03
1.30MAX
CONTACT SIDE
PI ??
0.30±0.03

BACK

55.76 SENSOR OD
3.07
54.50 FOAM OD
3.70
51.16
5.37
8.64
6.58
6.38
83.08 SENSOR OD
82.68 FOAM OD
75.64
4*R0.50
T=0.5MM
Grounded
T=0.2MM
3.00
5.00
PI +FPC
T=0.3±0.05M4

NO.	Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:
1.DRIVER IC: FT6236
2.WORKING VOLTAGE: 3.3V
3.LIGHT TRANSMISSION：≥86%
4.SURFACE HARDNESS: 6H
5.OPERATING TEMP：−20℃～+70℃，≤90%RH
6.STORAGE TEMP：−30℃～+80℃，≤90%RH
7.UNMARKED TOLERANCE±0.2mm
8.PRECISE DIMENSION IN<>

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			DRAWING NAME	E35RG73248LW6M250-C	
	TOLERANCE( )		PARTS NO.		
ReV.	Revision content description	Date			
			TOLERANCE UNLESS X.X±0.3	Drawn	Unit
			OTHERWISE SPECIFIED X.XX±0.2	Checked	mm
	Scale 1:1			Approve	Page 1/1

2.3 LCM + CTP

Dimensions (left view - FRONT/lens):
- 61.90±0.2 LENS OD
- 49.96 LENS VA
- 48.96 LCD A.A.
- 5.97
- 6.47
- 9.74
- 9.24
- 96.04±0.2 LENS OD
- 73.44 LCD A.A.
- 74.44 LENS VA
- 320(RGB)*480 3.5"TFT LCD
- 4*R2.00
- 8.08±0.5
- 6.50
- 12.00
- 10.00
- 6.50
- 21.02
- 3.50
- 3.50
- 51.82
- 50
- 1
- W=0.30
- P0.5*49=24.5±0.05
- 25.50
- COMPONENT AREA
- 0.30±0.05
- 0.50
- P0.5*(8-1)=3.50±0.05
- 4.50±0.1

Side view (FRONT / BACK):
- 4.33±0.20 TOTAL
- 1.78±0.15 CTP
- 2.55±0.10 LCM
- 0.80
- 0.13±0.03
- 1.30MAX
- CONTACT SIDE PI ??
- 0.30±0.03
- CONTACT SIDE PI ??
- 0.30±0.03

Right view (BACK/sensor):
- 55.50±0.20 BL
- 55.76 SENSOR OD
- 54.50±0.1
- 0.50
- 3.20
- 3.07
- 6.38
- 6.13
- 0.50
- 83.08 SENSOR OD
- 83.96±0.1
- 84.96±0.20 BL
- T:0.2mm
- 5.13
- 15.00
- 47.82
- CONPONENT AREA
- 3.00
- 5.00
- Grounded T=0.2MM
- 3.00
- 5.00
- 丝印白色对位线

TFT Pin Name

NO.	TFT Pin Name
1	GND
2	IOVCC
3	IOVCC
4	VCI
5	VCI
6	IM0/ID
7	IM1
8	IM2
9	RESX
10	VSYNC
11	HSYNC
12	PCLK
13	DE
14	DB17/R5,MSb
15	DB16/R4
16	DB15/R3
17	DB14/R2
18	DB13/R1
19	DB12/R0,LSb
20	DB11/G5,MSb
21	DB10/G4
22	DB09/G3
23	DB08/G2
24	DB07/G1
25	DB06/G0,LSb
26	DB05/B5,MSb
27	DB04/B4
28	DB03/B3
29	DB02/B2
30	DB01/B1
31	DB0/B0,LSb
32	GND
33	DOUT
34	DIN_SDA
35	RDX
36	WRX_SCL
37	DCX
38	CSX
39	XR(X+)
40	YD(Y-)
41	XL(X-)
42	YU(Y+)
43	LEDA
44	LEDK1
45	LEDK2
46	LEDK3
47	LEDK4
48	LEDK5
49	LEDK6
50	GND

CTP Pin Name

NO.	CTP Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:
1. DISPLAY TYPE: 3.5", TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: T/N NORMALLY WHITE
3. VIEWING DIRECTION: 6:00
4. TFT DRIVER IC: ILI9488 (COG)
   CTP DRIVER IC: FT6236
5. VCI: 3.3V(TFT)
   VDD: 3.3V(CTP)
6. CTP SURFACE HARDNESS: 6H
7. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
8. TFT BACK LIGHT: LED WHITE, 6 LED, 120mA, 3.2±0.3V
9. RoHS COMPLIANT.

LED(B/L) CIRCUIT
- K1
- K_
- K3
- K4
- K5
- K6
- A

Interface type

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	0	1	DBI Tyb_ 9-bit interface	DB8-DB0
0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0
0	1	1	DBI Tyb_ 8-bit interface	DB7-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDI SCL CS
1	1	1	4-Wire 8 BIT data serial interface	SDI SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.
2. If use RGB interface must select serial interface

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TOLERANCE( )	DRAWING NAME	E35RG73248LW6M250-C		
	PARTS NO.			
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3	Drawn		Unit
	X.XX±0.2	Checked		mm
Scale 1:1		Approve		Page 1/1

ReV	Revision content description	Date

3.   Input TFT Terminal Pin Assignment

Recommended TFT Connector: FH12S-50S-0.5SH(55) | Recommended CTP Connector: FH12-8S-0.5SH(55)

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	IOVCC	Supply voltage (1.8-3.3V)	P
3	IOVCC	Supply voltage (1.8-3.3V)	P
4	VCI	Supply voltage (3.3V)	P
5	VCI	Supply voltage (3.3V)	P
6	IM0/ID	MPU parallel interface bus and serial interface select. Must select serial interface in RGB interface mode. Fix pin at VCI and GND.	I
7	IM1		I
8	IM2		I
9	RESX	Reset signal. Must be used to properly initialize the chip.	I
10	VSYNC	Frame synchronizing signal for RGB interface. Fix to VCI or GND when not used.	I
11	HSYNC	Line synchronizing signal for RGB interface. Fix to VCI or GND when not in use.	I
12	PCLK	Dot clock signal for RGB interface. Fix to VCI or GND when not in use.	I
13	DE	Data enable signal for RGB interface. Fix to VCI or GND when not used.	I
14-31	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND when not used.	I
32	GND	Ground	I
33	DOUT	Serial data output in serial bus interface. Leave open when not used.	O
34	DIN_SDA	Serial input signal. Data applied on rising edge of SCL signal. Fix to VCI or GND when not used.	I
35	RDX	Read signal /MCU read data at rising edge. Fix to VCI or GND if not used.	I
36	WRX_SCL	Data applied on the rising edge of SCL signal. Fix to VCI or GND if not used.	I
37	DCX	Display data/command section pin.	I
38	CSX	Chip select input pin ("low" enable). Fix to VCI or GND if not used.	I
39	XR(NC)	Touch panel right glass terminal	A/D
40	YD(NC)	Touch panel bottom film terminal	A/D
41	XL(NC)	Touch panel left glass terminal	A/D
42	YU(NC)	Touch panel top film terminal	A/D
43	LEDA	Anode pin of backlight	P
44	LEDK1	Cathode pin of backlight	P
45	LEDK2	Cathode pin of backlight	P
46	LEDK3	Cathode pin of backlight	P
47	LEDK4	Cathode pin of backlight	P
48	LEDK5	Cathode pin of backlight	P
49	LEDK6	Cathode pin of backlight	P
50	GND	Ground	P

3.1   CTP

No	Symbol	Description	I/O
1	GND	Ground	P
2	VDDIO	I/O power supply voltage	P
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host	I
7	RST	External reset, low is active	I
8	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical specification

Item			Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio			CR	Θ=0 Normal viewing angle	--	500	--		(2)
Transmittance			T%		--	5.5	--	%	(3)
Response time	Rising		Tr+Tf		--	20	40	ms	(4)
	Falling				--			ms	
Color Filter Chromaticity	White	W_X			0.292	0.307	0.322		(5)
		W_Y			0.312	0.327	0.342		
	Red	R_X			0.609	0.624	0.639		
		R_Y			0.316	0.331	0.346		
	Green	G_X			0.281	0.296	0.311		
		G_Y			0.562	0.577	0.592		
	Blue	B_X			0.128	0.143	0.158		
		B_Y			0.094	0.109	0.114		
Viewing angle	Hor.	ΘL		CR>10	--	70	--	deg	(1)(6)
		ΘR			--	70	--		
	Ver.	ΘU			--	60	--		
		ΘD			--	60	--		
NTSC					57	60	--	%	(5)
Cross Talk			Ct		--	--	2	%	

4.2 Measuring conditions
Measuring surrounding: dark room
Ambient temperature: 25±2 ℃
15min. warm-up time.

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
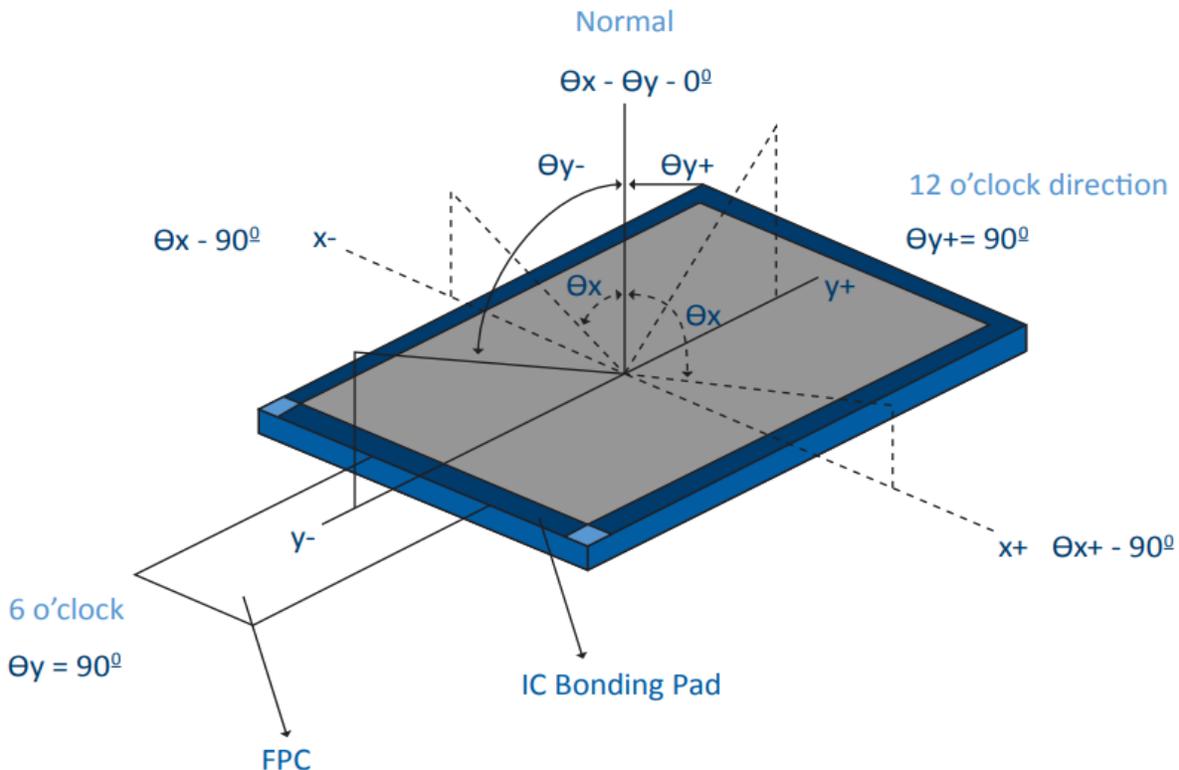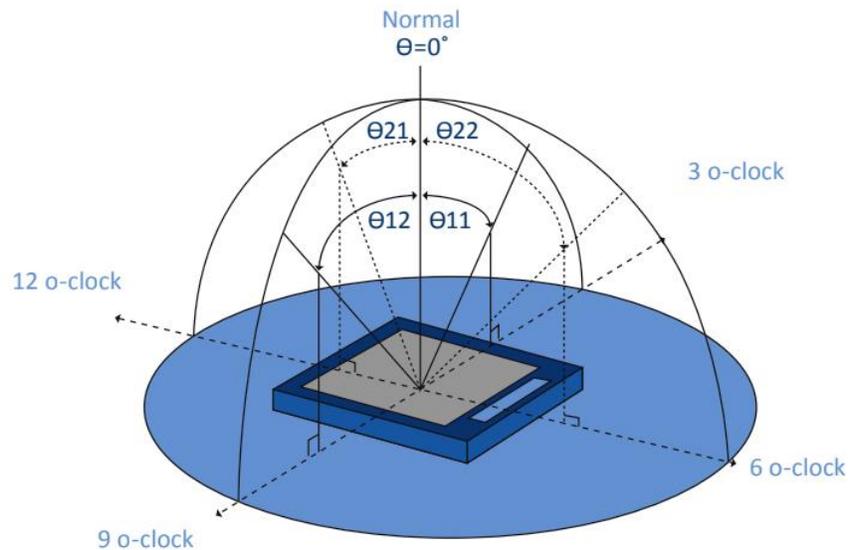
(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.
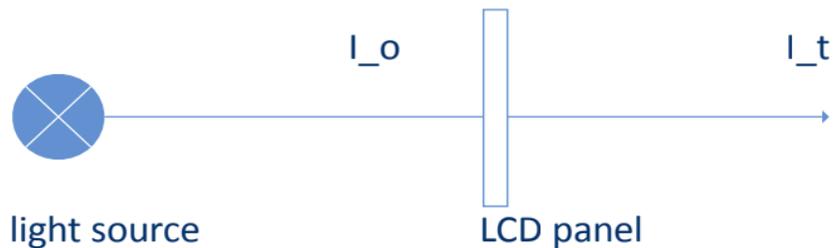
The transmittance is defined as:

$$Tr = \frac{It}{Io} \; x \; 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.
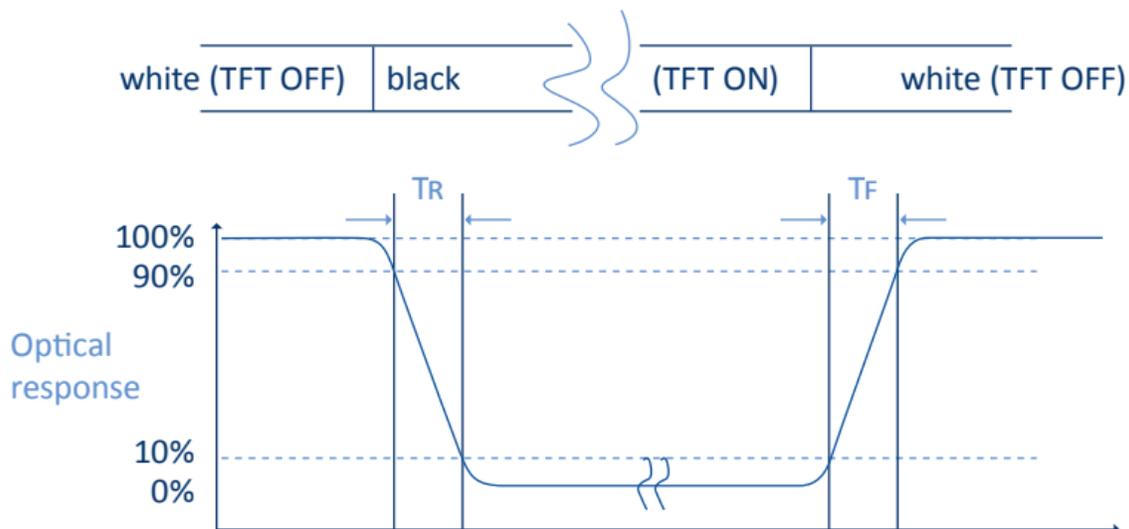
(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
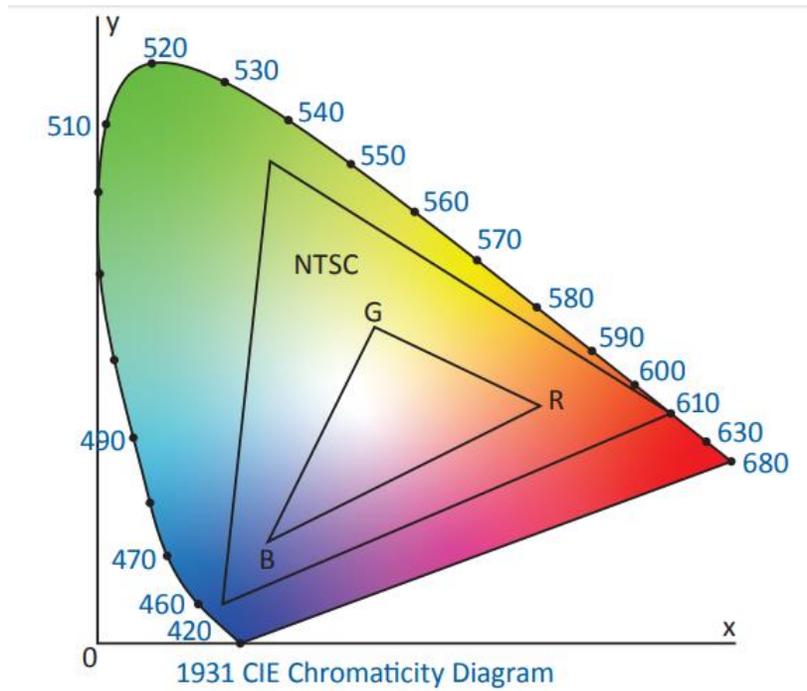
Fig. 1931 CIE chromacity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:
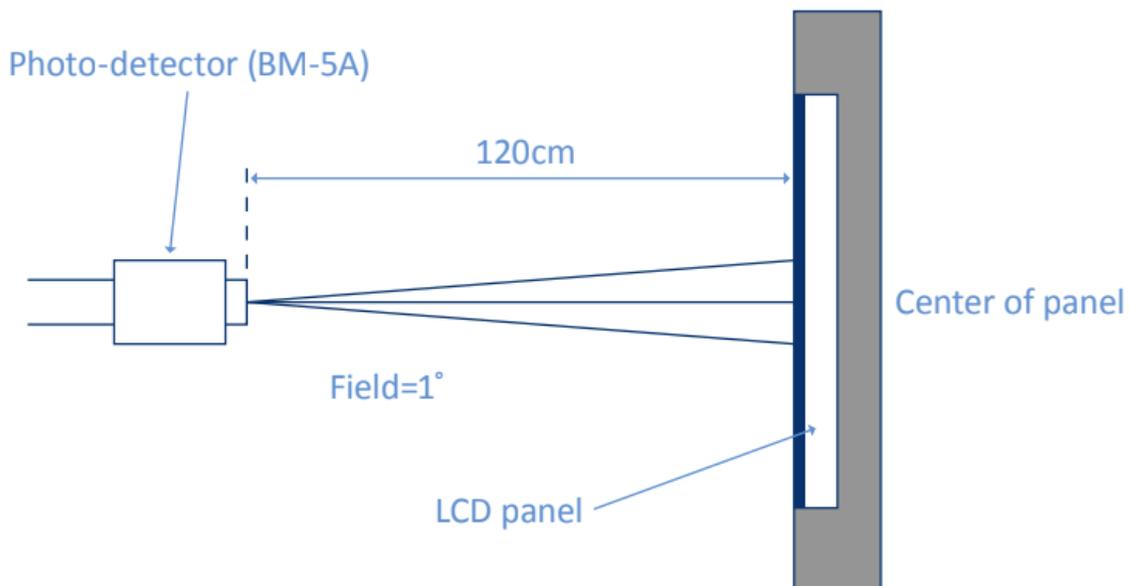
(6) Optical Measurement Setup Continued:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.

Horizontal Dimension

X = test point

X = 1 to 5
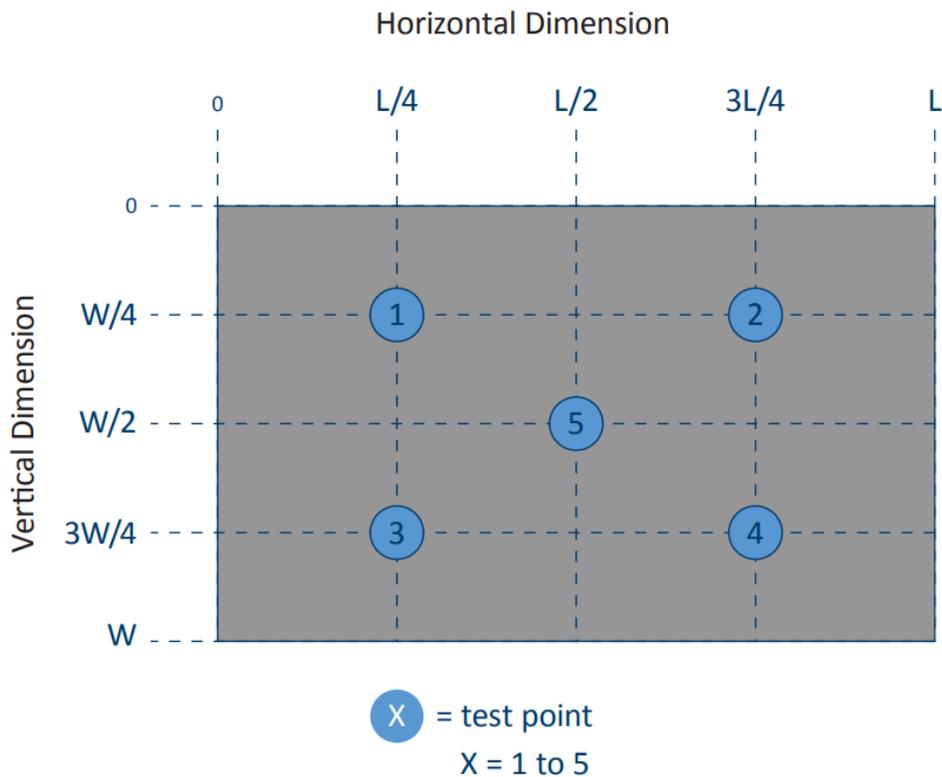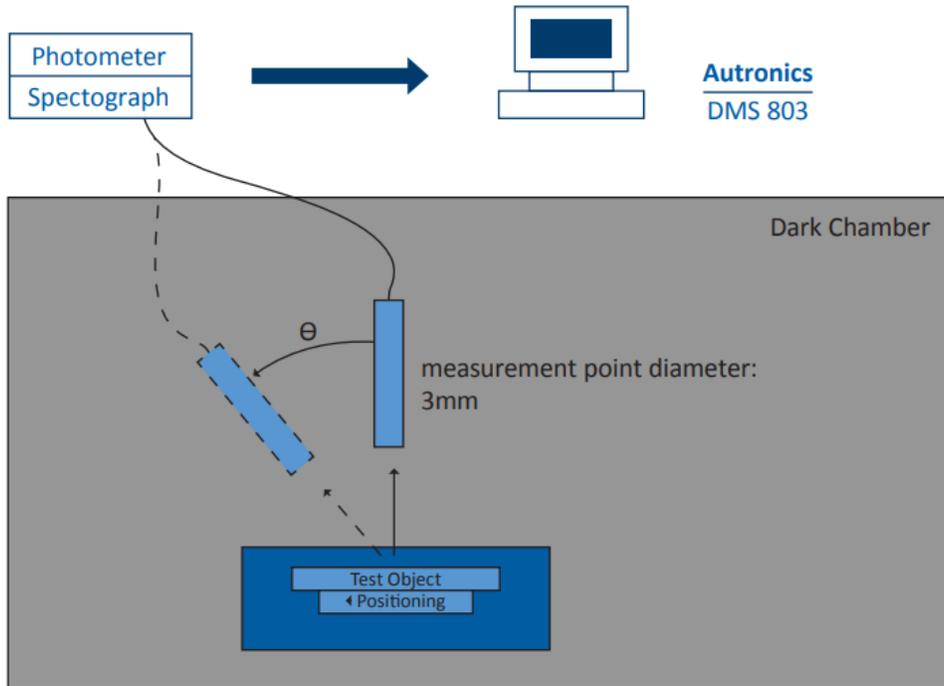
5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Interface Supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	TOP	-20	+70	℃
Storage temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI/VDD	3.0	3.3	4.2	V	
Interface Operation Voltage	VDDIO	1.65	3.3	4.2	V	
Normal Mode Current Consumption	IDD	--	30	--	mA	
Level input voltage	VIH	0.7 VDDIO		VDDIO	V	
	VIL	GND		0.3 VDDIO	V	
Level output voltage	VOH	0.8VDDIO		VDDIO	V	
	VOL	GND		0.2VDDIO	V	

5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	90	120	--	mA	
Forward Voltage	VF	2.9	3.2	3.4	V	
LCM Luminance	LV	250	--	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 6 chips White LED

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition:

Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at

Ta=25℃ and IL=120mA. The LED lifetime could be decreased if operating IL is larger than 120mA. The constant current driving method is suggested.

LED(B/L) CIRCUIT
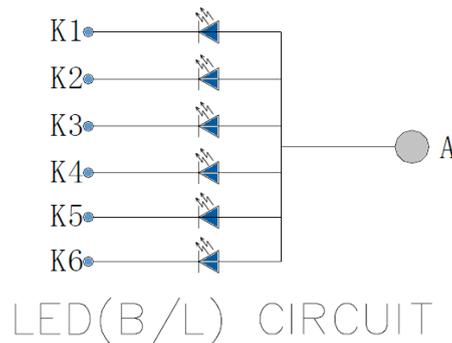
Note 3: Luminance Uniformity of these 9 points is defined as below:
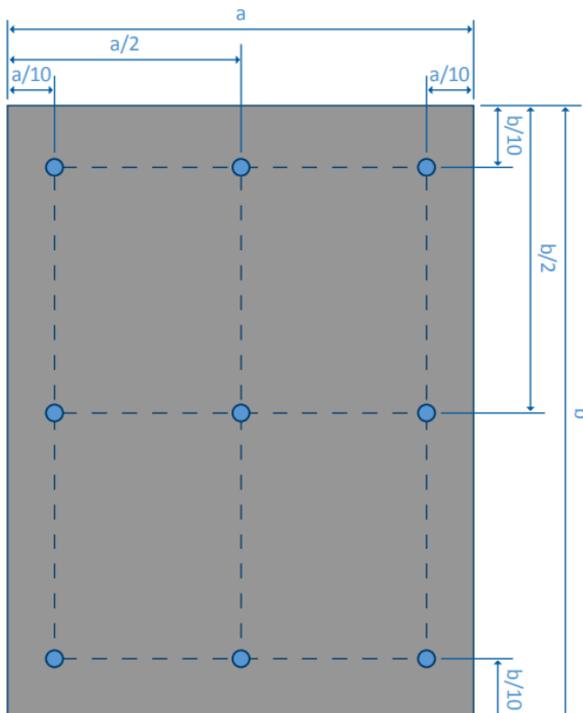
$$\text{Luminance} = \frac{(\text{Total Luminance of 9 points})}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristic

6.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)
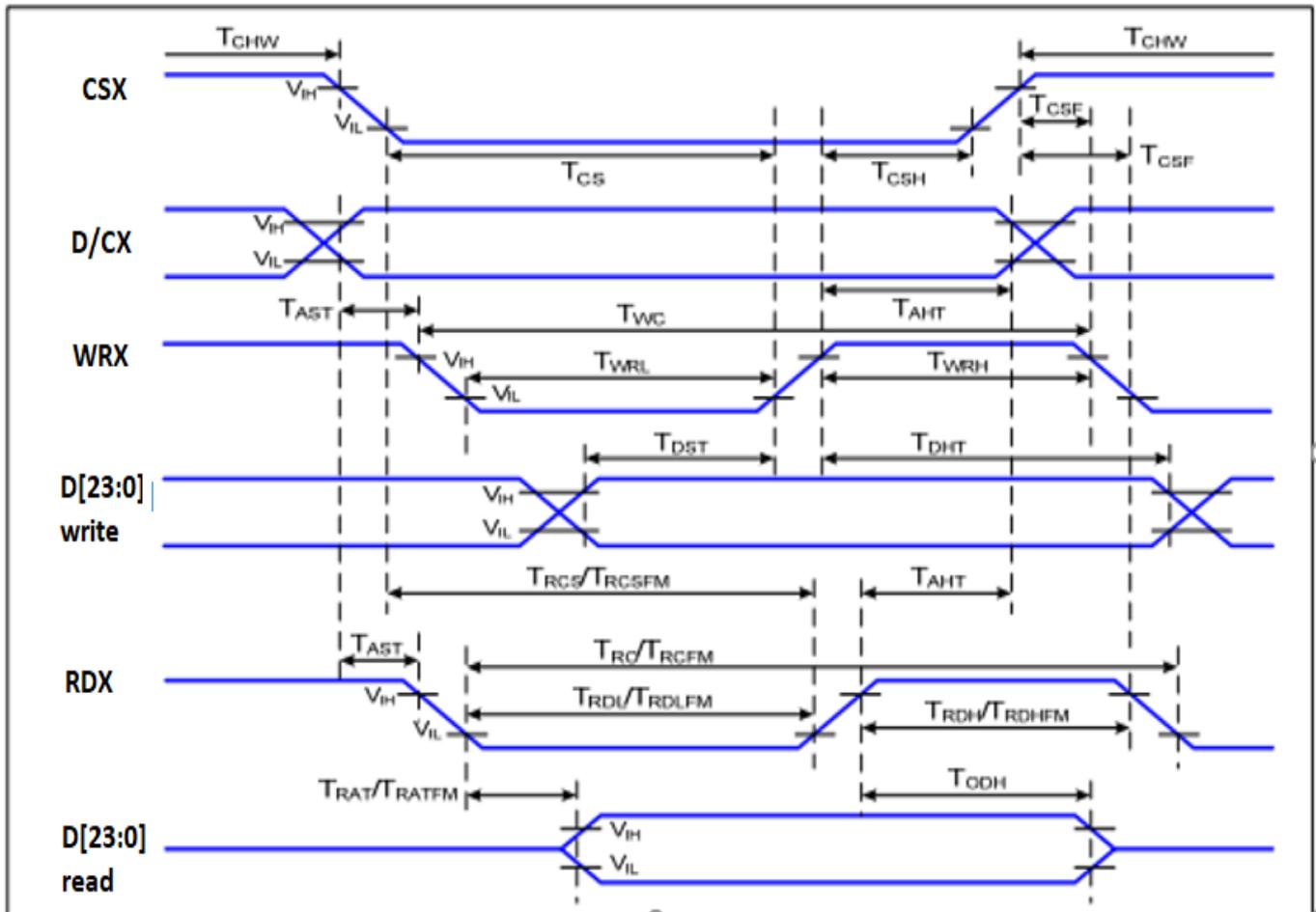
Figure 6.1: Parallel Interface Timing Diagram (8080-Series MCU Interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	30		ns	
	T_{SHW}	SCL "H" pulse width (write)	10		ns	
	T_{SLW}	SCL "L" width (write)	10		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL "H" pulse width (read)	60		ns	
	T_{SLR}	SCL "L" pulse width (read)	60		ns	
SDA/SDI (Input)	T_{SDS}	Data setup time (write)	10		ns	
	T_{SDH}	Data hold time (Write)	10			
SDA/SDO (Output)	T_{ACC}	Access time (read)	10	100	ns	Max CL=30pF
	T_{OH}	Output disable time (read)	15	100	ns	Min CL=8pF

Table 6.1: Parallel Interface Timing Characteristics (8080-Series MCU Interface)

CSX timings:
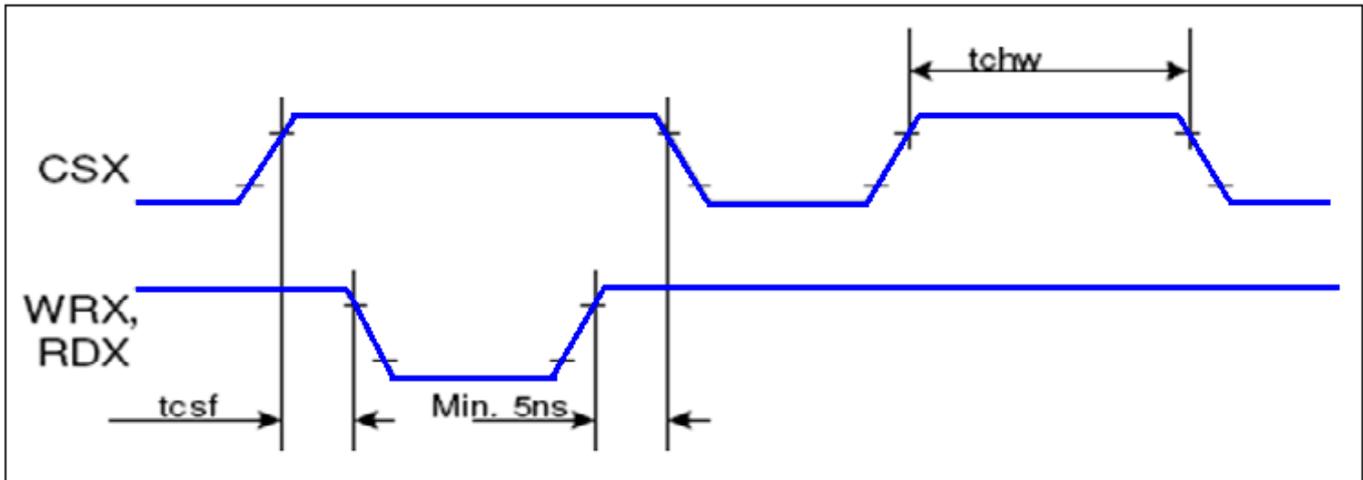
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

Write to read or read to write timings:
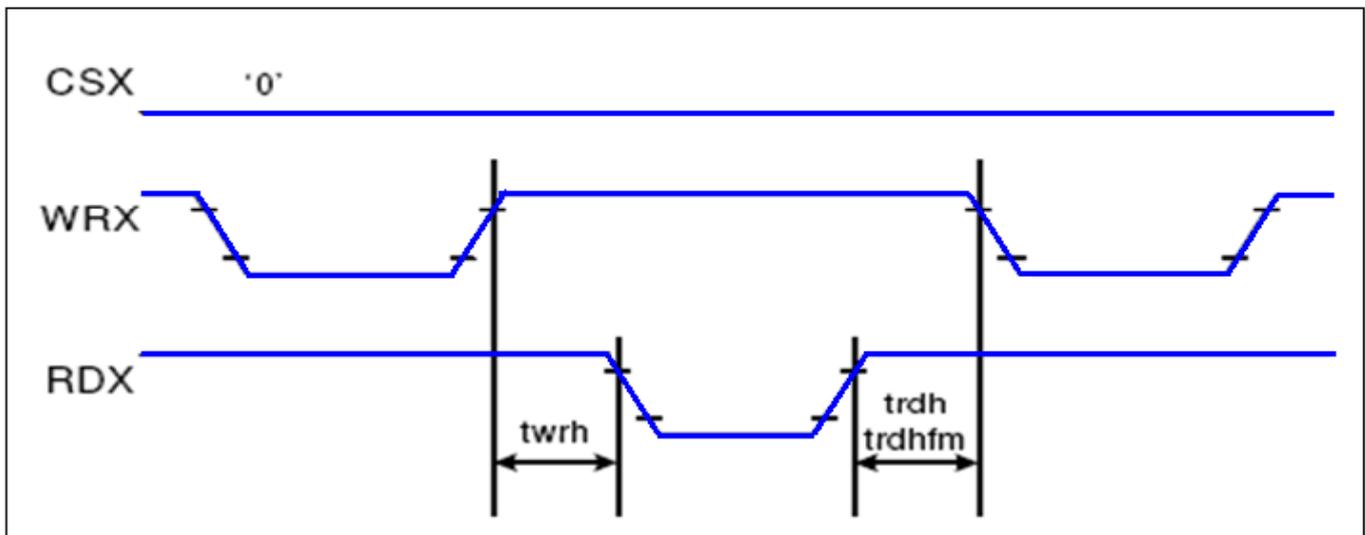
Note: Ta = -30 to 70 C, IOVCC = 1.65V to 2.8V, VCI = 2.5V to 3.3V, GND = 0V.
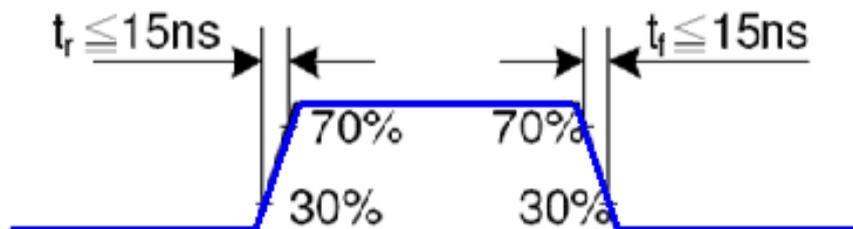
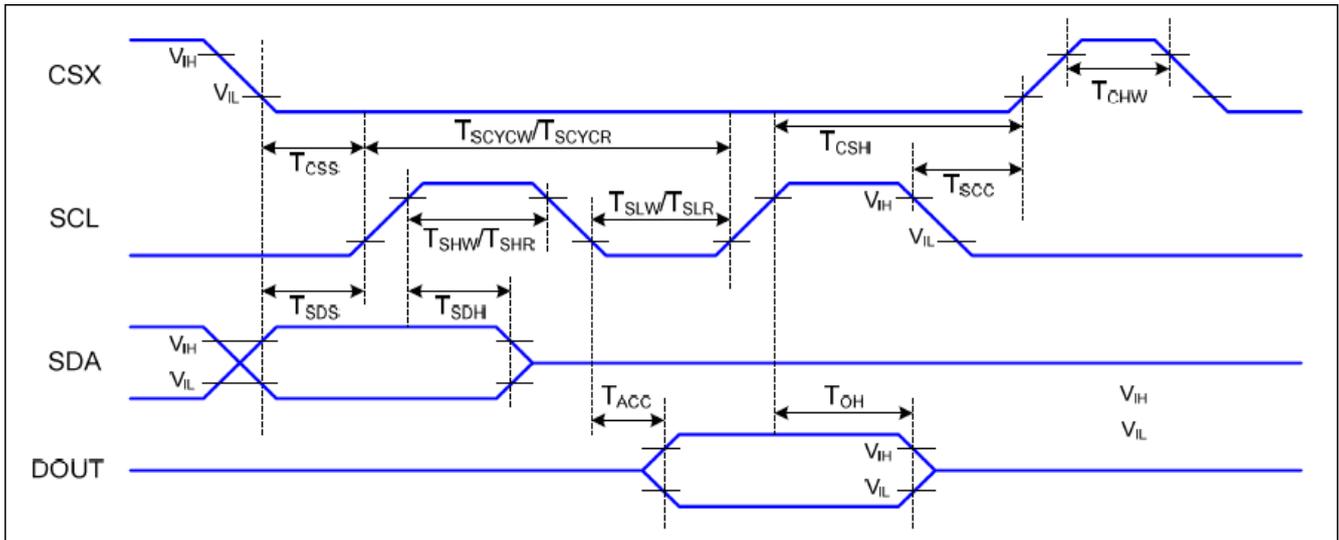## 6.2   Display Serial Interface Characteristics (3-line SPI system)

Figure 6.2: 3-line Serial Interface Timing Diagram

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C^o

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{SC}	SCL-CSX	15		ns	-
	T_{CSH}	Chip select hold time (write)	65		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	
	T_{SHW}	SCL "H" pulse width (write)	15		ns	
	T_{SLW}	SCL "L" width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL "H" pulse width (read)	60		ns	
	T_{SLR}	SCL "L" pulse width (read)	60		ns	
SDA/SDI (Input)	T_{SDS}	Data setup time (write)	10		ns	
	T_{SDH}	Data hold time (Write)	10			
SDA/SDO (Output)	T_{ACC}	Access time (read)	10	50	ns	Max CL=30pF
	T_{OH}	Output disable time (read)	15	50	ns	Min CL=8pF

Table 6.2: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

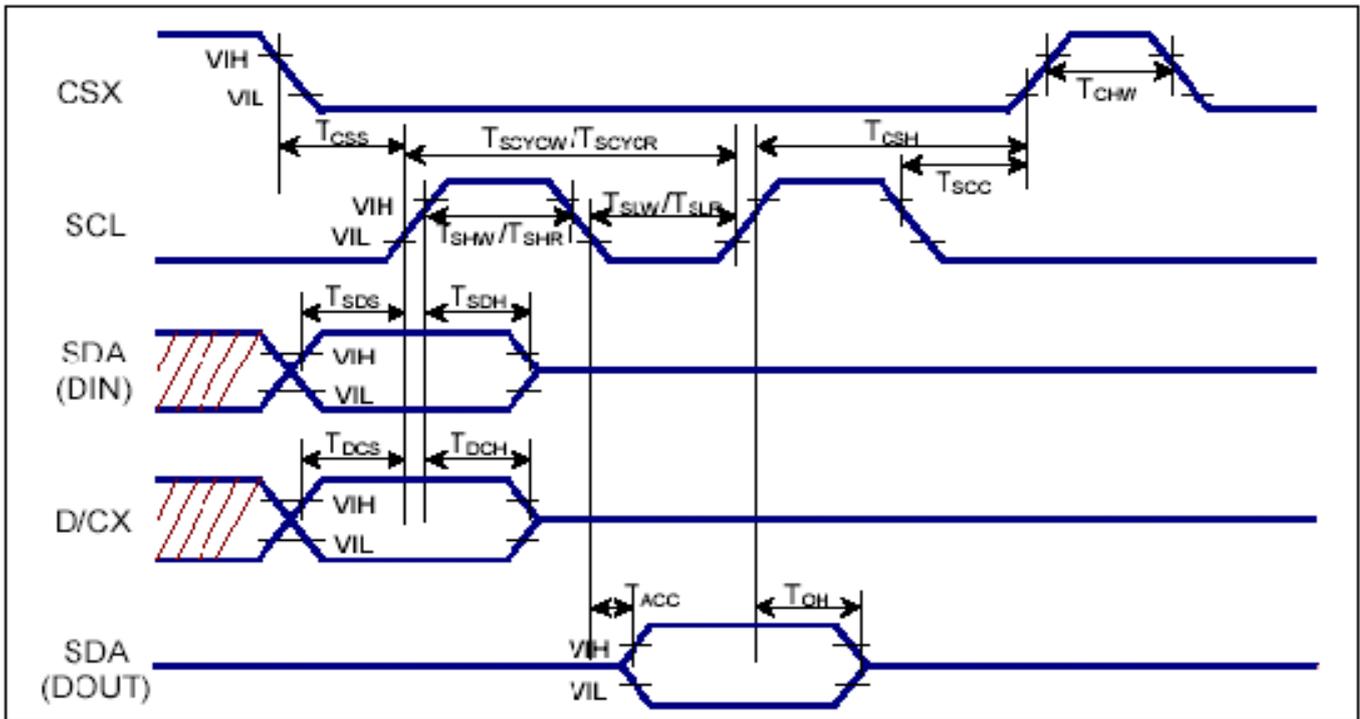## 6.3 Display Serial Interface Characteristics (4-line SPI serial)

Figure 6.3: 4-line SPI Serial Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (read)	15		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	50		ns	write command & data ram
	T_{SHW}	SCL "H" pulse width (write)	10		ns	
	T_{SLW}	SCL "L" width (write)	10		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	read command & data ram
	T_{SHR}	SCL "H" pulse width (read)	60		ns	
	T_{SLR}	SCL "L" pulse width (read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
SDA(DOUT)	T_{ACC}	Access time (read)	10	50	ns	For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table 6.3: 4-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.
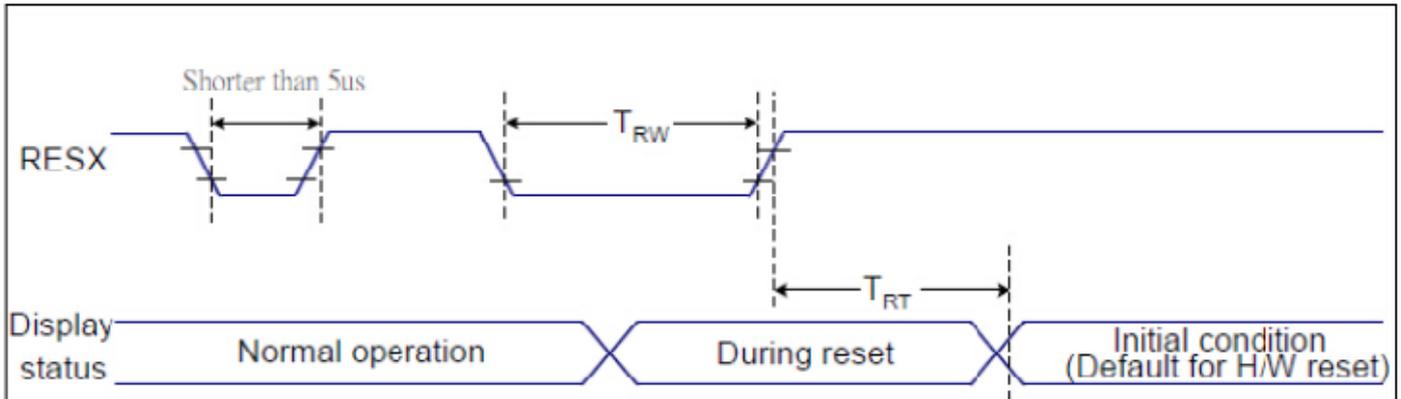
## 6.4 Reset Timing

Figure 4: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:
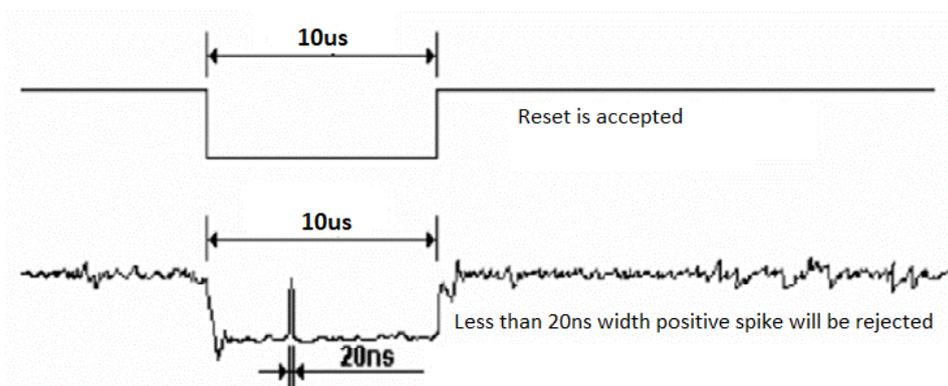
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating Temperature	T	-20	+70	℃	-
Storage Temperature	T_{ST}	-30	+80	℃	-

Note: If used beyond the absolute maximum ratings, FT6236 may permanently damage. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

### 7.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode current consumption	I_{OPr}	VDD=2.8V Ta=25℃ MCLK=17.5 MHz		4		mA	
Monitor mode current consumption	I_{mon}			1.5		mA	
Sleep mode current consumption	I_{sip}			50		uA	
Level input voltage	V_{IH}		0.7VDDIO		VDDIO	V	
	V_{IL}		-0.3		0.3VDDIO	V	
Level output voltage	V_{OH}	I_{OH}=-0.1mA	0.7VDDIO			V	
	V_{OL}	I_{OL}=0.1mA			0.3VDDIO	V	

7.1.3 AC Characteristics

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA=2.8V; Ta=25℃	34.65	35	35.35	MHz	
Sensor acceptable clock	ftx	VDDA=2.8V; Ta=25℃	0	100	300	kHz	
Sensor output rise time	Ttxr	VDDA=2.8V; Ta=25℃	-	100	-	Ns	
Sensor output fall time	Ttxf	VDDA=2.8V; Ta=25℃	-	80	-	Ns	
Sensor input voltage	Trxi	VDDA=2.8V; Ta=25℃	-	5	-	V	

7.1.4 I2C Interface

The I2C is always configured in the slave mode. The data transfer format is shown below.
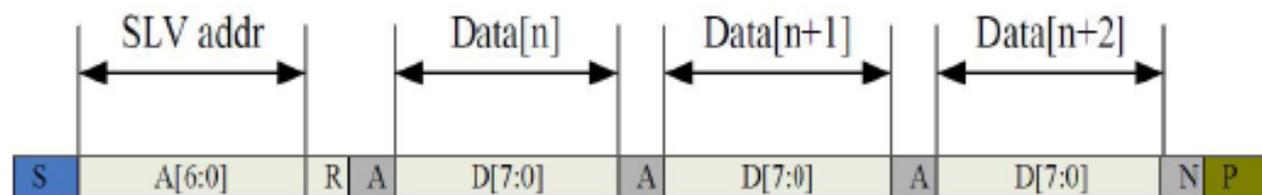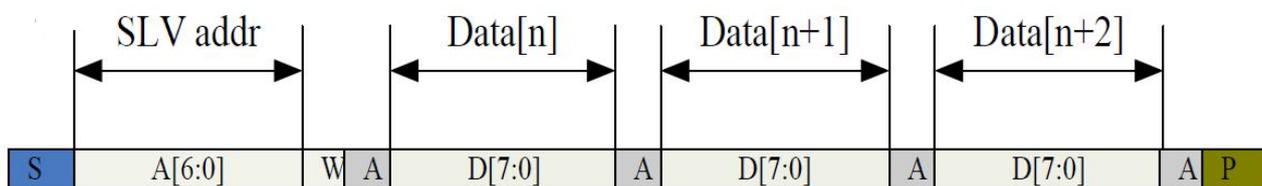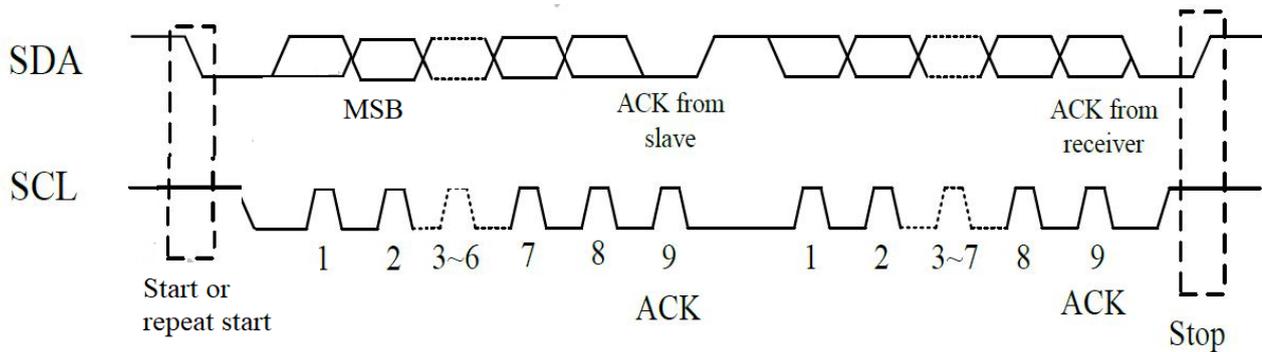
The following table lists the meanings of the mnemonics used in the above figures.

Mnemonics	Description
S	I2C start or I2C restart
A [6:0]	Slave address
R/W	Read/Write bit, '1' for read, '0' for write
A(N)	ACK(NACK)
P	Stop: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	kHz
Bus free time between a stop and start condition	4.7	-	us
Hold time (repeated) start condition	4.0	-	us
Data setup time	250	-	us
Setup time for a repeated start condition	4.7	-	us
Setup time for stop condition	4.0	-	us

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.