AFCT-725SMZ

25GE/10GE SFP+ for Single-Mode Optical Fiber
Digital Diagnostic SFP, 1310nm, Low Voltage (3.3V)
25GBASE-LR, Ethernet Optical Transceiver

Data Sheet

Description

Avago Technologies' AFCT-725SMZ optical transceiver supports high speed serial links over single-mode optical fiber at signalling rates up to 25.78Gb/s (the serial line rate of 25GE). The product is compliant with Small Form Pluggable industry agreements SFP and SFP+ for mechanical and low speed electrical specifications. High speed electrical and optical specifications are compliant with IEEE 802.3by for 25GBASE-LR.

The AFCT-725SMZ is a 1310nm transceiver which ensures compliance with 25GBASE-LR specifications. Per the requirements of 25GE, internal clock and data recovery circuits (CDRs) are present on both electrical input and electrical output of this transceiver. These CDRs will lock at 25.78Gb/s.

Digital diagnostic monitoring information (DMI) is present in the AFCT-725SMZ per the requirements of SFF-8472, providing real time monitoring information of transceiver laser, receiver and environment conditions over a SFF-8419 2-wire serial interface.

Related Products

- AFBR-89CDDZ: 850nm QSFP28 for 100GBASE-SR4
- AFBR-79EQDZ: 850nm QSFP+ for 40GBASE-SR4, 100m
- AFBR-79E3PZ: 850nm QSFP+ for 40GBASE-SR4, 300m
- AFBR-709ISMZ: 850nm SFP+ for 10GBASE-SR/SW, -40/85C
- AFBR-709SMZ: 850nm SFP+ for 10GBASE-SR/SW, 0/70C
- AFCT-709SM: 1310nm SFP+ for 10GBASE-LR, 0/70C

Patent - www.avagotech.com/patents

Features

- Compliant to RoHS directives
- 1310nm Distributed Feedback Laser (DFB)
- Class 1 eye safe per IEC60825-1 and CDRH
- Wide temperature range (0°C to 70°C)
- LC duplex connector optical interface conforming to ANSI TIA/EIA604-10 (FOCIS 10A)
- Diagnostic features per SFF-8472 "Diagnostic Monitoring Interface for Optical Transceivers"
- Enhanced operational features including variable electrical EQ/emphasis settings
- Real time monitoring of:
  - Transmitter average optical power
  - Received average optical power
  - Laser bias current
  - Temperature
  - Supply Voltage
- SFP+ mechanical specifications per SFF-8432
- SFP+ compliant low speed interface per SFF-8419
- Compliant to 25GBASE-LR 802.3cc and 802.3 Clause 52 10GBASE-LR specifications

Applications

- Ethernet switches (director, stand alone, blade)
- Ethernet NIC Cards/Adapters
- Port side connections
- Inter-switch or inter-chassis aggregated links

Transmitter Section

The transmitter section includes a Transmitter Optical Sub-Assembly (TOSA), laser driver circuit, Clock and Data Recovery circuit (CDR) and an electrical input stage with variable equalization controls. The TOSA contains a 1310nm Distributed Feedback Laser (DFB) light source with integral light monitoring function and imaging optics to assure efficient optical coupling to the LC connec-tor interface. The TOSA is driven by a laser driver IC, which uses the differential output from an integral Tx CDR stage to modulate and regulate laser optical power. As man-dated by 802.3, the integral CDR cleans up any incoming jitter accumulated from the host ASIC, PCB traces and SFP electrical connector. Between the SFP electrical connector and Tx CDR is a variable, 2-wire serial controlled, equalization circuit to optimize SFP performance with non-ideal incoming electrical waveforms.

Receiver Section

The receiver section includes a Receiver Optical Sub-As-sembly (ROSA), pre-amplification and post-amplification circuit, Clock and Data Recovery Circuit and an electrical output stage with variable emphasis controls. The ROSA, containing a high speed PIN detector, pre-amplifier and imaging optics efficiently couple light from the LC con-nector interface and perform an optical to electrical con-version. The resulting differential electrical signal passes through a post-amplification circuit and into a Clock and Data Recovery circuit (CDR) for cleaning up accumulated jitter.

Digital Diagnostics

The AFCT-725SMZ is compliant to the Diagnostic Monitoring Interface (DMI) defined in document SFF-8472. These features allow the host to access, via 2-wire serial, real time diagnostic monitors of transmit optical power, received optical power, temperature, supply voltage and laser op-erating current.

Low Speed Interfaces

Conventional low speed interface I/Os are available as defined in documents SFF-8419 to manage coarse and fine functions of the optical transceiver. On the transmit side, a Tx_DISABLE input is provided for the host to turn on and off the outgoing optical signal. A transmitter fault indicator output, Tx_FAULT, is available for the SFP to signal a host of a transmitter operational problem. A received optical power loss of signal indicator, RX_LOS, is available to advise the host of a receiver operational problem.

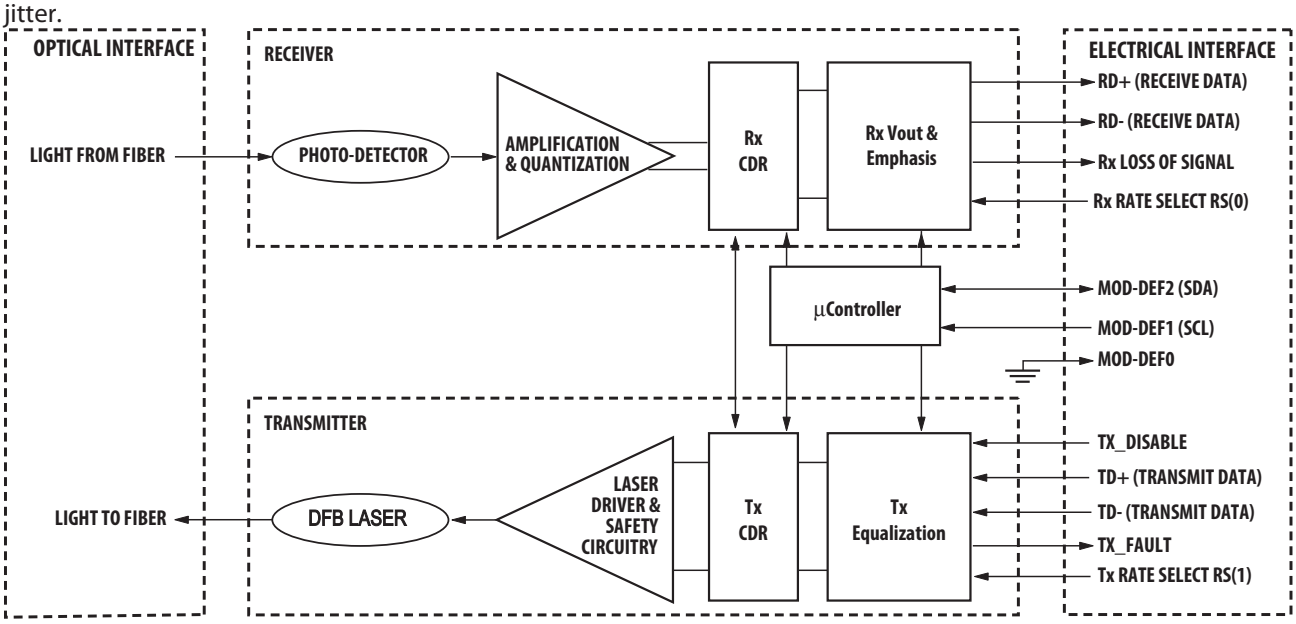


Figure 1. Transceiver functional diagram.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed contacts shall withstand 1000V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15kV air discharges during operation and 8kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10V/m field s ept from 80 MHz to 1 GHz applied to the module without a chassis enclosure
Laser Eye Safety and Equipment Type Testing TÜV Rheinland Product Safety | BAUART GEPRÜFT / TYPE APPROVED	US FDA CDRH AEL Class 1 US21 CFP, Subchapter J per Paragraphs 1002.10 and 1002.12 (IEC) EN60825-1:1994 +A11 +A2 (IEC) EN60825-2:1994 +A1 (IEC) EN60950:1992 +A1 +A2 +A3 +A4 +A11	CDRH Certification 9521220-224 TUV File: R50229221
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E484615
RoHS Compliance		Less than 1000 ppm of cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls (PPB) and polybrominated biphenyl ethers (PBDE).

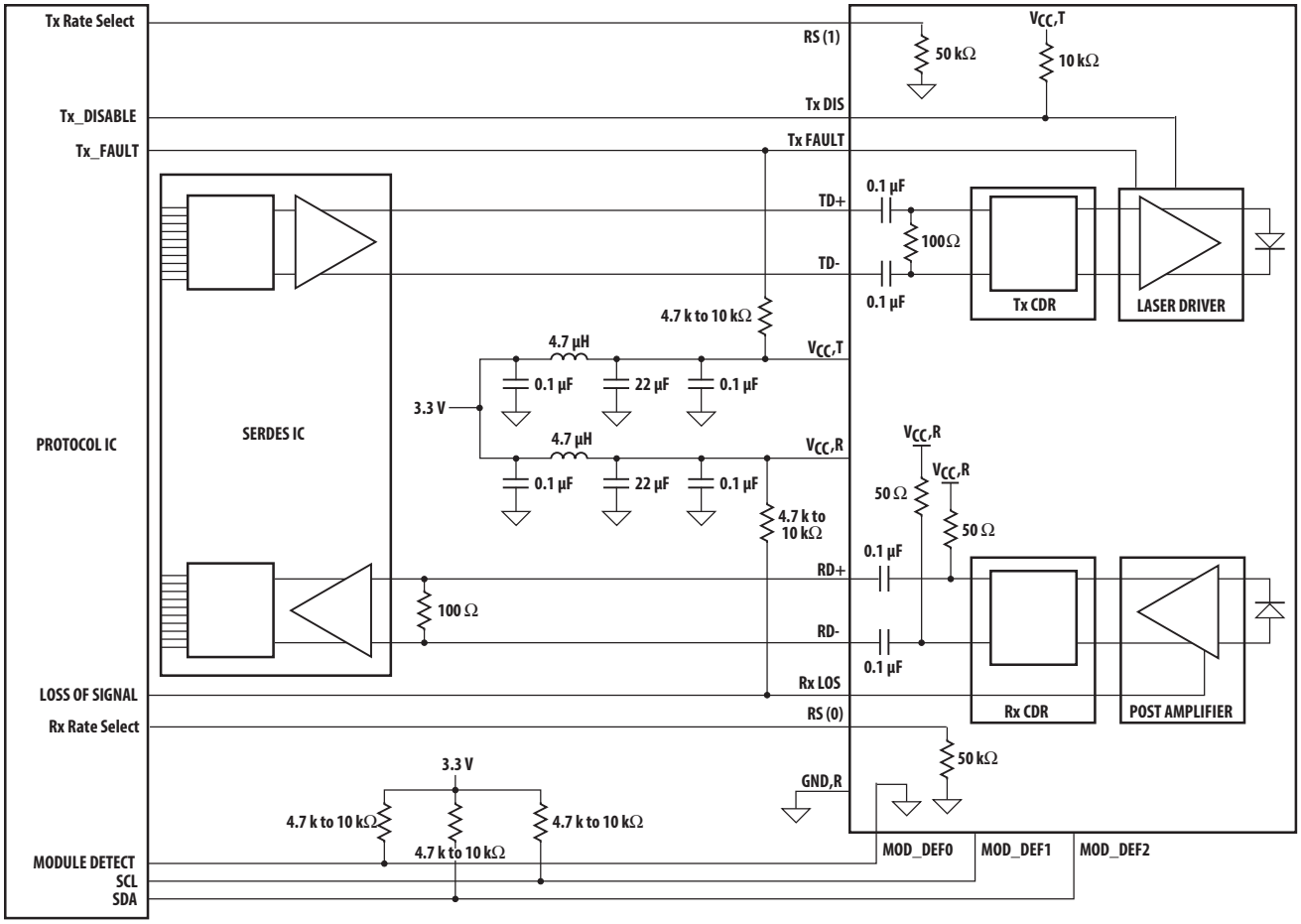
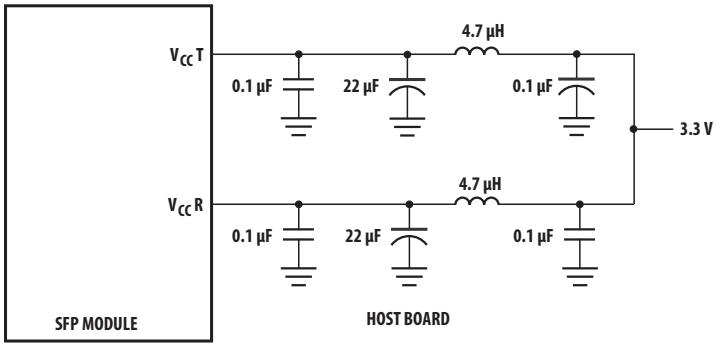


Figure 3. Typical application configuration



NOTE: INDUCTORS MUST HAVE LESS THAN 1Ω SERIES RESISTANCE TO LIMIT VOLTAGE DROP TO THE SFP MODULE.

Figure 4. Recommended power supply filter

Table 2. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	
2	TX_FAULT	Transmitter Fault Indication – High indicates a fault condition	Note 1
3	TX_DISABLE	Transmitter Disable – Module optical output disables on high or open	Note 2
4	MOD-DEF2	Module Definition 2 – Two wire serial ID interface data line (SDA)	Note 3
5	MOD-DEF1	Module Definition 1 – Two wire serial ID interface clock line (SCL)	Note 3
6	MOD-DEF0	Module Definition 0 – G ounded in module (module present indicator)	Note 3
7	Rx Rate Select, RS(0)	Receiver Rate Select. Logic High = 25.78Gb/s, Logic Low = 10.3Gb/s or other	Note 8
8	RX_LOS	Loss of Signal – High indicates loss of received optical signal	Note 4
9	Tx Rate Select, RS(1)	Transmitter Rate Select. Logic High = 25.78Gb/s, Logic Low = 10.3Gb/s or other	Note 8
10	VeeR	Receiver Ground	
11	VeeR	Receiver Ground	
12	RD-	Inverse Received Data Out	Note 5
13	RD+	Received Data Out	Note 5
14	VeeR	Receiver Ground	
15	VccR	Receiver Power + 3.3 V	Note 6
16	VccT	Transmitter Power + 3.3 V	Note 6
17	VeeT	Transmitter Ground	
18	TD+	Transmitter Data In	Note 7
19	TD-	Inverse Transmitter Data In	Note 7
20	VeeT	Transmitter Ground	

Notes

1. TX_FAULT is an open collector/drain output, which must be pulled up with a 4.7k – 10kΩ resistor on the host board. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.
2. TX_DISABLE is an input that is used to shut down the transmitter optical output. It is internally pulled up (within the transceiver) with a 6.8kΩ resistor.

Low (0 – 0.8V):	Transmitter on
Between (0.8V and 2.0V):	Undefine
High (2.0 – Vcc max) or OPEN:	Transmitter Disabled

3. The signals Mod-Def 0, 1, 2 designate the two wire serial interface pins. They must be pulled up with a 4.7k – 10kΩ resistor on the host board.
   Mod-Def 0 is grounded by the module to indicate the module is present
   Mod-Def 1 is serial clock line (SCL) of two wire serial interface
   Mod-Def 2 is serial data line (SDA) of two wire serial interface
4. RX_LOS (Rx Loss of Signal) is an open collector/drain output that must be pulled up with a 4.7k – 10kΩ resistor on the host board. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.
5. RD-/+ designate the differential receiver outputs. They are AC coupled 100Ω differential lines which should be terminated with 100Ω differential at the host SERDES input. AC coupling is done inside the transceiver and is not required on the host board. The voltage swing on these lines will be between 50 and 900 mV differential (25 – 450 mV single ended) when properly terminated.
6. VccR and VccT are the receiver and transmitter power supplies. They are defined at the SFP connector pin. The maximum supply current is 300 mA and the associated in-rush current will typically be no more than 30 mA above steady state after 500 nanoseconds.
7. TD-/+ designate the differential transmitter inputs. They are AC coupled differential lines with 100Ω differential termination inside the module. The AC coupling is done inside the module and is not required on the host board. The inputs will accept differential swings of 40 – 1200 mV (20 – 600 mV single ended), though it is recommended that values between 50 and 900 mV differential (25 – 450 mV single ended) be used for best EMI performance.
8. RATE_SELECT is an input used to control transmitter and receiver compliance among multiple rates. It is internally pulled down with a 40kΩ resistor.

Low (0 - 0.8V) or OPEN:	Low Bit Rate Compatible (10.3 Gb/s or other)
Between (0.8V and 2.0V):	Undefined per SFF-8074i
High (2.0 – Vcc max):	High Bit Rate Compliance (25.78Gb/s)

Table 3. Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the module concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	T_S	-40	85	°C	Note 1
Case Operating Temperature	T_C	-40	85	°C	
Relative Humidity	RH	5	95	%	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Low Speed Input Voltage	V_I	-0.5	Vcc+0.5, 3.6	V	

Table 4. Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the optical and electrical characteristics hold unless otherwise noted. Optical and electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min.	Typ.	Max.	Units	Reference
Case Operating Temperature	Tc	0		70	°C	Note 2
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate		10.3125	25.78125		Gb/s	Note 3
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	Note 4

Table 5. Transceiver Electrical Characteristics

The following characteristics are defined ver the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbols	Min.	Typ.	Max.	Units	Reference
Transceiver Power Consumption				1.5	W	
Transceiver Power Supply Current				300	mA	
Power Supply Noise Rejection (peak-peak)	PSNR			66	mV	Note 5
Low Speed Outputs:	I_{OH}	-50		37.5	µA	Note 6
TX_FAULT, RX_LOS, MOD_DEF2	V_{OL}			0.4	V	
Low Speed Inputs	V_{IH}	2.0		Vcc	V	Note 7
TX_DIS, MOD_DEF1, MOD_DEF2, RS(0), RS(1)	V_{OL}	0		0.8	V	

Notes:

1. Absolute maximum ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheet for specific eliability performance. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.
2. The position of case temperature measurement is shown in Figure 9. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability.
3. 25GE requires FEC RS(528,514) encoding per IEEE 802.3.
4. With 500us clock stretch per SFF-8419
5. Filter per SFP specific tion is required on the host board to remove 10Hz to 2MHz content.
6. Pulled up externally with a 4.7k-10kΩ resistor on the host board to 3.3V
7. Mod_Def1 and Mod_Def2 must be pulled up externally with a 4.7k-10kΩ resistor on the host board to 3.3V

Table 6. High Speed Electrical Module Input Characteristics

From CAUI-4, 802.3 Clause 83E, Table 83E-7. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate, Per Lane	TP1		25.78125		GBd	± 100 ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Input Return Loss. min	TP1		Eq 83E-5		dB	802.3
Common Mode to Differential Input Return Loss, min	TP1		Eq 83E-6		dB	802.3
Differential Termination Mismatch	TP1			10	%	
Module stressed input test	TP1a		83E.3.4.2			802.3, below
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode output voltage	TP1a	-0.350		2.85	V	Note 8
Electrical Input LOS Assert Threshold, Differential Peak-to-Peak Voltage Swing	ΔVdi pp los	50			mVpp	
LOS Hysteresis		0.5		4	dB	Note 9

Parameter	Value	Units	Notes/Conditions
Module stressed input test			Note 10
Eye width	0.46	UI	
Applied pk-pk sinusoidal jitter	Table 88-13		802.3
Eye height	95	mV	

Notes:

8. DC common mode voltage generated by the host. Specific tion includes effects of ground offset voltage.
9. LOS Hysteresis is defined as 20*log(LOS De-assert Level / LOS Assert Level).
10. Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1

Table 7. Reference Points

Test Point	Description
TP0	Host ASIC transmitter output at ASIC package pin on a DUT board
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input
TP1a	Host ASIC transmitter output across the Host Board and Host Edge Card connector at the output of the host compliance board
TP2	Optical transmitter output as measured at the end of a 2-5m patch cord mated to the optical module
TP3	Optical test point as measured at the end of an optical fiber cable; closest est point to the presumed optical receiver input.
TP4	Module output through mated module and host edge card connector through module compliance board
TP4a	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input
TP5	Input to host ASIC

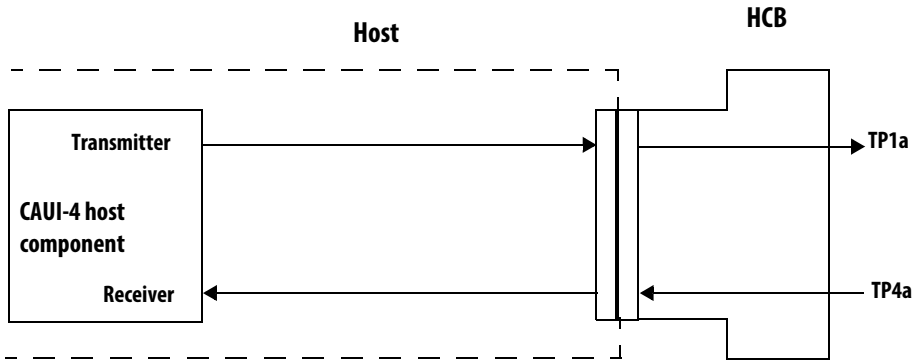


Figure 83E–4—Host CAUI-4 Compliance Points

Figure 5. IEEE 802.3 CAUI-4 compliance points TP1a, TP4a

Note a reference receiver is used to measure host eye width and eye height at TP1a. The reference receiver includes a selectable continuous time linear equalizer (CTLE) which is described by Equation (83E–4, below) with coefficients given in Table 83E–2.

$$H(f) = \frac{GP_1P_2}{Z_1}$$

where:
$H(f)$ is the CTLE transfer function, f is the frequency in GHz
G is the CTLE gain
P_1, P_2 are the CTLE poles in Grad/s
Z_1 is the CTLE zero in Grad/s

Table 83E-2 - Reference CTLE coefficients

Peaking (dB)	G	$P_1/2\pi$	$P_2/2\pi$	$Z_1/2\pi$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672
10	0.31623	15.6	14.1	2.3715

Table 8. High Speed Electrical Module Output Characteristics

From CAUI-4, 802.3 Clause 83E, Table 83E-3. The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate, Per Lane	TP4		25.78125		GBd	± 100 ppm
Common Mode AC Output Voltage, RMS	TP4			17.5	mV, rms	
Differential Output Voltage	TP4			900	mV	
Eye Width	TP4	0.57			UI	
Eye Height, Differential	TP4	228			mV	
Vertical Eye Closure	TP4			5.5	dB	
Differential Output Return Loss, min	TP4		Eq 83E-2		dB	802.3
Common to Differential Mode Conversion, min	TP4		Eq 83E-3		dB	802.3
Differential termination mismatch	TP4			10	%	
Transition Time (20% to 80%)	TP4	12			ps	
DC common mode voltage	TP4	-0.35		2.85	V	Note 11

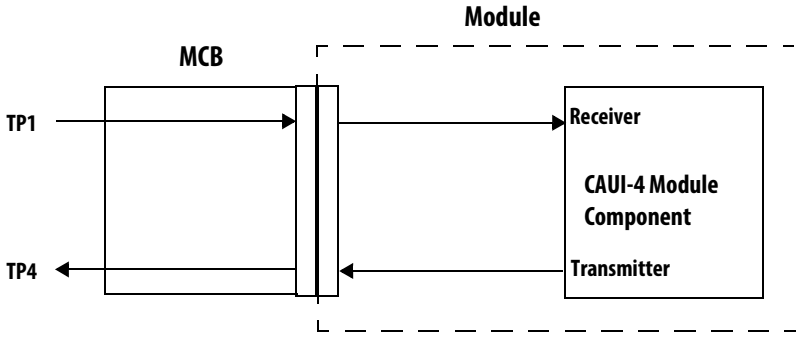


Figure 83E–5—Module CAUI-4 Compliance Points

Figure 6. IEEE 802.3 CAUI-4 compliance points TP1, TP4

Notes:
11. DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

Table 9. High Speed Optical Transmitter Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Test Point*	Min.	Typ.	Max.	Units	Notes/Conditions
Signaling Rate (range)			25.78125		GBd	± 100ppm
Center wavelength (range)	TP2	1295		1325	nm	
Side-mode suppression ratio	TP2	30			dB	
Average launch power	TP2	-7.0[12]	-	+2.0	dBm	
Optical Modulation Amplitude (OMA)	TP2	-4.0 [13]	-	+2.2	dBm	
Launch Power in OMA minus TDP	TP2	-5.0			dBm	
Transmitter and dispersion penalty (TDP)	TP2			2.7	dB	
Average launch power of OFF transmitter	TP2	-		-30	dBm	
Extinction ratio	TP2	3.0	-	-	dB	
Optical return loss tolerance	TP2			20	dB	
Transmitter reflectance [14]	TP2			-26		Type A1a.2 50um Fiber per IEC 61280-1-4
Transmitter Eye Mask definition: {X1, X2, X3, Y1, Y2, Y3}	TP2	SPECIFICATION VALUES {0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				Hit Ratio 5 x 10-5 hits per sample

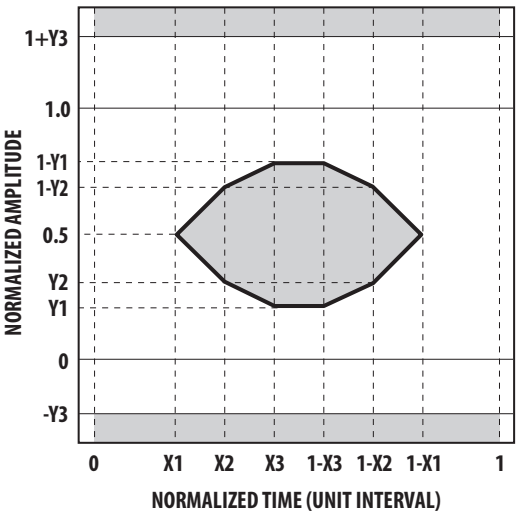


Figure 7. Transmitter eye mask definitions

Notes:

12. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
13. Even if the TDP < 1dB, the OMA (min) must exceed this value.
14. Transmitter reflectance is defined looking into the transmitter.

Table 10. Receiver Optical Characteristics

(Tc = 0°C to 70°C, VccT, VccR = 3.3V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Signaling Rate (range)			25.78125		GBd	± 100ppm
Center wavelength (range)		1295		1325	nm	
Damage threshold		3.0			dBm	
Average receive power (Overload)	Pavg			2.0	dBm	
Receive power (OMA, Overload)	OMA			2.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMA)				-12.0	dBm	Note 1
Stressed receiver sensitivity (OMA)				-9.5	dBm	Note 1
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty				2.5	dB	
Stressed eye J2 Jitter				0.27	UI	
Stressed eye J4 Jitter				0.39	UI	
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.31, 0.40, 0.45, 0.34, 0.38, 0.40}				
Loss of Signal – Assert	Pa	-30			dBm,OMA	
Loss of Signal – De-asserted	P_D			-11	dBm,OMA	
Loss of Signal – Hysteresis	$P_A - P_D$	0.5			dB	

Notes:
1. Assumes a FEC encoded RS(528, 514) signal and allows a BER of 1E-6.

Table 11. Transceiver SOFT DIAGNOSTIC Timing Characteristics

(T_C = 0°C to 70°C, VccT, VccR = 3.3V ± 5%)

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Hardware TX_DISABLE Assert Time	t_off		100	µs	Note 1
Hardware TX_DISABLE Negate Time	t_on		2	ms	Note 2
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Note 3
Hardware TX_FAULT Assert Time	t_fault_on		1	ms	Note 4
Hardware TX_DISABLE to Reset	t_reset	10		µs	Note 5
Hardware RX_LOS DeAssert Time	t_los_on		100	µs	Note 6
Hardware RX_LOS Assert Time	t_los_off		100	µs	Note 7
Software TX_DISABLE Assert Time	t_off_soft		100	ms	Note 8
Software TX_DISABLE Negate Time	t_on_soft		100	ms	Note 9
Software Tx_FAULT Assert Time	t_fault_soft		100	ms	Note 10
Software Rx_LOS Assert Time	t_los_on_soft		100	ms	Note 11
Software Rx_LOS De-Assert Time	t_los_off_soft		100	ms	Note 12
Analog parameter data ready	t_data		1000	ms	Note 13
Serial bus hardware ready	t_serial		300	ms	Note 14
Serial bus buffer time	t_buf	20		µs	Note 15
Complete Single or Sequential Write up to 4 Byte	twR		40	ms	Note 16
Complete Sequential Write of 5-8 Byte	twR		80	ms	Note 16
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Note 17
Serial ID Clock Rate	f_serial_clock		400	kHz	Note 18

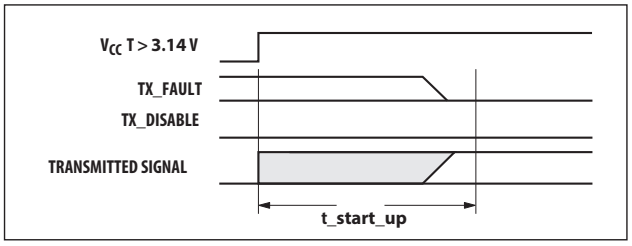
Notes

1. Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
3. Time from power on or falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal.
4. From power on or negation of TX_FAULT using TX_DISABLE.
5. Time TX_DISABLE must be held high to reset the laser fault shutdown circuitry.
6. Time from loss of optical signal to Rx_LOS Assertion.
7. Time from valid optical signal to Rx_LOS De-Assertion.
8. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
9. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output rises above 90% of nominal.
10. Time from fault to two-wire interface TX_FAULT (A2h, byte 110, bit 2) asserted.
11. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
12. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
13. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
14. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
15. Time between START and STOP commands.
16. Time from stop bit to completion of a write command.
17. Maximum time the SFP+ module may hold the SCL line low before continuing with a read or write operation.
18. With a maximum Clock Stretch of 500us. A maximum of 100kHz operation can be supported without a Clock Stretch.

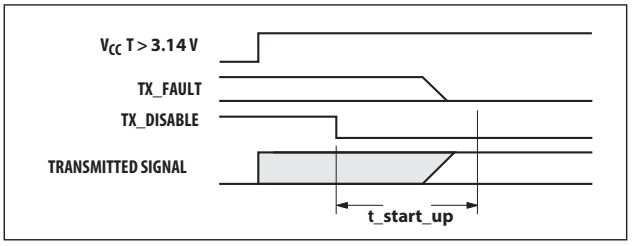
Table 12. Transceiver Digital Diagnostic Monitor (Real Time Sense) Characteristics

(T_C = 0°C to 70°C, VccT, VccR = 3.3V ± 5%)

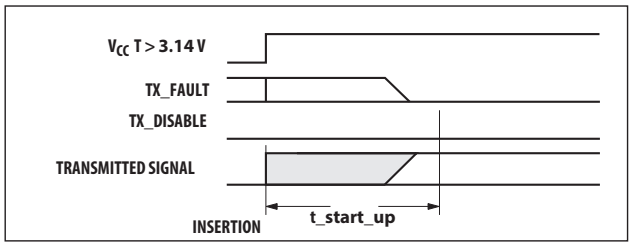
Parameter	Symbol	Min.	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	± 3.0	°C	Temperature is measured internal to the transceiver. Valid from = 0°C to 70 °C case temperature.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	± 0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP Vcc pin. Valid over 3.3 V ± 5%.
Transmitter Laser DC Bias Current Accuracy	I_{INT}	± 10	%	I_{INT} is better than ±10% of the nominal value.
Transmitted Average Optical Output Power Accuracy	P_T	± 3.0	dB	Coupled into 9um single-mode fiber. Valid from -7dBm to +2dBm avg.
Received Optical Input Power Accuracy	P_R	± 3.0	dB	Coupled from 9um multi-mode fiber. Valid from -12.8dBm to +2dBm avg.



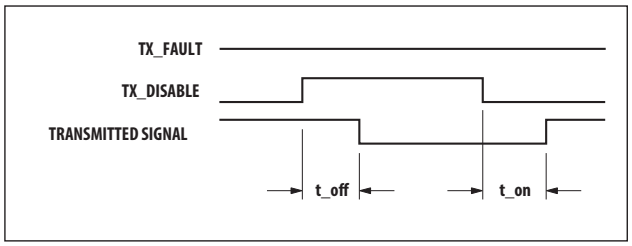
t_start_up: TX DISABLE NEGATED



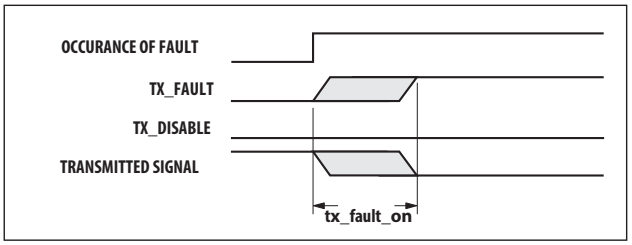
t_start_up: TX DISABLE ASSERTED



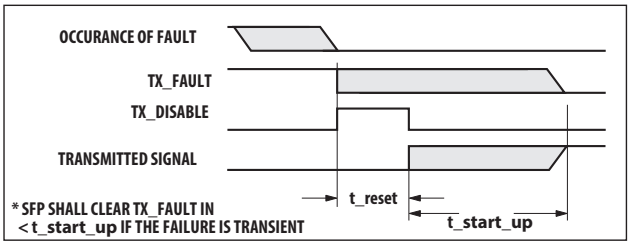
t_start_upt: TX DISABLE NEGATED, MODULE HOT PLUGGED



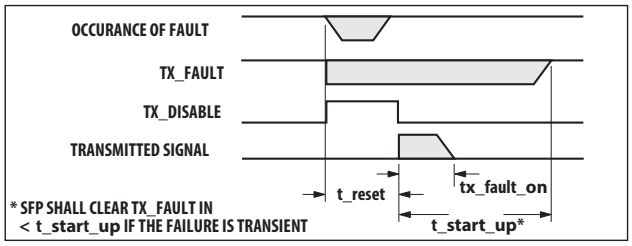
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



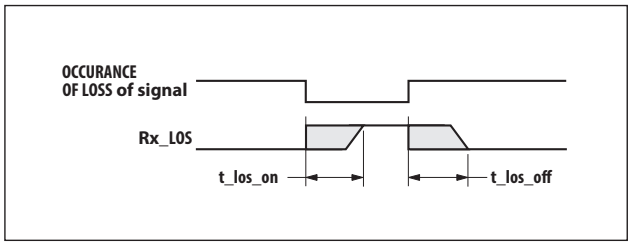
tx_fault_on: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED



t_reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



tx_fault_on: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL NOT RECOVERED



t_los_on & t_los_off

Figure 8. Transceiver timing diagrams (module installed except where noted)

Table 13. EEPROM Serial ID Memory Contents – Address A0h

Byte # Decimal	Hex	Description	Byte # Decimal	Hex	Description
0	03	SFP physical device	37	00	Hex Byte of Vendor OUI [1]
1	04	SFP function defined y serial ID only	38	17	Hex Byte of Vendor OUI [1]
2	07	LC optical connector	39	6A	Hex Byte of Vendor OUI [1]
3	00		40	41	"A" - Vendor Name ASCII Character
4	00		41	46	"F" - Vendor Name ASCII Character
5	00		42	43	"C" - Vendor Name ASCII Character
6	00		43	54	"T" - Vendor Name ASCII Character
7	00		44	2D	"-" - Vendor Name ASCII Character
8	00		45	37	"7" - Vendor Name ASCII Character
9	01		46	32	"2" - Vendor Name ASCII Character
10	00		47	35	"5" - Vendor Name ASCII Character
11	07	256B/257B (transcoded FEC-enabled data)	48	53	"S" - Vendor Name ASCII Character
12	FF	Greater than 25.5Gb/s (See Address 66)	49	4D	"M" - Vendor Name ASCII Character
13	00		50	5A	"Z" - Vendor Name ASCII Character
14	0A	10km of single mode fiber at 25GE	51	20	" " - Vendor Name ASCII Character
15	64	10km of single mode fiber at 25GE	52	20	" " - Vendor Name ASCII Character
16	00		53	20	" " - Vendor Name ASCII Character
17	00		54	20	" " - Vendor Name ASCII Character
18	00		55	20	" " - Vendor Name ASCII Character
19	00		56	20	" " - Vendor Name ASCII Character
20	41	"A" - Vendor Name ASCII Character	57	20	" " - Vendor Name ASCII Character
21	56	"V" - Vendor Name ASCII Character	58	20	" " - Vendor Name ASCII Character
22	41	"A" - Vendor Name ASCII Character	59	20	" " - Vendor Name ASCII Character
23	47	"G" - Vendor Name ASCII Character	60	05	Hex Byte of Laser Wavelength [2]
24	4F	"O" - Vendor Name ASCII Character	61	1E	Hex Byte of Laser Wavelength [2]
25	20	" " - Vendor Name ASCII Character	62	00	
26	20	" " - Vendor Name ASCII Character	63		Checksum for Bytes 0-62 [3]
27	20	" " - Vendor Name ASCII Character	64	0A	CDRs present. 1.5W power level 2
28	20	" " - Vendor Name ASCII Character	65	3A	Hardware Tx_Disable, Tx_Fault, Rx_LOS, Rate Select
29	20	" " - Vendor Name ASCII Character	66	67	25.78 Mbit/sec nominal bit rate (25GE)
30	20	" " - Vendor Name ASCII Character	67	00	
31	20	" " - Vendor Name ASCII Character	68 - 83		Vendor Serial Number ASCII characters [4]
32	20	" " - Vendor Name ASCII Character	84 - 91		Vendor Date Code ASCII characters [5]
33	20	" " - Vendor Name ASCII Character	92	68	Digital diagnostics, Internal Cal, Rx Pwr Avg
34	20	" " - Vendor Name ASCII Character	93	FA	Alarms/Warnings, Software Tx_Disable, Tx-Fault, Rx_LOS, Rate_Select
35	20	" " - Vendor Name ASCII Character	94	08	SFF-8472 compliance to revision 12.2
36	03	25GBASE-LR	95		Checksum for Bytes 62-94 [3]
			96 – 255	00	

Notes:

1. The IEEE Organizationally Unique Identified (OUI) assigned to Avago Technologies is 00-17-6A (3 bytes of hex).
2. Laser Wavelength is represented in 16 unsigned buts. The hex representation of 1310nm is 051E.
3. Addresses 63 and 95 are checksums calculated (per SFF-8472 and SFF-8074) and stored prior to product shipment.
4. Address 68-83 specify the AFCT-725SMZ ASCII serial number and will vary on a per unit basis.
5. Address 84-91 specify the AFCT-725SMZ ASCII data code and will vary on a per date code basis.

Table 14. EEPROM Serial ID Memory Contents - Enhanced SFP Memory (Address A2h)

Byte # Decimal	Notes	Byte # Decimal	Notes	Byte # Decimal	Notes
0	Temp H Alarm MSB [1]	26	Tx Power L Alarm MSB [4]	104	Real Time Rx Power MSB [5]
1	Temp H Alarm LSB [1]	27	Tx Power L Alarm LSB [4]	105	Real Time Rx Power LSB [5]
2	Temp L Alarm MSB [1]	28	Tx Power H Warning MSB [4]	106	Reserved
3	Temp L Alarm LSB [1]	29	Tx Power H Warning LSB [4]	107	Reserved
4	Temp H Warning MSB [1]	30	Tx Power L Warning MSB [4]	108	Reserved
5	Temp H Warning LSB [1]	31	Tx Power L Warning LSB [4]	109	Reserved
6	Temp L Warning MSB [1]	32	Rx Power H Alarm MSB [5]	110	Status/Control – See Table 16
7	Temp L Warning LSB [1]	33	Rx Power H Alarm LSB [5]	111	Reserved
8	Vcc H Alarm MSB [2]	34	Rx Power L Alarm MSB [5]	112	Flag Bits – See Table 17
9	Vcc H Alarm LSB [2]	35	Rx Power L Alarm LSB [5]	113	Flag Bits – See Table 17
10	Vcc L Alarm MSB [2]	36	Rx Power H Warning MSB [5]	114	Tx Input EQ Control - See Table 20, 21
11	Vcc L Alarm LSB [2]	37	Rx Power H Warning LSB [5]	115	Rx Output Emphasis Control - See Table 22, 23
12	Vcc H Warning MSB [2]	38	Rx Power L Warning MSB [5]	116	Flag Bits – See Table 17
13	Vcc H Warning LSB [2]	39	Rx Power L Warning LSB [5]	117	Flag Bits – See Table 17
14	Vcc L Warning MSB [2]	40-55	Optional Alarm and Warning	118	Status/Control – See Table 17
15	Vcc L Warning LSB [2]	56-94	External Calibration Constants [6]	119	CDR Loss of Lock Status - See Table 19
16	Tx Bias H Alarm MSB[3]	95	Checksum for Bytes 0-94 [7]	120-126	Reserved
17	Tx Bias H Alarm LSB[3]	96	Real Time Temperature MSB [1]	127	Page Select Control
18	Tx Bias L Alarm MSB [3]	97	Real Time Temperature LSB [1]	128-247	Customer Writable
19	Tx Bias L Alarm LSB[3]	98	Real Time Vcc MSB [2]	248-255	Vendor Specifi
20	Tx Bias H Warning MSB[3]	99	Real Time Vcc LSB [2]		
21	Tx Bias H Warning LSB[3]	100	Real Time Tx Bias MSB [3]		
22	Tx Bias L Warning MSB [3]	101	Real Time Tx Bias LSB [3]		
23	Tx Bias L Warning LSB[3]	102	Real Time Tx Power MSB [4]		
24	Tx Power H Alarm MSB [4]	103	Real Time Tx Power LSB [4]		
25	Tx Power H Alarm LSB [4]				

Notes:
1. Temperature (Temp) is decoded as a 16 bit signed two's complement integer in increments of 1/256 °C.
2. Supply Voltage (Vcc) is decoded as a 16 bit unsigned integer in increments of 100 μV.
3. Tx bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 μA.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
6. Bytes 56-94 are not intended for use, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

Table 15. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110)

Bit #	Status/Control Name	Description	Notes
7	TX_DISABLE State	Digital state of TX_DISABLE Input Pin (1 = TX_DISABLE asserted)	Note 1
6	Soft TX_DISABLE Control	Read/write bit for changing digital state of TX_DISABLE function	Note 1, 2
5	RS(1) State	Digital state of TX Rate_Select Input Pin RS(1) (1 = Rate High asserted)	
4	RS(0) State	Digital state of RX Rate_Select Input Pin RS(0) (1 = Rate High asserted)	
3	Soft RS(0) Control	Read/write bit for changing digital state of Rx Rate_Select RS(0) function	Note 3
2	TX_FAULT State	Digital state of TX_FAULT Output Pin (1 = TX_FAULT asserted)	Note 1
1	RX_LOS State	Digital state of SFP RX_LOS Output Pin (1 = RX_LOS asserted)	Note 1
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = Data Ready)	

Notes:

1. The response time for soft commands of the AFCT-725SMZ is 100msec as specified by MSA SFF-8472.
2. Bit 6 is log OR'd with the SFP TX_DISABLE input pin 3 …. either asserted will disable the SFP transmitter.
3. Bit 3 is logic OR'd with the SFP RS(0) RX Rate_Select input pin 7 …. either asserted will set receiver to Rate = High.

Table 16. EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

Byte	Bit	Flag Bit Name	Description
112	7	Temp High Alarm	Set when transceiver internal temperature exceeds high alarm threshold.
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds low alarm threshold.
	5	Vcc High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold.
	4	Vcc Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold.
	3	Tx Bias High Alarm	Set when transceiver laser bias current exceeds high alarm threshold.
	2	Tx Bias Low Alarm	Set when transceiver laser bias current exceeds low alarm threshold.
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold.
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold.
113	7	Rx Power High Alarm	Set when received average optical power exceeds high alarm threshold.
	6	Rx Power Low Alarm	Set when received average optical power exceeds low alarm threshold.
	0-5	reserved	
116	7	Temp High Warning	Set when transceiver internal temperature exceeds high warning threshold.
	6	Temp Low Warning	Set when transceiver internal temperature exceeds low warning threshold.
	5	Vcc High Warning	Set when transceiver internal supply voltage exceeds high warning threshold.
	4	Vcc Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold.
	3	Tx Bias High Warning	Set when transceiver laser bias current exceeds high warning threshold.
	2	Tx Bias Low Warning	Set when transceiver laser bias current exceeds low warning threshold.
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold.
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold.
117	7	Rx Power High Warning	Set when received average optical power exceeds high warning threshold.
	6	Rx Power Low Warning	Set when received average optical power exceeds low warning threshold.
	0-5	reserved	

Table 17. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 118)

Bit #	Status/Control Name	Description	Notes
4-7	Reserved		
3	Soft RS(1) Control	Read/write bit for changing digital state of Tx Rate_Select RS(1) function	Note 1
2	Reserved		
1	Power Level State	Always set to zero.	
0	Power Level Select	Unused.	

Notes:
1. Bit 3 is log OR'd with the SFP RS(1) TX Rate_Select input pin 9 …. either asserted will set transmitter to Rate = High.

Table 18. EEPROM Serial ID Memory Contents – CDR Loss of Lock (LOL) Status Indicators (Address A2h, Byte 119).

Bit #	Status/Control Name	Description
7-2	Reserved	
1	Tx CDR LOL Flag	A value of 0 indicates the CDR is locked. A value of 1 indicates CDR loss of lock.
0	Rx CDR LOL Flag	A value of 0 indicates the CDR is locked. A value of 1 indicates CDR loss of lock.

Table 19. EEPROM Serial ID Memory Contents – Transmitter Input Electrical Equalization Control (Address A2h, Byte 114).

Bit #	Status/Control Name	Description
7-4	TX EQ, RS(1)=HIGH	Selects an input equalization value per Table 9-13 of SFF-8472
3-0	TX EQ, RS(1)=LOW	Not Applicable.

Table 20. Transmitter Input Equalization Control Values (Address A2h, Byte 114)

From Table 9-13 of SFF-8472

	Transmitter Input Equalization	
Code	Nominal	Units
11xx	Reserved	
1011	Reserved	
1010	10	dB
1001	9	dB
1000	8	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No Equalization

Table 21. EEPROM Serial ID Memory Contents – Receiver Output Electrical Emphasis Control (Address A2h, Byte 115).

Bit #	Status/Control Name	Description	Notes
7-4	RX EMPH, RS(0)=HIGH	Selects an output emphasis value per Table 9-14 of SFF-8472	
3-0	RX EMPH, RS(0)=LOW	Not Applicable.	

Table 22. Receiver Output Emphasis Control Values (Address A2h, Byte 115)

From Table 9-14 of SFF-8472

	Receiver Output Emphasis At nominal Output Amplitude	
Code	**Nominal**	**Units**
1xxx	Vendor Specifi	
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No Emphasis

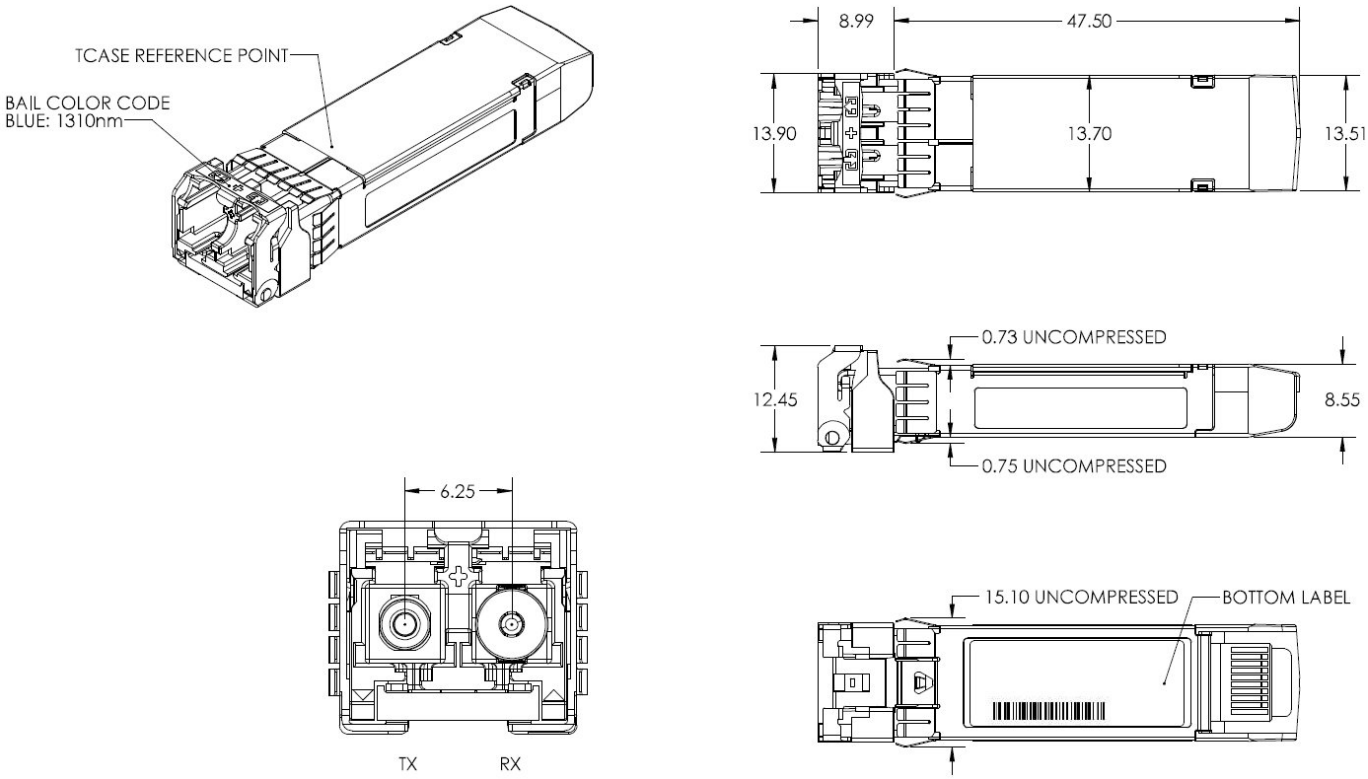
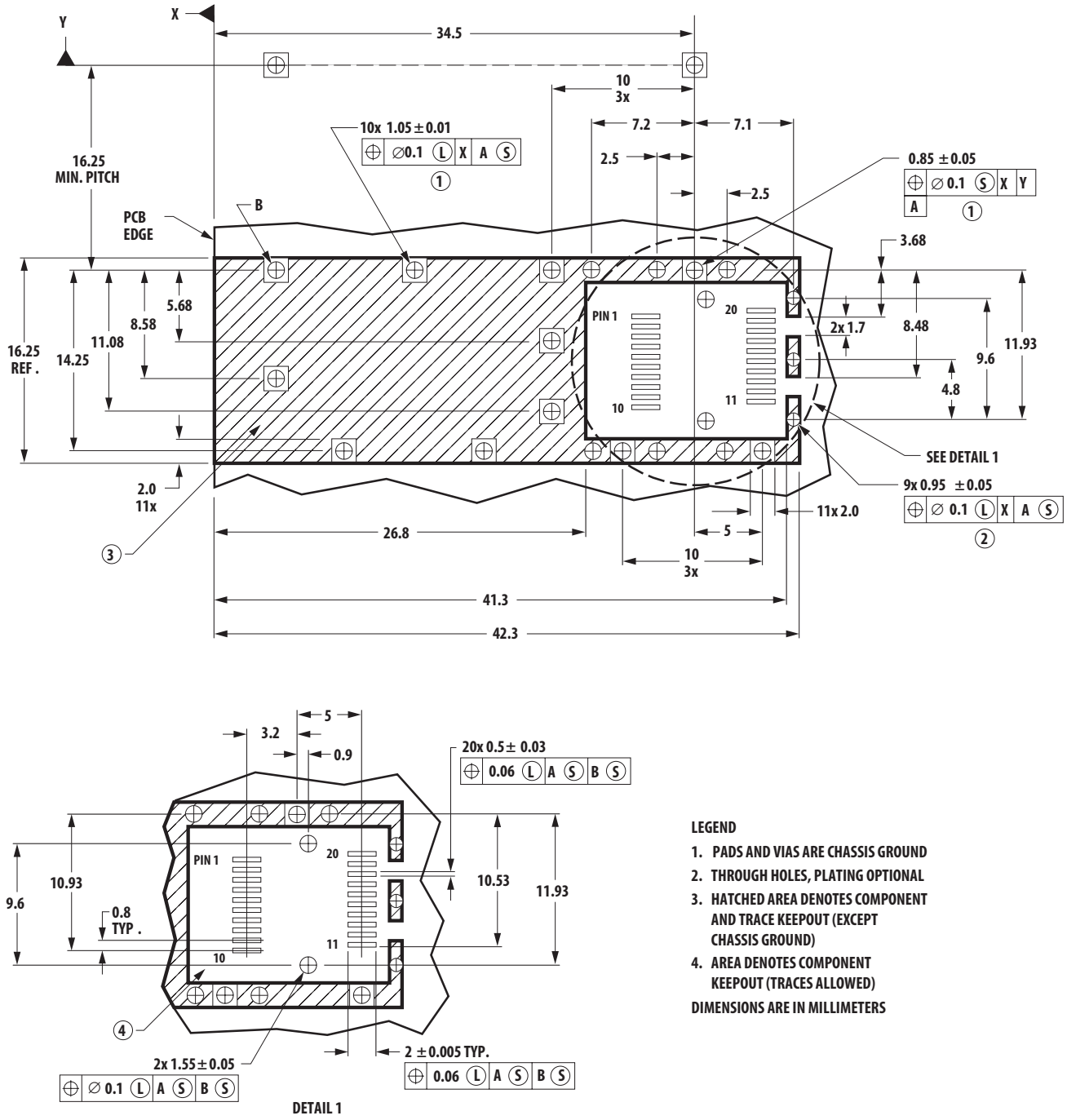


Figure 9. Module drawing

Figure 10. Module Label



LEGEND

1. PADS AND VIAS ARE CHASSIS GROUND
2. THROUGH HOLES, PLATING OPTIONAL
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND)
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED)

DIMENSIONS ARE IN MILLIMETERS

Figure 11. SFP host board mechanical layout

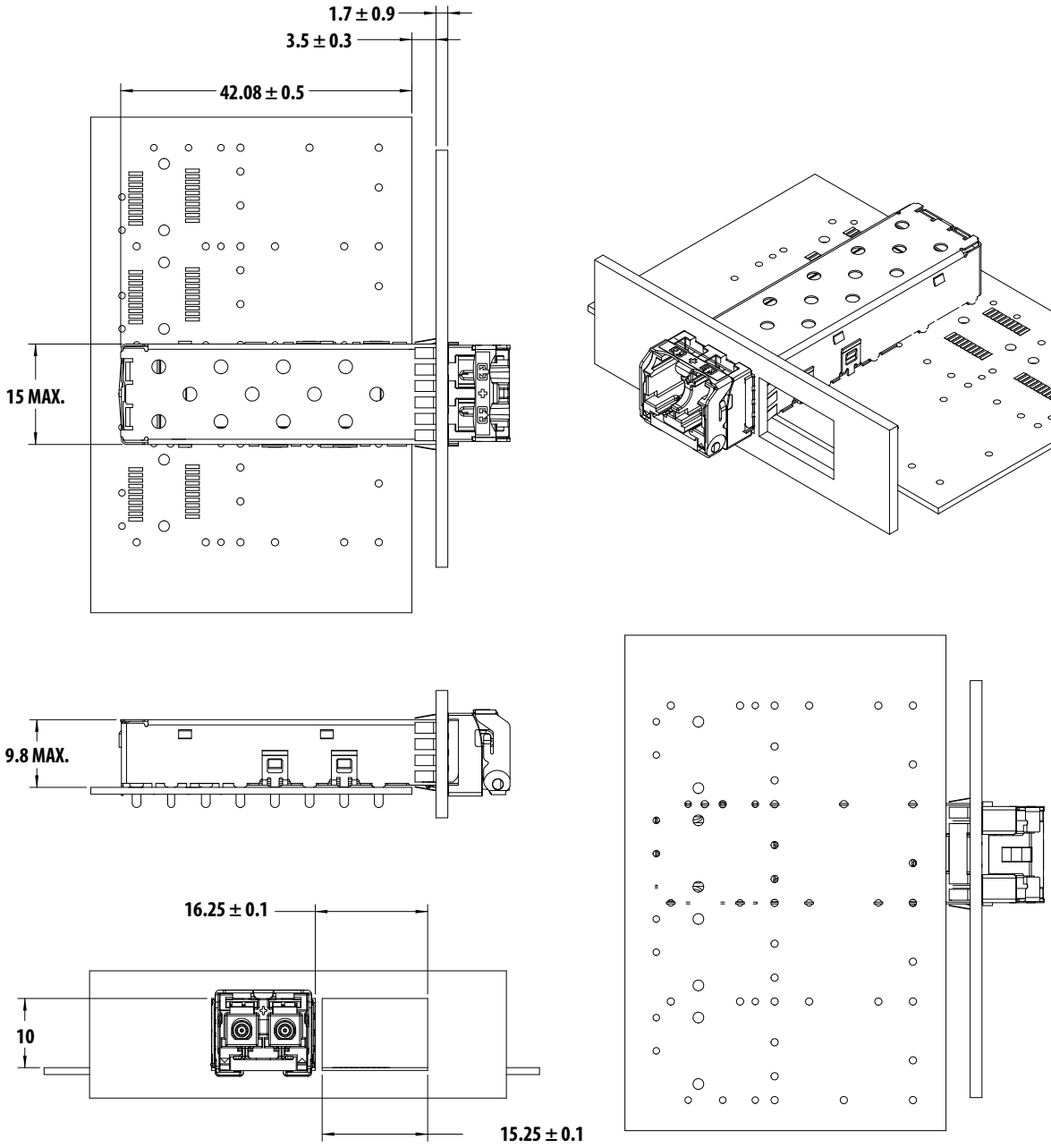


Figure 12. SFP Assembly drawing

Customer Manufacturing Processes

This module is pluggable and is not designed for aqueous wash, IR reflow, or wave soldering processes.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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