Rigid Disk Data Channel Qualifier

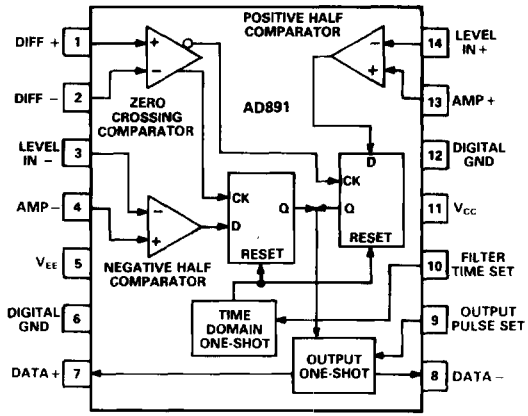
AD891

FEATURES

Three Matched, Offset-Trimmed Comparators
3.1 ns (typ) Comparator Propagation Delay
ECL Logic Permits 50 Mb/s Transfer Rates
6.8 ns Delay (typ) from Inputs to Data Output
500 ps (typ) Additional Pulse Pairing
Temperature-Compensated Operation
Compatible with 10 KH ECL Logic
Two Temperature-Compensated One-Shots
One-Shot Periods Set Using External Resistors

FUNCTIONAL BLOCK DIAGRAM

Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD891 disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891 provides both level and time-domain qualification. Level qualification is performed on alternating half cycles of the data waveform using a user-defined threshold level which is applied to each of two 3.1 ns propagation delay comparators. This technique prevents single bit errors from being propagated into two bit errors. A third comparator is used to provide zero-crossing detection. Factory trimmed offsets and a careful internal layout ensure symmetric operation and low pulse pairing with a differential input waveform.

An external RLC passive delay-line differentiator should be used with the AD891; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

The outputs from the amplitude-qualification comparators are applied to the "D" inputs of two master-slave D-type flip-flops which are then clocked by the outputs from the zero-crossing comparator. Each valid zero-crossing event causes a one-shot with a user-definable period to be triggered. This disables the operation of the flip-flops, thus preventing the detection of additional zero-crossing events during the one-shot period.

Simultaneously, an output one-shot is activated, the leading edge of which is synchronous with the change in the flip-flop outputs. The period of this one-shot is also user-definable and is intended to ensure adequate output pulse duration for transmission within the external environment. Each one-shot requires a single metal-film resistor to set its period. All one-shots have trimmed pulse periods; temperature stability is maintained by the use of an internal bandgap reference.

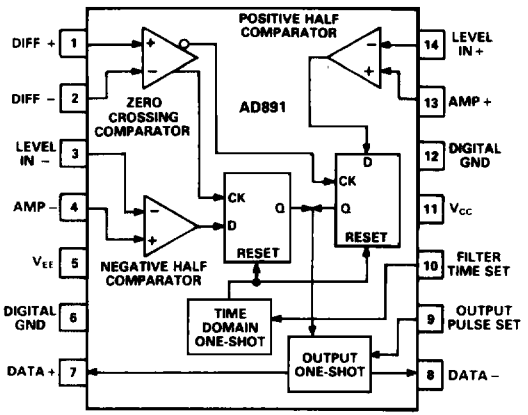
The AD891's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10 KH ECL logic levels. The AD891 can drive a properly terminated 75 Ω transmission line.

The AD891 is specified to operate over the commercial (0 to +70°C) temperature range. It is available either in a 14-pin cerdip package or in a 20-pin PLCC package.

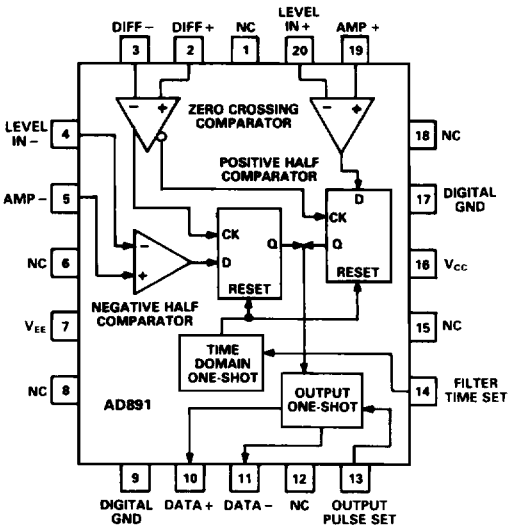
This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN CONFIGURATIONS

14-Pin Cerdip (Q) Package



20-Pin PLCC (P) Package



ORDERING GUIDE

Model No.	Package Description	Package Option*
AD891JQ	14-Pin Cerdip	Q-14
AD891JP	20-Pin PLCC	P-20A

*For outline information see Package Information section.