MPX2002

All-in-One Flyback Controller with Integrated Primary Control Circuitry and Secondary Synchronous Rectification Driver

DESCRIPTION

The MPX2002 is an all-in-one flyback controller with an integrated primary driving circuit, secondary controller, synchronous rectification driver, and safety-compliant feedback. It offers the benefits of both primary-side regulation (PSR) and secondary-side regulation (SSR).

A feedback circuit is not required, which reduces system complexity and the total BOM cost. The synchronous rectifier (SR) can match the driving signal of the primary-side MOSFET, meaning the SR can operate safely in continuous conduction mode (CCM). Meanwhile, the integrated SR controller regulates the SR MOSFET at a low threshold, which increases the overall efficiency and design flexibility. An internal linear regulator is integrated for the SR power supply, so the MPX2002 can drive the low-side SR MOSFET without auxiliary winding, even when the output is low.

The MPX2002 can run in CCM under heavy loads, then operate in quasi-resonant (QR) mode when the load decreases. If the load drops further, the MPX2002 works in pulse-frequency modulation (PFM) mode. The switching frequency (f_{SW}) is fixed at 20kHz when the device enters burst mode, which can prevent audible noise. The MPX2002 achieves high efficiency under most load conditions while improving electromagnetic interference (EMI) performance.

The MPX2002 features advanced protections, including V_{CC} over-voltage protection (OVP), primary over-current protection (POCP), secondary-sense output overload protection (OLP), internal brown-in/brownout (B/I, B/O), short-circuit protection (SCP), current-sense short protection (SSP), SR gate open/short protection (SGOP/SGSP), SRD abnormal protection (SRDP), FB OVP and under-voltage protection (UVP), internal thermal shutdown, under-voltage lockout (UVLO), and an externally triggered protection (Ext.P).

The MPX2002 is available in SOICW-16 and TSOICW16-15 packages.

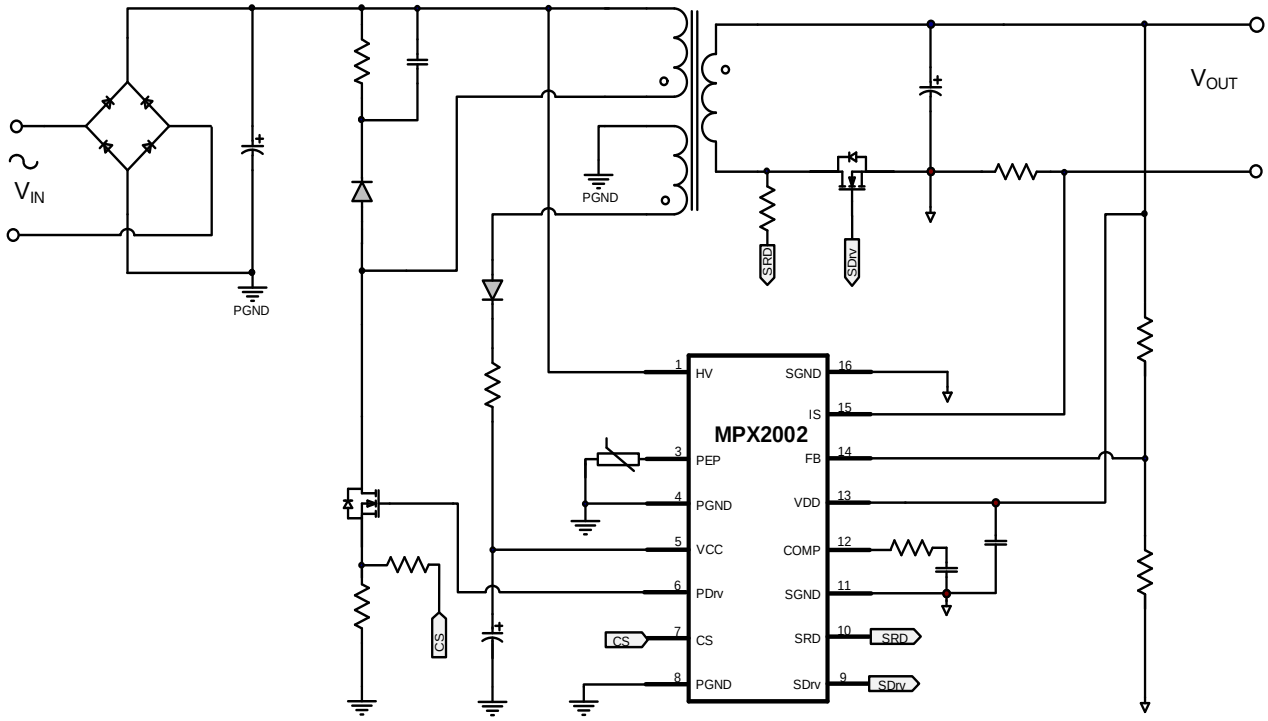
FEATURES

- Isolation Voltage >3750V_{AC}
- 100% Production HIPOT Compliance Testing
- UL1577 and IEC62368 Safety Approved, DIN VDE V 0884-17 in Progress
- Integrated Multi-Mode: Discontinuous Conduction Mode (DCM), Quasi-Resonant (QR) Mode, Continuous Conduction Mode (CCM)
- Flyback Controller, Secondary-Side Synchronous Rectifier (SR) Sensing/Driving Circuitry, and Safety-Compliant Feedback Link
- Integrated 650V Primary-Side Current Source and 150V Secondary-Side Current Source
- Less than 30mW in Standby Mode
- Improved SR Control for Reliable Operation and Higher Efficiency
- V_{CC} Over-Voltage Protection (OVP), Primary Over-Current Protection (POCP), Secondary-Sense Output Overload Protection (OLP), Internal Brown-In/Brownout (B/O, B/I), Short-Circuit Protection (SCP), Current-Sense Short Protection (SSP), SR Gate Open/Short Protection (SGOP/SGSP), SRD Abnormal Protection (SRDP), FB OVP and Under-Voltage Protection (UVP), Internal Thermal Shutdown, Under-Voltage Lockout (UVLO), and an Externally Triggered Protection (Ext.P)
- Available in TSOICW16-15 and SOICW-16 Packages

APPLICATIONS

- High-Performance USB PD Adapters
- Offline Battery Chargers
- High Efficiency, High-Current Power Supplies

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPX2002GYT	TSOICW16-15	*See Below*	3
MPX2002GY	SOICW-16		

* For Tape & Reel, add suffix -Z (e.g. MPX2002GYT-Z, MPX2002GY-Z).

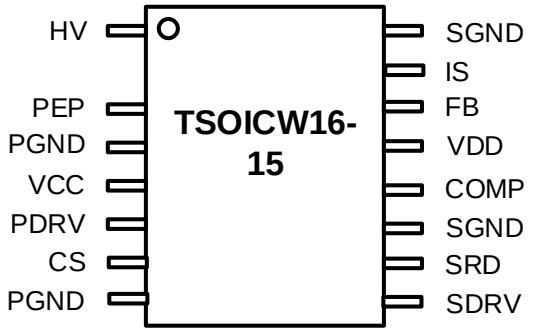
TOP MARKING

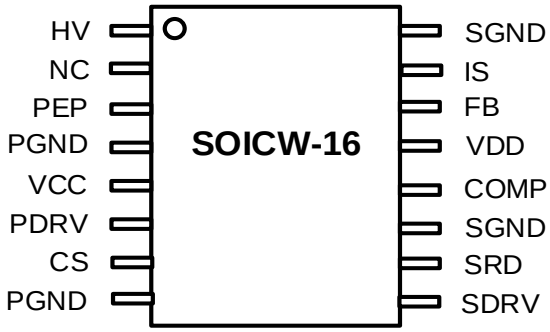
MPSYYWW
MPX2002
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MPX2002: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW





TSOICW16-15 (10.3mmx10mmx1.7mm)	SOICW16 (10.3mmx10mmx2.4mm)

PIN FUNCTIONS

Pin #		Name	Description
TSOICW16-15	SOICW-16		
1	1	HV	**High voltage.** The HV pin implements an internal, high-voltage current source for the primary IC's start-up sequence and normal operation. HV samples the input voltage for brown-in/brownout protection and provides line compensation on the primary peak current.
-	2	NC	**No connection.**
3	3	PEP	**External protection on the primary IC.** The PEP pin provides external protections. Protections include but are not limited to over-temperature protection (OTP) for the primary MOSFET and over-voltage protection (OVP) on the auxiliary winding. An internal current source allows for a direct connection between the external protection circuit and the PEP pin.
4	4	PGND	**Ground of the primary-side IC.**
5	5	VCC	**Power supply for the primary IC operation.** The VCC pin senses the output voltage (V_{OUT}) indirectly to provide over-voltage protection (OVP).
6	6	PDRV	**Output drive for the primary-side external power MOSFET.**
7	7	CS	**Primary MOSFET current sense for peak current mode regulation and SCP.** The CS pin implements over-power compensation based on the HV voltage.
8	8	PGND	**Ground of the primary-side IC.**
9	9	SDRV	**Output drive for the secondary-side external power MOSFET.**
10	10	SRD	**Voltage-sense drain of the synchronous rectifier MOSFET.** The voltage on the SRD pin controls the SR drive and QR operation. This pin can also supply power to VDD.
11	11	SGND	**Ground of the secondary side IC.**
12	12	COMP	**Internal error amplifier for output voltage regulation.** Connect the compensation network to the COMP pin to adjust the regulating performance. COMP can be configured as an external compensation network. The COMP voltage can be monitored for secondary overload protection (SOLP).
13	13	VDD	**Power supply for the secondary IC operation.**
14	14	FB	**Feedback for constant voltage regulation.** Connect FB to a resistor divider to sense the output voltage. The FB can be reused to achieve output OVP and OLP.
15	15	IS	**Output current sense.** IS senses the output current (I_{OUT}) when a current-sense resistor is connected to the output loop. This also provides accurate overload protection (OLP). In addition, the IS voltage can be used for cable drop compensation.
16	16	SGND	**Ground of the secondary side IC.**

ABSOLUTE MAXIMUM RATINGS (1)

HV to PGND ..... -0.3V to +650V
SRD to SGND..... -1V to +150V
VCC to PGND..... -0.3V to +35V
PDRV to PGND ..... -0.3V to +16V
SDRV to SGND ..... -0.3V to +16V
VDD to SGND..... -0.3V to +35V
CS, PEP to PGND ..... -0.3V to +6.5V
COMP, FB, IS to SGND..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
TSOICW16-15 .....2.7W
SOICW16 .....2.8W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -60°C to +150°C

Recommended Operating Conditions (3)

Operating junction temp (T_J) .... -40°C to +125°C
VCC to PGND..... 9.5V to 24V
VDD to SGND..... 4.8V to 30V

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOICW16-15	45	18	°C/W
SOICW-16	44	24	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical values tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Insulation						
Isolation voltage	V_{ISO}	50Hz/60Hz	3.75			kV_{RMS}
Primary Side (HV)						
Breakdown voltage	V_{HV-BD}	T_J = 25°C	650			V
Leakage current from HV	I_{HV-LK}	V_{HV} = 500V_{DC}		7	11	µA
Supply current from HV	I_{HV-SP1}	V_{CC} = 12V, V_{HV} = 80V, T_J = 25°C	4.5	5.5	6.5	mA
		V_{CC} = 12V, V_{HV} = 80V, T_J = 105°C	3.1	3.8	4.6	
	I_{HV-SP2}	V_{CC} = 1.5V, V_{HV} = 80V, T_J = 25°C		3.7		
		V_{CC} = 1.5V, V_{HV} = 80V, T_J = 105°C		3.1		
Brown-in threshold voltage	V_{HV-ON}		95	107	120	V
Brown-out threshold voltage	V_{HV-OFF}		85	98	110	V
Brown-in/out hysteresis	$V_{HV-\Delta}$			8.5		V
Delay time for brown-out	t_{BO}		45	55	67	ms
Primary Side (VCC)						
I_{HV-SP} turn-off voltage	$V_{CC-IOFF}$		13	14.5	16	V
Minimum operation voltage	V_{CC-MIN}		7.3	8.3	9.3	V
$V_{CC-IOFF}$ - V_{CC-MIN}	V_{CC-STW}		5.2	6.2	7.2	V
Auto-recovery protection level	V_{CC-AUT}		4.9	5.5	6.1	V
Over-voltage protection level	V_{CC-OVP}		24	26	28	V
V_{CC} OVP delay time	$t_{VCC-OVP}$			32		µs
Operating current	I_{OP}	V_{CC} = 15V, f_{SW} = 80kHz, C_L = 1nF			3	mA
Operating current during a protection	I_{OP-PRO}	V_{CC} = 10V, except B/O			120	µA
		V_{CC} = 10V, B/O	1			mA
Quiescent current	I_Q	V_{CC} = 12V			500	µA
Primary Side (PDRV)						
Driver voltage high level	V_{HIGH}	C_L = 1nF, V_{CC} = V_{CC-MIN} + 0.1V	5.8			V
		C_L = 1nF, V_{CC} = 12V	9.6			V
Driver voltage clamp level	V_{CLAMP}	C_L = 1nF, V_{CC} = 24V	11.5	14.5	16	V
Driver voltage low level	V_{LOW}	C_L = 1nF			100	mV
Driver voltage rising time	t_{RISE}	C_L = 1nF		20		ns
Driver voltage falling time	t_{FALL}	C_L = 1nF		18		ns

ELECTRICAL CHARACTERISTICS *(continued)*

Typical value tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Maximum switching frequency	f_{SW-MAX}			85		kHz
Maximum on time	t_{ON-MAX}			10		µs
Minimum off time	$t_{OFF-MIN}$			760		ns
Time to trigger primary OCP	t_{OCP}		45	55	68	ms
Minimal switching frequency during soft start	$f_{SW-SOFT}$			24		kHz
Primary Side (CS)						
Soft-start duration	t_{SOFT}			9.6		ms
Threshold for SCP	V_{SCP}		0.595	0.635	0.675	V
Second SCP blanking time	t_{SCP2}			90		µs
Maximum peak current limitation	$V_{IPK-MAX}$		0.384	0.4	0.416	V
Minimum peak current limitation	$V_{IPK-MIN}$			0.1		V
Jittering amplitude	ΔV_{IPK}	$V_{IPK} = V_{IPK-MAX}$		±2.9%		$V_{IPK-MAX}$
Jittering period (5)				256		cycles
f_{SW} at which I_{PK} foldback begins	f_{SW-H}			40		kHz
Slope of the compensation ramp	S_{RAMP}			20		mV/µs
LEB for current limitation	t_{LEB-L}			400		ns
LEB for SCP	t_{LEB-S}			250		ns
ΔI_{HVCS} / ΔV_{HV} Ratio	K_{HVCS}			0.53		µA/V
CS sourcing current	I_{HVCS}	V_{HV} = 200V, $V_{IPK} = V_{IPK-MAX}$, T_J = 25°C		36		µA
		V_{HV} = 375V, $V_{IPK} = V_{IPK-MAX}$, T_J = 25°C	100	126	152	
V_{IPK} (below which line compensation completely removed) (5)	V_{LC-END}		0.15			V
Detection time for CS short	t_{SSP}		4	5.8	7.5	µs
Threshold for CS short	V_{CSS}	During the soft-start period		50		mV
Primary Side (PEP)						
Sourcing current from PEP	I_{PEP}	V_{PEP} = 0.5V		110		µA
Protection trigger threshold	V_{PEP-T}		0.425	0.5	0.575	V
Protection trigger delay	t_{PEP-T}			300		µs

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Primary Side – Internal Thermal Protection						
OTP threshold (5)	T_{OTP-P}			150		°C
Hysteresis to recover from OTP (5)	$T_{\Delta-P}$			40		°C
Secondary Side (VDD)						
Operating current	I_{OPS}	V_{DD} = 5V, f_{SW} = 80kHz, C_L = 4.7nF			4.5	mA
		V_{DD} = 12V, f_{SW} = 80kHz, C_L = 4.7nF			6.5	
Quiescent current	I_{QS}	V_{DD} = 5V			370	µA
UVLO falling threshold	V_{DD-OFF}		4.0	4.25	4.5	V
UVLO rising threshold	V_{DD-ON}		4.3	4.5	4.7	V
UVLO hysteresis	$V_{DD-\Delta}$			0.3		V
Bleeding current during protection	I_{BLD}			10		mA
VDD ready threshold	V_{DD-RDY}		4.72	4.92	5.12	V
VDD clamp level when charged by SRD	V_{DD-C}		4.3	4.5	4.7	V
Secondary Side (FB)						
Feedback reference voltage	V_{REF}	T_J = 25°C	1.21	1.22	1.23	V
Feedback current	I_{FB}	V_{FB} = 1.22V, T_J = 25°C			50	nA
FBOLP threshold	V_{FBO}	V_{DD} > V_{DD-RDY}	0.075	0.095	0.115	V
FBOLP delay time	t_{FBO}			200		µs
OVP threshold	V_{OVP}		113%	118%	123%	V_{REF}
OVP delay time	t_{OVP-D}			115		µs
Secondary Side (SRD)						
Turn-on threshold	V_{SR-ON}		-50	-37	-24	mV
Regulated forward voltage	V_{FWD}		8	20	32	mV
Turn-off threshold	V_{SR-OFF}		8	18	28	mV
Turn-off threshold in t_{ON-MIN}	$V_{SR-OFFM}$			1.6		V
Input current at SRD pin	I_{SRD-L}	V_{SRD} = 30V			15	µA
Maximum charging current to V_{DD}	I_{SRD-C}	V_{SRD} = 30V, V_{DD} = 0V		50		mA
		V_{SRD} = 30V, V_{DD} = V_{DD-ON} - 0.5V		75		
Threshold for driver open detection	V_{SGO}	T_J = 25°C	-0.52	-0.47	-0.42	V
Minimal time for driver open detection	t_{SGO}	DCM		0.9		µs
Secondary Side (SDRV)						
Blanking for turn-on detection	t_{SR-ONB}		270	400	570	ns
Turn-on delay	t_{SR-OND}	C_L = 4.7nF		150		ns

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values tested at T_J = -40°C to 125°C, unless otherwise noted.

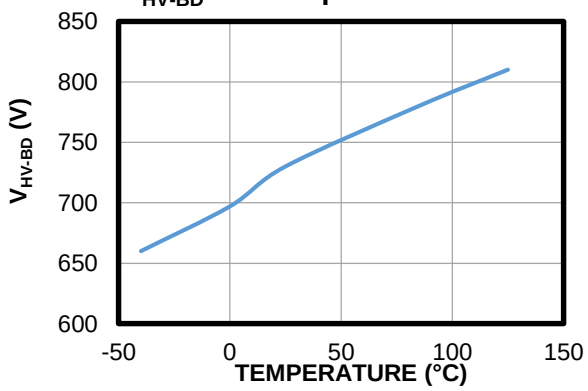
Parameter	Symbol	Condition	Min	Typ	Max	Units
Turn-off delay	$t_{SR-OFFD}$	C_L = 4.7nF		35	62	ns
Minimal on time	t_{ON-MIN}		0.8	1.05	1.35	µs
Driver voltage low level	V_{DRV-L}	V_{DD} = V_{DD-OFF} + 0.1V			0.1	V
		V_{DD} = 5V			0.1	
Driver voltage high level	V_{DRV-H}	V_{DD} = V_{DD-OFF} + 0.1V	4.1	4.3	4.6	V
		V_{DD} = 5V		5		
		V_{DD} = 12V	9		10	
		V_{DD} = 24V	9		10	
Max sourcing current (5)	I_{SON}	V_{DD} = 12V		0.5		A
Max sinking current (5)	I_{SOFF}	V_{DD} = 12V		3		A
Driver pull-down resistance	$R_{PULL-DOWN}$	C_L = 4.7nF, V_{DD} = 12V		0.65	1.05	Ω
Dead time under CCM condition	t_{DT}			30		ns
Secondary Side (IS)						
Overload protection threshold	V_{OLP}		37	42	47	mV
Overload protection delay	t_{OLP}		55	66	77	ms
CDC voltage on FB	V_{CDC_MAX}	V_{IS} = 40mV		50		mV
Secondary Side (COMP)						
Transconductance	GM			430		µA/V
Maximum sink current	I_{SINK}		56	86	120	mA
Maximum source current	I_{SOURCE}		-125	-88	-60	mA
Maximum COMP voltage(5)	V_{COMP-S}	V_{DD} = 5V	2.25	2.38	2.51	V
Threshold for the max frequency limitation	V_{FS-MAX}		2.12	2.2	2.3	V
Threshold for burst entry	V_{BURST}		0.3	0.33	0.36	V
Burst exit hysteresis	$V_{BURST-HYS}$			0.018		V
Maximum PFM frequency	f_{S-MAX}	T_J = 25°C	82	85	89	kHz
Minimal PFM (burst entry) frequency	f_{S-MIN}	T_J = 25°C	18	20		kHz
Burst exit frequency	f_{S-MIN}	T_J = 25°C	18	20		kHz
Secondary Side – Internal Thermal Protection						
OTP threshold (5)	T_{OTP-S}			150		°C
Hysteresis to recover from OTP (5)	$T_{Δ-S}$			40		°C

Note:

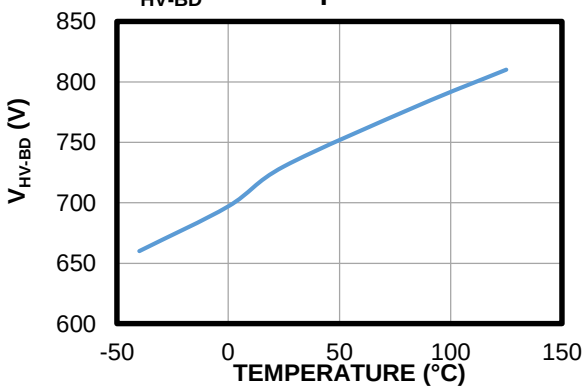
5) These parameters are guaranteed by design.

TYPICAL CHARACTERISTICS

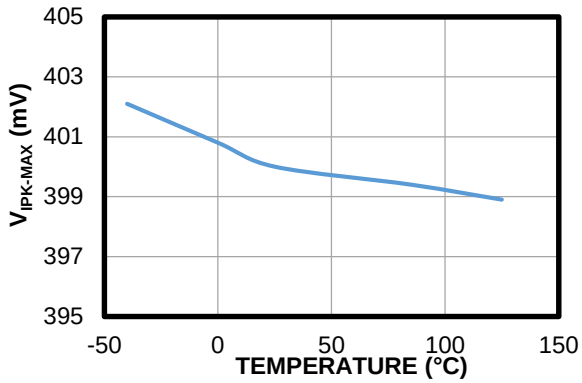
V_{HV-BD} vs. Temperature



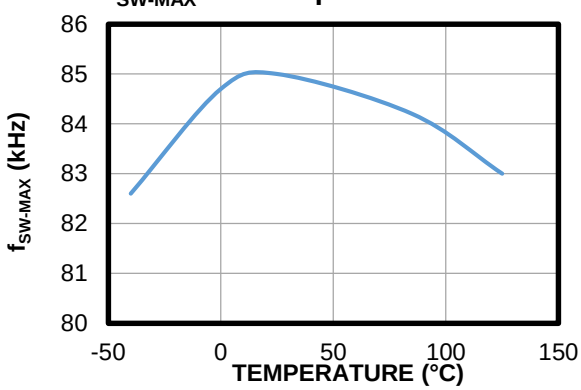
V_{HV-BD} vs. Temperature



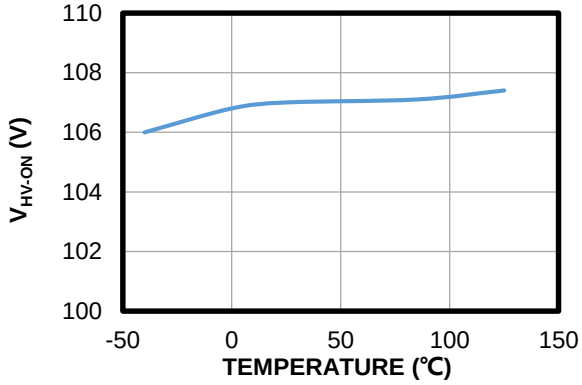
$V_{IPK-MAX}$ vs. Temperature



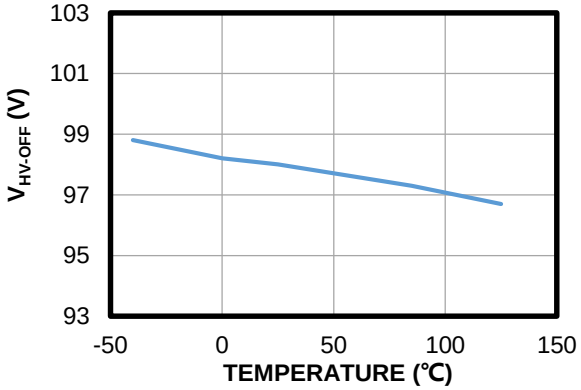
f_{SW-MAX} vs. Temperature



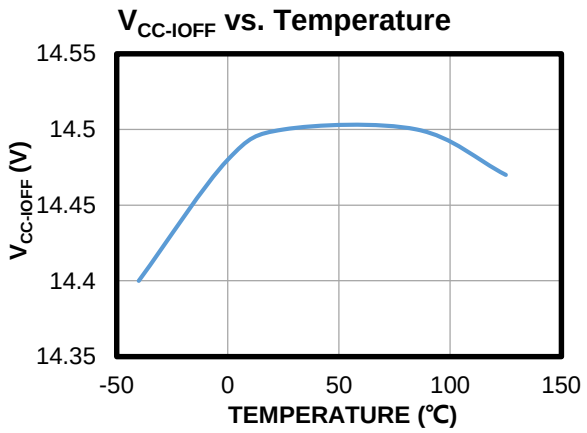
V_{HV-ON} vs. Temperature

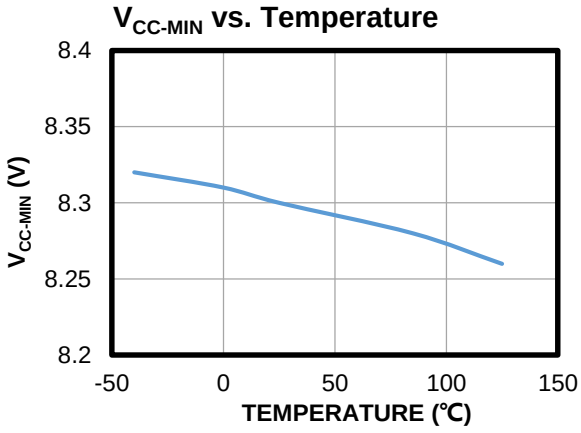


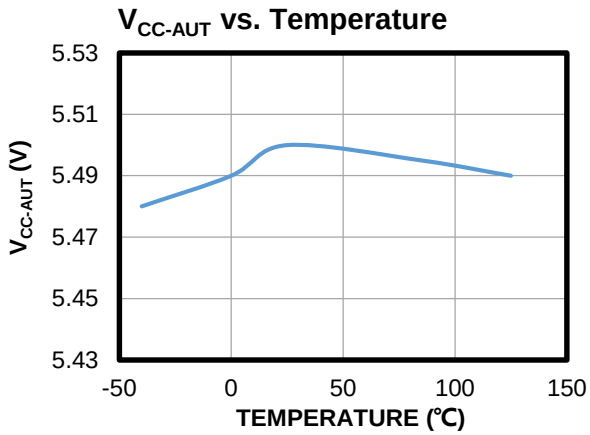
V_{HV-OFF} vs. Temperature

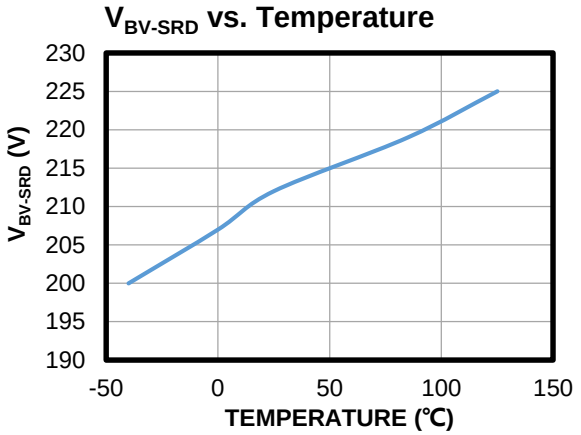


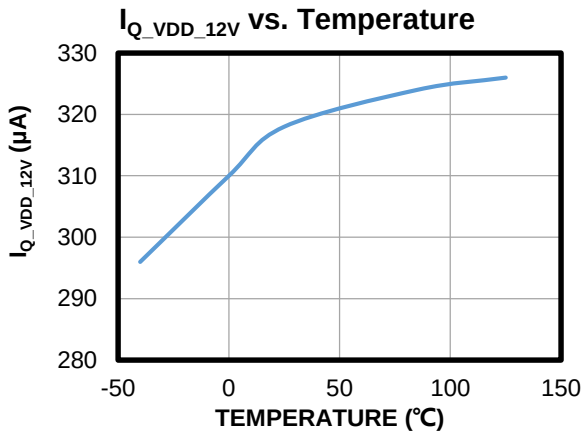
TYPICAL CHARACTERISTICS *(continued)*

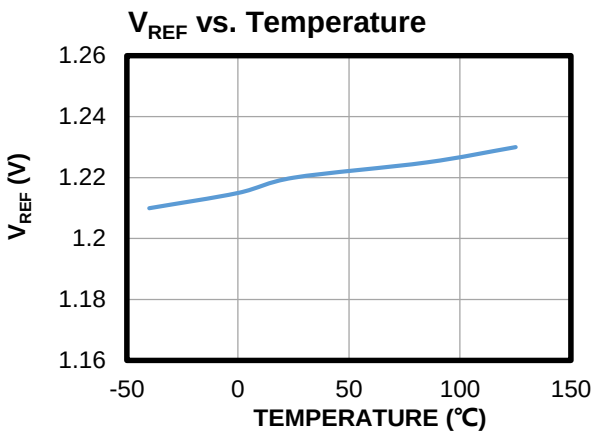




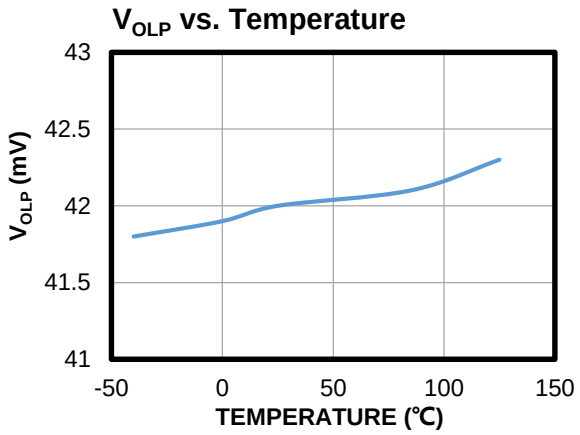


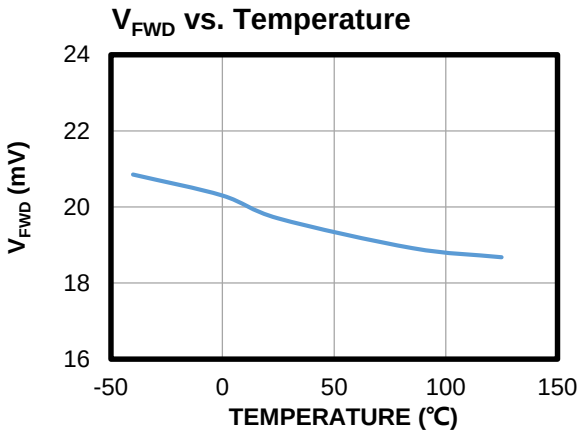






TYPICAL CHARACTERISTICS *(continued)*



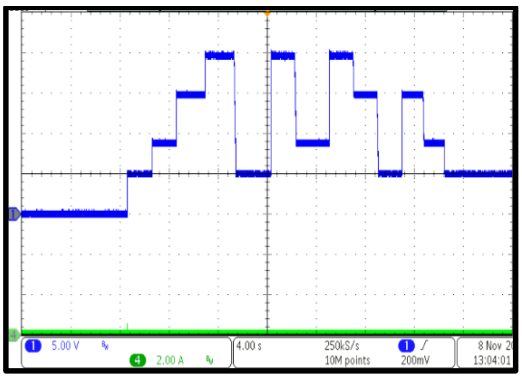


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, 15V, or 20V, I_{OUT} = 0A to 3.25A, unless otherwise noted.

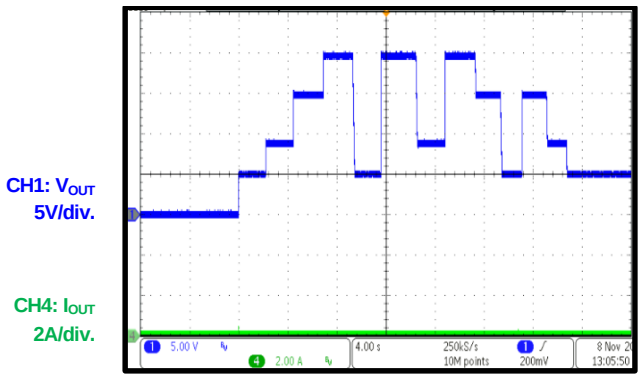
Output Voltage Transient Response

V_{IN} = 115V_{AC}, I_{OUT} = 0A



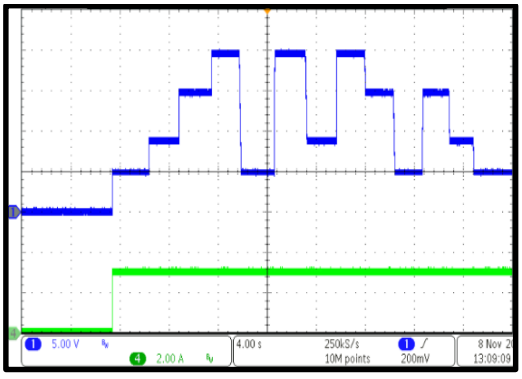
Output Voltage Transient Response

V_{IN} = 230V_{AC}, I_{OUT} = 0A



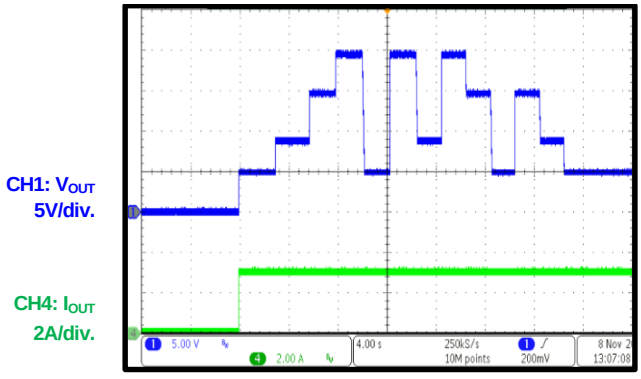
Output Voltage Transient Response

V_{IN} = 115V_{AC}, I_{OUT} = 3A



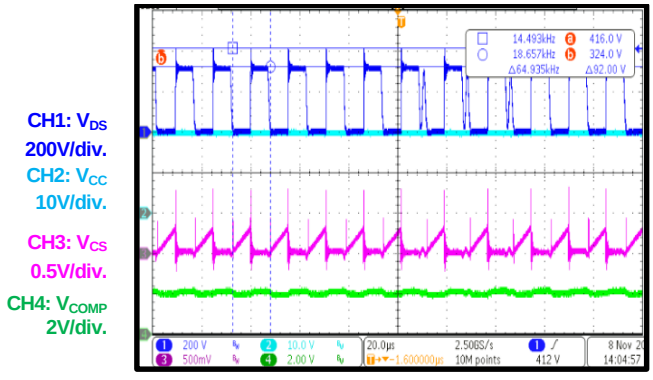
Output Voltage Transient Response

V_{IN} = 230V_{AC}, I_{OUT} = 3A



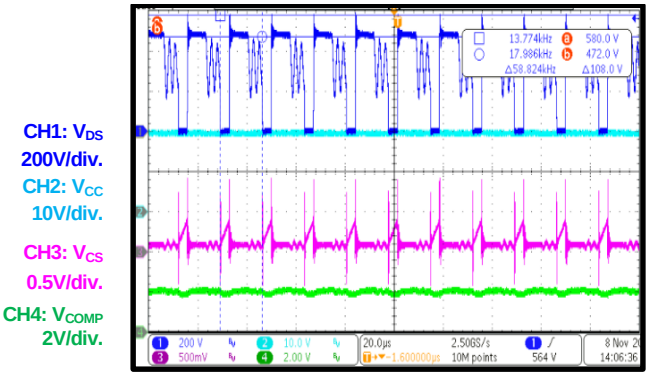
Steady State

V_{IN} = 115V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A



Steady State

V_{IN} = 230V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A



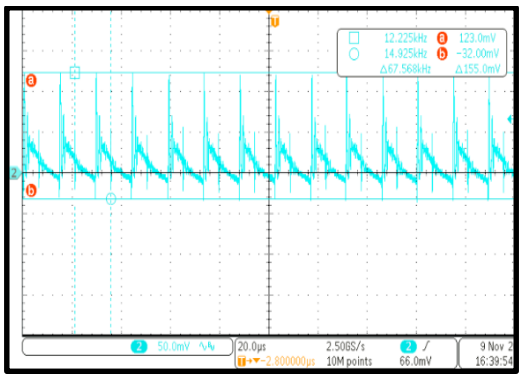
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, 15V, or 20V, I_{OUT} = 0A to 3.25A, unless otherwise noted.

Output Voltage Ripple

V_{IN} = 115V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A

CH2: V_{OUT_AC} 50mV/div.

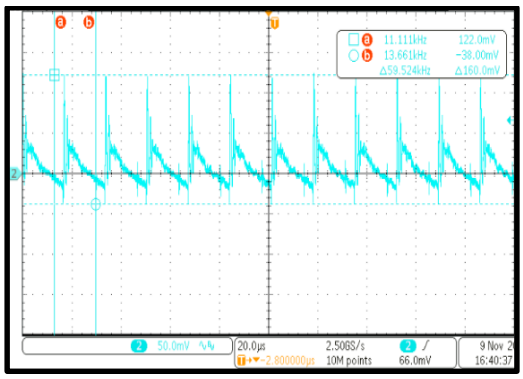


20µs/div.

Output Voltage Ripple

V_{IN} = 230V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A

CH2: V_{OUT_AC} 50mV/div.

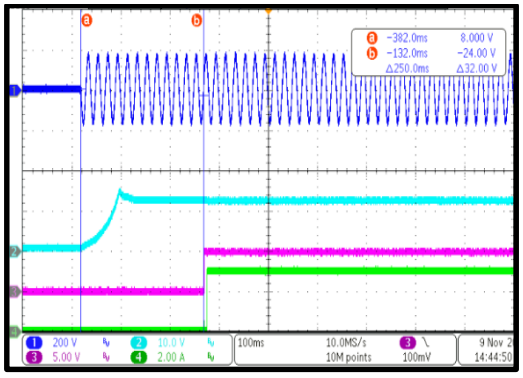


20µs/div.

Start-Up

V_{IN} = 115V_{AC}, V_{OUT} = 5V, I_{OUT} = 3A

CH1: V_{IN} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 5V/div.
CH4: I_{OUT} 2A/div.

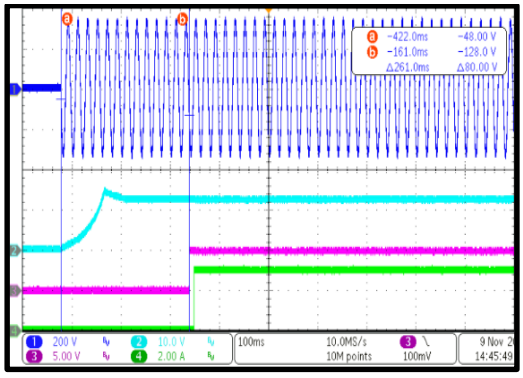


100ms/div.

Start-Up

V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 3A

CH1: V_{IN} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 5V/div.
CH4: I_{OUT} 2A/div.

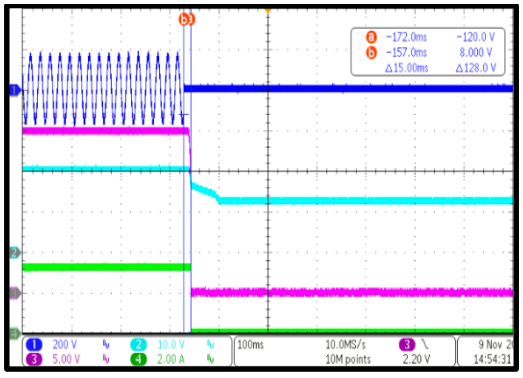


100ms/div.

Shutdown

V_{IN} = 115V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A

CH1: V_{IN} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 5V/div.
CH4: I_{OUT} 2A/div.

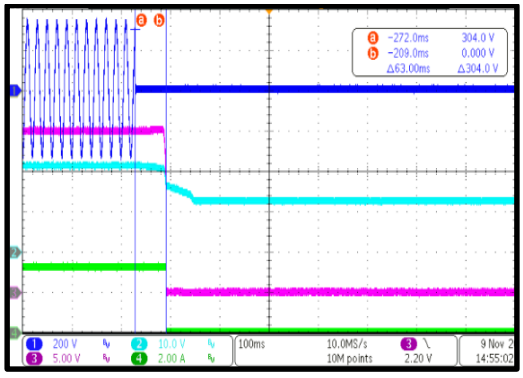


100ms/div.

Shutdown

V_{IN} = 230V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A

CH1: V_{IN} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 5V/div.
CH4: I_{OUT} 2A/div.



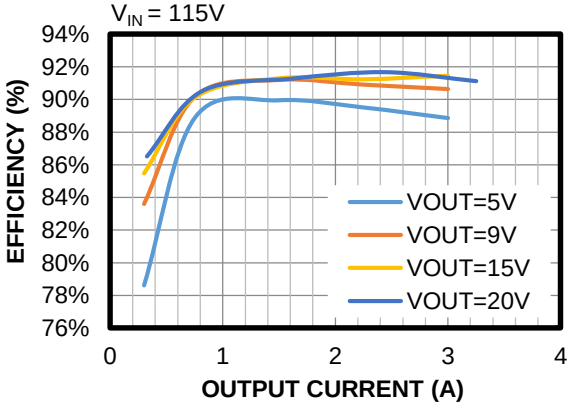
100ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, 15V, or 20V, I_{OUT} = 0A to 3.25A, tested with a 10cm cable.

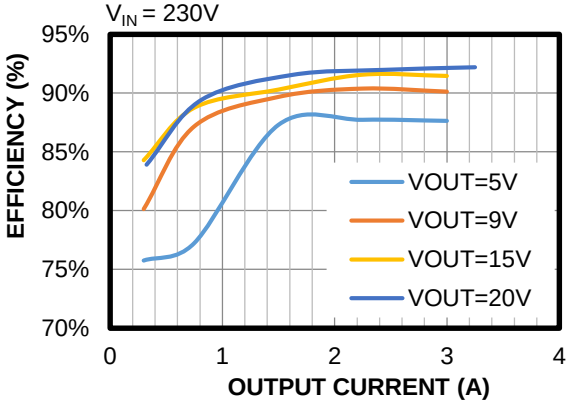
Efficiency vs. Load Current

V_{IN} = 115V

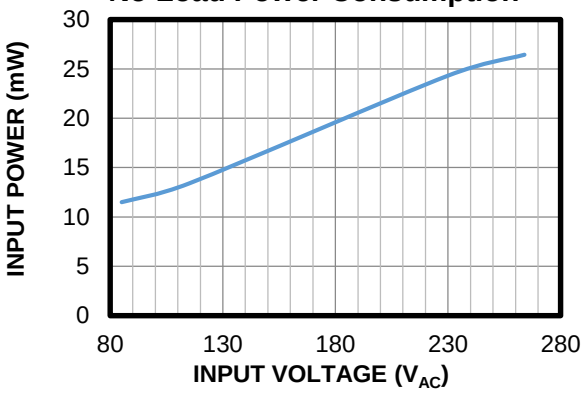


Efficiency vs. Load Current

V_{IN} = 230V

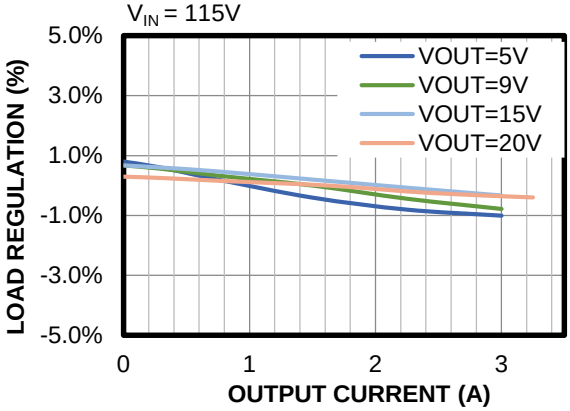


No Load Power Consumption



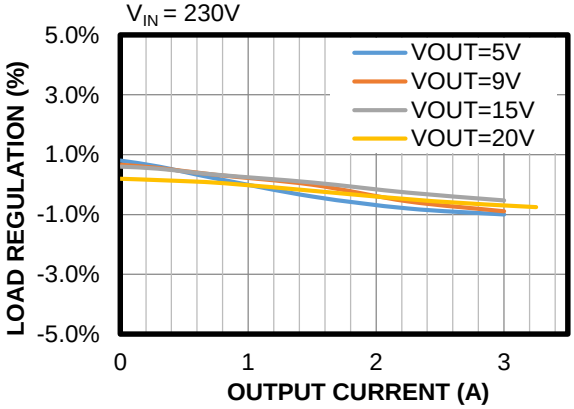
Load Regulation

V_{IN} = 115V



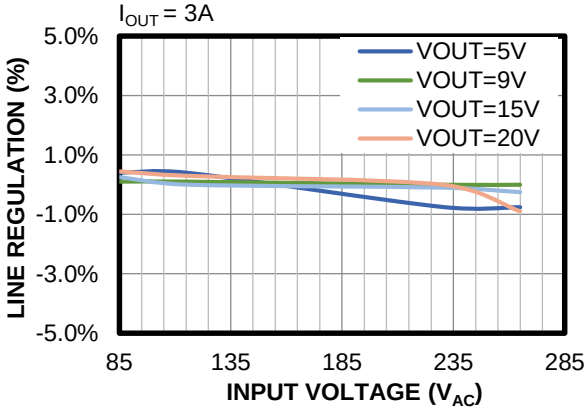
Load Regulation

V_{IN} = 230V



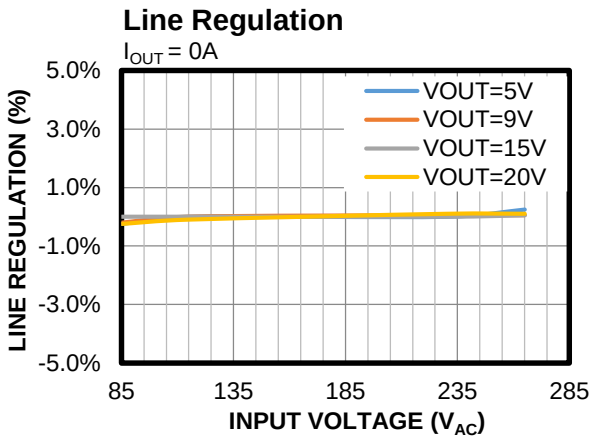
Line Regulation

I_{OUT} = 3A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, 15V, or 20V, I_{OUT} = 0A to 3.25A, test with a 10cm cable.

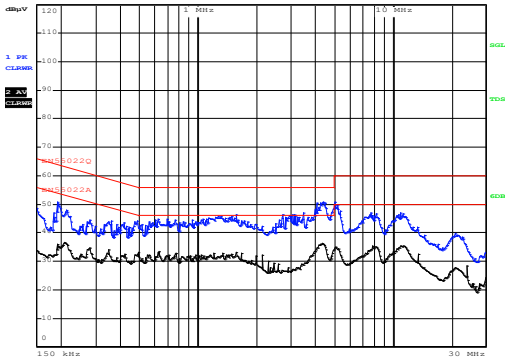


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 115V_{AC}/230V_{AC}, V_{OUT} = 5V, 9V, 15V, or 20V, I_{OUT} = 0A to 3.25A, unless otherwise noted.

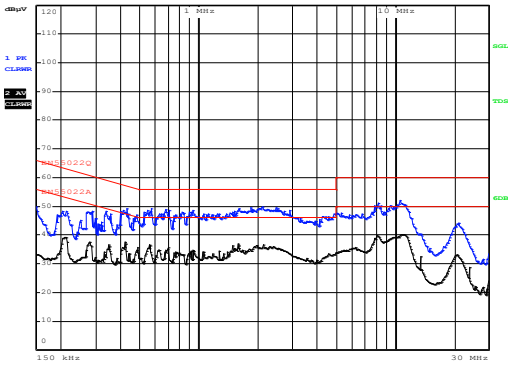
EMI

V_{IN} = 115V_{AC}, L line, V_{OUT} = 20V, I_{OUT} = 3.25A



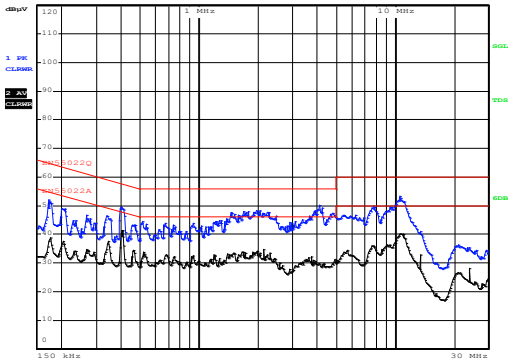
EMI

V_{IN} = 115V_{AC}, N line, V_{OUT} = 20V, I_{OUT} = 3.25A



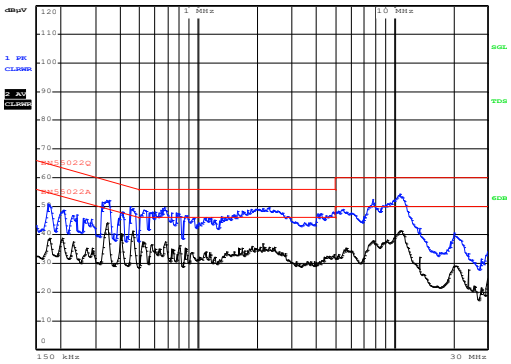
EMI

V_{IN} = 230V_{AC}, L line, V_{OUT} = 20V, I_{OUT} = 3.25A



EMI

V_{IN} = 230V_{AC}, N line, V_{OUT} = 20V, I_{OUT} = 3.25A



FUNCTIONAL BLOCK DIAGRAM

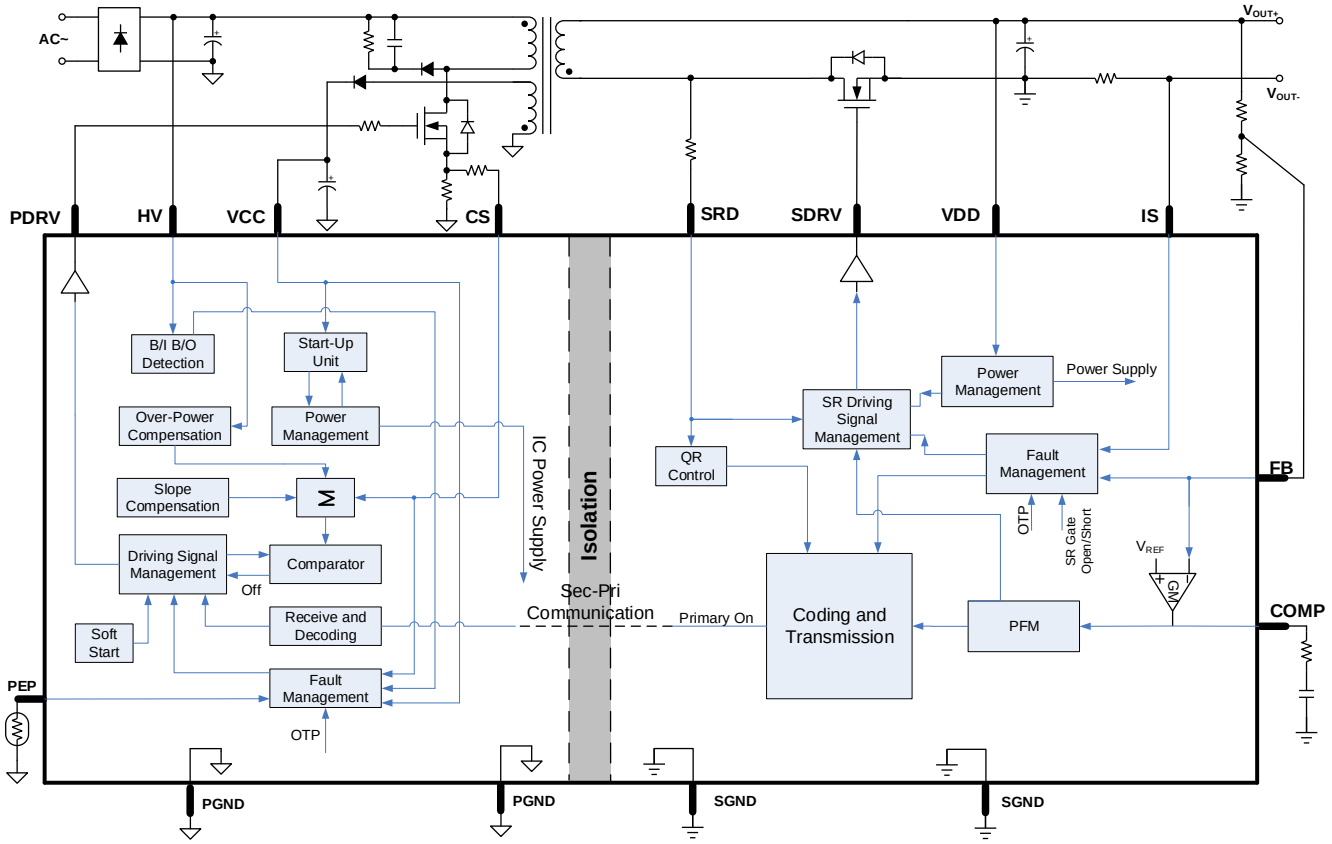


Figure 1: Functional Block Diagram

OPERATION

The MPX2002 is an all-in-one flyback controller that provides the benefits of primary-side regulation (PSR) and secondary-side regulation (SSR). The MPX2002 achieves accurate regulation while reducing system complexity and the total solution cost.

The MPX2002 implements a complete SSR scheme. Both the control loop and the modulation block are placed on the secondary IC, so the driving signal of the synchronous rectifier (SR) can match the driving signal of the primary-side MOSFET. This allows the SR to operate safely in continuous conduction mode (CCM), which increases overall efficiency and provides the robust design more flexibility.

PRIMARY IC FUNCTIONS

Start-Up with Brown-In/Brownout Detection

The IC is disabled when there is no power supply. When a voltage is applied to the HV pin, VCC is charged by an internal current source from HV. Once V_{CC} exceeds the HV current source turn-off voltage ($V_{CC-IOFF}$, typically 14.5V), the current source stops charging.

To eliminate voltage drop influence on the external resistor, brown-in/brownout protection is enabled after the HV current source turns off. If the HV voltage exceeds V_{HV-ON} (typically 107V), a brown-in condition has occurred. The primary IC turns on the HV current source to charge V_{CC} back to $V_{CC-IOFF}$ (to guarantee a maximized start-up window) and operates in normal start-up mode. Otherwise, it is treated as a brownout condition. The primary IC's operation remains disabled. Meanwhile, V_{CC} is charged and discharged between $V_{CC-IOFF}$ and V_{CC-MIN}.

Once V_{CC} exceeds $V_{CC-IOFF}$, the primary IC begins monitoring the status of the secondary IC before the primary IC runs into normal start-up mode. There are three conditions for primary IC start-up, described below.

1. If the primary IC starts up normally when a brown-in condition is detected, and the primary IC does not detect any status from the secondary IC, the primary IC starts switching on its own. Once the secondary IC is active, the primary IC stops switching independently, and the secondary IC takes control.

   There is a time limit on the primary IC's start-up period. Independent primary switching stops when the timer (t_{OCP}) runs out. This means that if there is a fault condition (e.g. an overload), the secondary IC may not start up successfully. t_{OCP} starts counting from soft start. Then the primary over-current protection (POCP) flag is set, and the primary IC runs in a protection operation.

2. If the secondary IC is active before primary-side switching begins, the primary IC does not require independent switching. The secondary IC takes control directly after the brown-in condition is detected.

3. If the protection status is detected before start-up, the IC indicates a fault condition, such as an overload on the secondary side. In this scenario, the primary IC does not switch at all, but sets the protection flag and runs in a protection operation.

Figure 2 shows the start-up logic for the primary IC.

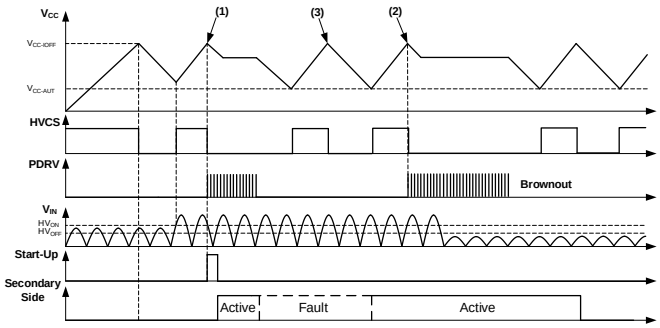


Figure 2: Start-Up Logic for the Primary IC

Brownout Protection during Normal Operation

To prevent power supply issues caused by an insufficient input voltage, the primary IC implements brownout protection. If the HV voltage is below V_{HV-OFF} (typically 98V, which is the internal B/O threshold), the brownout timer starts running. If the HV voltage exceeds V_{HV-OFF}, the timer is reset. If the brownout timer reaches t_{BO}, the primary IC triggers brownout protection, and VCC initiates hiccup operation while it is between V_{CC-MIN} (typically 8.3V) and $V_{CC-IOFF}$.

The primary IC does not start up again until there is a valid brown-in detection condition. Brown-in and brownout detection are suspended when the HV current source turns on (to avoid the effect of the HV voltage drop). These protections can be detected after the HV current source turns off.

Soft Start (SS)

To reduce stress on the power circuits, a soft-start function is implemented for the primary IC. When the primary IC enters normal start-up mode and starts switching on its own, the internal soft start gradually increases the current limitation from $V_{IPK-MIN}$ (typically 0.1V) to $V_{IPK-MAX}$ (typically 0.4V). During this time, the switching frequency (f_{SW}) rises from $f_{SW-SOFT}$ (typically 24kHz) to f_{SW-MAX} (typically 85kHz). The soft-start period lasts for t_{SOFT} (typically 9.6ms).

Peak Current Control with Internal Slope Compensation

The primary IC employs peak current mode control with a switching on time. This on time is controlled by comparing the voltage across the CS current-sense resistor with the internal reference voltage. The reference voltage is regulated by f_{SW} with a maximum value of $V_{IPK-MAX}$ and a minimum value of $V_{IPK-MIN}$.

The reference voltage is clamped at $V_{IPK-MAX}$ when f_{SW} exceeds f_{SW-H} (typically 40kHz); the reference voltage clamped at $V_{IPK-MIN}$ when f_{SW} is below f_{S-L} (typically 20kHz) (see Figure 3). When f_{SW} is between f_{SW-H} and f_{SW-L}, the reference voltage is adjusted continuously.

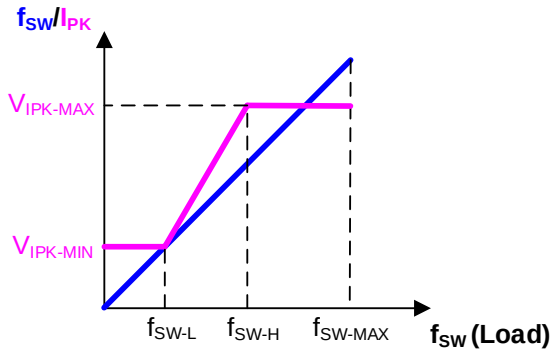


Figure 3: Peak Current Reference vs. Switching Frequency

A synchronized positive slope is added to the current-sense signal on CS to prevent sub-harmonic oscillations and guarantee stable peak current mode control across a wide range of input voltages.

Due to parasitic capacitance, a spike usually occurs on the current-sense resistor after the MOSFET turns on. To prevent the peak current limitation comparator from being falsely triggered by this turn-on spike, a leading edge blanking (LEB) function is implemented on the comparator. During the blanking time, the peak current limitation comparator is disabled, so the MOSFET cannot turn off. Two-level LEB is adopted in the comparator. Normal operation has t_{LEB-L} (typically 400ns), while t_{LEB-S} (typically 250ns) is the blanking time during SCP.

Line Compensation for Peak Current Control

Ideally, the primary peak current should be exactly the same as the reference because of peak current control operation. However, the IC has a logic propagation delay and driver delay, so the actual peak current always exceeds the reference value. The difference between the actual value and reference value varies with the input voltage. A higher input voltage results in a higher peak current overshoot (see Figure 4). This leads to a significant variation in the maximum power limitation.

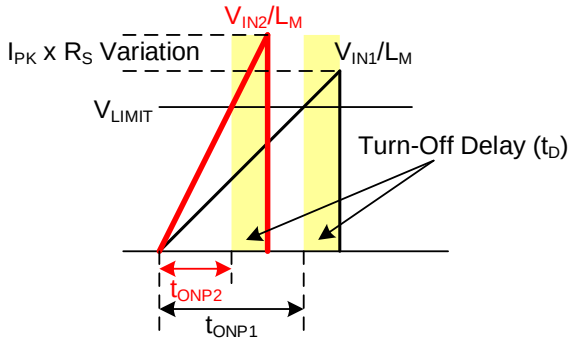


Figure 4: Peak Current Difference Caused by Turn-Off Delay

The slope compensation voltage is proportional to the primary MOSFET's turn-on time, which is determined by the load and input voltage. This means that the slope compensation value is lower when the input voltage is higher, even if the load is the same.

To compensate for this variation and improve overload protection (OLP) accuracy, an offset proportional to the input voltage is added on the CS signal.

The offset is created by an internal sourcing current on CS that flows across an external resistor (R_{HVCS}). The current source is proportional to the HV voltage (see Figure 5).

The compensation level can be externally adjusted by R_{HVCS}.

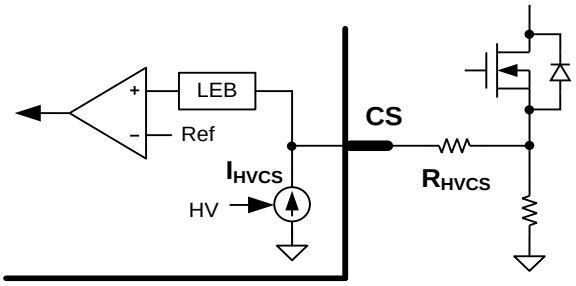


Figure 5: Implementation of the Line Compensation Function

The compensation current is at its maximum value (corresponding to the HV voltage) only when the peak current reference is at its maximum limit. The compensation current is removed gradually when f_{SW} drops below f_{SW-H}. Compensation is removed once the peak current reference drops below V_{LC-END}. (see Figure 6).

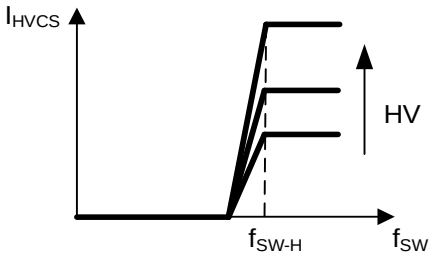


Figure 6: Current on CS for Line Compensation

Driver

The driver capability is specified in the PDRV section of Electrical Characteristics section on page 6. The voltage is clamped internally at V_{CLAMP} (typically 14.5V) to guarantee that the external MOSFET operates safely.

Under-Voltage Lockout (UVLO)

If V_{CC} drops below V_{CC-MIN} (typically 8.3V), under-voltage lockout (UVLO) stops primary switching immediately. V_{CC} is recharged by the current source from HV.

Primary-Side Protections

The primary IC provides full protection features and responds to faults on the secondary side.

If a protection is triggered, switching is terminated immediately, and V_{CC} drops. If V_{CC} drops to V_{CC-AUT}, the related protection flag is reset, and the HV current source is enabled to charge the VCC capacitor. Then the primary IC initiates normal start-up logic and operation.

Short-Circuit Protection (SCP)

If the CS voltage exceeds V_{SCP}, the IC triggers short-circuit protection (SCP), which means that the peak current is not effectively regulated by its limit due to a fault condition, such as winding short circuit or output short circuit. During SCP, auto-restart protection mode is triggered. A reduced LEB time (t_{LEB-S}, typically 250ns) is also adopted by the SCP comparator to prevent a false trigger by the turn-on spike.

For the MPX2002, the behavior during SCP is designed as a surge-proof approach. If SCP is triggered for the first time, the IC does not shut down completely. Instead, primary switching is blanked for t_{SCP2}, during which the primary IC does not respond to the secondary IC unless there is a protection signal.

After the blanking time passes, the primary IC resumes switching. If SCP is triggered for a second time within 8 switching cycles, the primary IC stops switching and initiates auto-restart recovery. If the short-circuit condition is removed after the first SCP event, the primary IC resets the SCP counter and resumes normal operation.

CS Short Protection (SSP)

If the CS voltage does not exceed V_{CSS} (typically 50mV) within t_{SSP} (typically 5.8µs) after the primary MOSFET turns on, the primary IC initiates CS short protection (SSP) to prevent the primary current from overstress due to a CS short.

SSP detection is only executed during the first few switching cycles to prevent the CS pin or CS resistor from being directly shorted to GND due to improper soldering.

Over-Voltage Protection (OVP)

If V_{CC} exceeds V_{CC-OVP} (typically 26V), the primary IC stops switching after a validation time ($t_{VCC-OVP}$). Over-voltage protection (OVP) triggers auto-restart mode. The primary IC initiates OVP

to prevent components from breaking down due to overstress.

Brownout Protection (BOP)

For more information about brownout protection (BOP), see the Start-Up with Brown-In/Brownout Detection section on page 19 and the Brownout Protection during Normal Operation section on page 19. BOP triggers auto-restart mode.

Primary Over-Temperature Protection (POTP)

To prevent thermal damage on the chip, primary over-temperature protection (POTP) shuts down switching immediately if the junction temperature exceeds T_{OTP-P} (typically 150°C). The protection flag is latched until the junction temperature drops by $T_{\Delta-P}$ (typically 40°C).

Primary Over-Current Protection (POCP)

For more information about primary over-current protection (POCP), see the Start-Up with Brown-In/Brownout Detection section on page 19. If the primary IC does not receive a start-up signal from the secondary IC for t_{OCP} (typically 55ms), POCP is triggered and initiates auto-restart mode.

Primary External Protection (PEP)

PEP is a general-purpose protection pin. When the IC starts to operate, it begins to monitor the voltage on PEP every 100µs to 200µs. There is an internal current flowing out of PEP with a fixed value of I_{PEP} (typically 110µA). A resistor or a bipolar junction transistor (BJT) can be connected to PEP to set the target voltage. If the PEP voltage is below the protection trigger threshold (V_{PEP-T}, typically 0.5V) and the condition lasts longer than the trigger delay time (t_{PEP-T}, typically 300µs), the PEP flag is set to high. The PEP flag does not reset until V_{CC} drops below V_{CC-AUT}.

PEP detection acts as a switch mode. The current source is only on for several microseconds for every 100µs to 200µs, which can save power loss during steady state.

Typically, PEP can be used to implement an OTP function for external power devices (e.g. the primary MOSFET) by connecting PEP to a negative temperature coefficient (NTC) resistor (see Figure 7). PEP can also configure the OVP threshold.

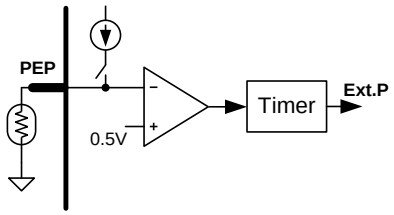


Figure 7: Primary External Protection

Response to the Secondary Protections

For more information about responses to secondary protections, see the Start-Up with Brown-In/Brownout Detection section on page 19.

SECONDARY IC FUNCTIONS

Secondary IC Power Supply Management

VDD is the general-purpose power supply for the secondary IC. The VDD voltage (V_{DD}) can be supplied by itself or the output voltage (V_{OUT}). Figure 8 shows the circuit when V_{DD} is supplied by V_{OUT}.

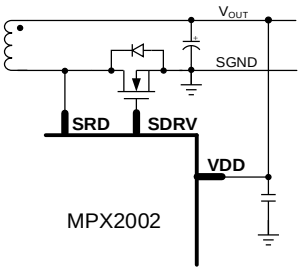


Figure 8: V_{DD} Supply from Output

When the voltage supplied from V_{OUT} is below V_{DD-C}, the current supply to V_{DD} comes from SRD to allow the MPX2002 to support low-output applications.

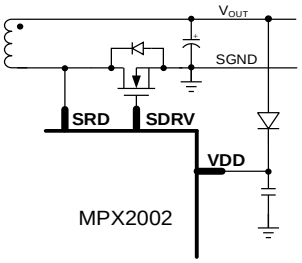


Figure 9: V_{DD} Supply from Both the Output and SRD

By allowing V_{DD} to be powered by V_{OUT} and SRD, the SR driver has an expedited start-up, which limits the voltage spike caused by the body diode's reverse recovery. Otherwise, the current supply for V_{DD} comes from V_{OUT} for optimized efficiency.

Synchronous Rectification Turn On

After the primary-side MOSFET turns off, the inductor current is transferred from the primary side to the secondary side, which makes the SR MOSFET's drain voltage drop. When the voltage on the SRD pin crosses the turn-on threshold (V_{SR-ON}), the secondary IC starts to set the SR driver, and the SR MOSFET turns on after the turn-on delay (t_{SR-OND}).

When the SR MOSFET is on, there is a minimum on time (t_{ON-MIN}) that prevents the MOSFET from being falsely turned off by parasitic oscillation. During the minimum on time, the turn-off action is not completely blanked, and the turn-off threshold rises to $V_{SR-OFFM}$. This ensures that the SR MOSFET can always be turned off under severe situations, even during the minimum on time.

Synchronous Rectification Conduction

During the SR conduction period, the gate voltage is regulated based on the forward voltage drop across the MOSFET (V_{SRD}). When V_{SRD} is below the internal reference voltage, the gate driver fully turns on to reach the minimum turn-on resistance. V_{SRD} rises as the current decreases. When V_{SRD} exceeds the reference voltage, the gate voltage is pulled down to increase the turn-on resistance, and the regulation voltage quickly switches to $-V_{FWD}$. This means that the rising of V_{SRD} is regulated to a certain level, which effectively prevents a premature turn-off while maximizing the SR conduction period.

Synchronous Rectification Turn Off

As the inductor current reaches zero during discontinuous conduction mode (DCM), V_{SRD} rises to zero. Once V_{SRD} exceeds V_{SR-OFF}, the gate immediately pulls down to turn off the SR MOSFET (see Figure 10).

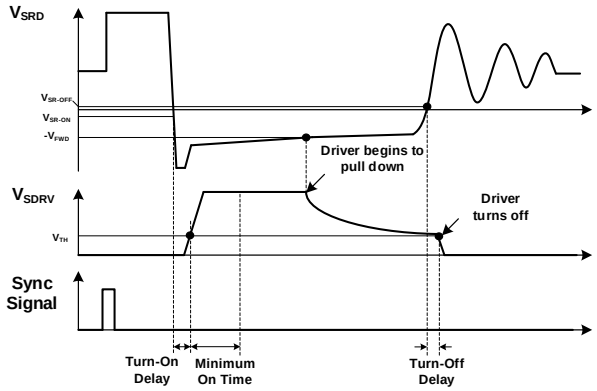


Figure 10: SR Operation during DCM

During continuous conduction mode (CCM), the secondary IC generates a signal based on a dead time to determine when the SR MOSFET turns off and the primary MOSFET turns on. This feature reduces the chances of shoot-through (see Figure 11).

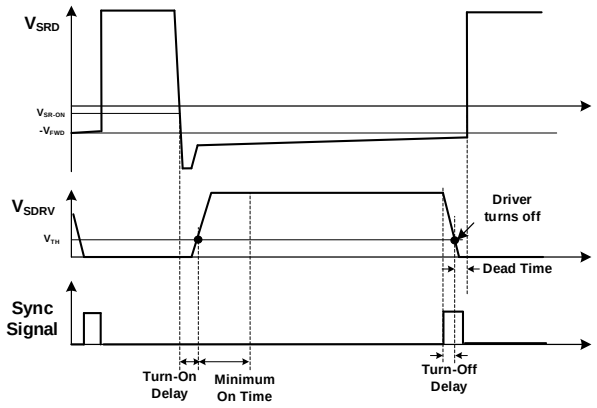


Figure 11: SR Operation during CCM

In burst mode, the SR gate block turns off to reduce power loss. When the IC exits burst mode, the SR gate block turns on after one switching operation.

Output Voltage Regulation

The internal error amplifier regulates the output voltage (V_{OUT}). V_{OUT} is fed back through the FB pin and external dividing resistors, and is then compared to the internal precise reference voltage (V_{REF}). The compensation voltage is generated by the transconductance amplifier. In this situation, the external compensation network can be designed by the COMP pin to adjust the regulation performance.

Due to the error amplifier behavior, the COMP voltage can indicate the output load condition, such as when the COMP voltage rises as the load increases.

The COMP voltage is sent to the pulse-frequency modulation (PFM) block to modulate the switching frequency (f_{SW}). A lower COMP voltage results in a lower f_{SW}, and there are also upper and lower limitations on the frequency modulation. When the COMP voltage exceeds V_{FS-MAX}, f_{SW} is clamped at the maximum frequency (f_{SW-MAX}). When the COMP voltage is below V_{BURST}, the switching pulse stops until the COMP voltage exceeds V_{BURST} + $V_{BURST-HYS}$. f_{SW-MIN} is the minimum f_{SW} corresponding to V_{BURST}. The first switching pulse is sent without any delay once it exits burst mode. This closed-loop regulation controls the output voltage.

Cable Drop Compensation

The voltage drop on the cable is proportional to the output current, which is reflected on the voltage of the IS pin (see Figure 12). The maximum CDC voltage on FB is V_{CDC_MAX}. The cable drop compensation voltage can be calculated with Equation (20) on page 29.

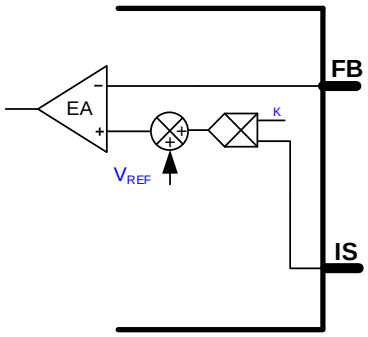


Figure 12: Cable Drop Compensation

Quasi-Resonant (QR) Mode Switching

The secondary-side IC achieves quasi-resonant (QR) mode by comparing the SRD voltage and V_{DD} when the converter runs in DCM. The primary side switching is always on when the primary side switch is near its minimum voltage. This reduces power loss and minimizes EMI noise.

The primary IC has a variable current limit when f_{SW} is below f_{SW-H}, which means that switching is irregular when the IC operates in QR mode. To prevent the IC from entering this mode, the QR is disabled when f_{SW} is below f_{SW-H}. At this point, the primary side's on signal does not wait for the QR detection period.

The IC can immediately exit QR mode when certain operations are detected. For example, it exits QR mode under the following conditions:

- If CCM is required (the load becomes heavy)
- More than 6 oscillation valleys are detected
- The oscillation period during DCM lasts longer than 20μs

Secondary-Side Protections

Secondary Under-Voltage Lockout (SUVLO)

The secondary IC does not begin operating until V_{DD} rises above V_{DD-ON} (typically 4.5V). If V_{DD} falls below V_{DD-OFF} (typically 4.25V), the secondary IC shuts down, and all internal signals are reset. To avoid voltage spike influences (mainly caused by the capacitor's ESR), any valid UVLO detection typically requires a 10μs delay time.

Secondary Overload Protection (SOLP)

The IS pin senses the output current with external sensing resistors. When the IS voltage (V_{IS}) exceeds the overload protection threshold (V_{IS-OLP}) and lasts longer than the overload protection delay time (t_{OLP}), the secondary overload protection (SOLP) flag is set to high and switching stops. The SOLP flag is reset when the secondary IC or primary IC trigger UVLO.

If the IS pin is shorted to SGND, the SOLP function is still available, though the COMP signal is less accurate. SOLP is implemented based on the COMP signal. If the COMP voltage exceeds V_{FS-MAX} (higher than the threshold where the switching frequency is set at the maximum limit), the OLP timer begins counting. SOLP is triggered after the timer runs out.

Once SOLP is triggered, COMP is internally shorted to SGND, and it is not released until SOLP is cleared.

Secondary Over-Voltage Protection (SOVP)

If the FB voltage exceeds the OVP threshold (V_{OVP}) and lasts longer than the OVP delay time (t_{OVP-D}), the secondary over-voltage protection (SOVP) flag is set to high and switching stops.

Switching reverts to normal modulation once the FB voltage returns to V_{REF}. During SOVP, there is an extra current (I_{BLD}) drawn from the VDD pin. This current helps ease the over-voltage condition by discharging the VDD capacitor.

FB Open-Loop Protection (FBOLP)

If there are fault conditions (i.e. FB shorted to SGND or an upper FB resistor is open), the MPX2002 loses its feedback loop and the output voltage goes out of regulation. To protect the circuit from being further damaged, the MPX2002 implements a cross check between V_{OUT} and the FB voltage.

If V_{DD} exceeds V_{DD-RDY}, this means that V_{DD} is no longer supplied by SRD. If the FB voltage is still below V_{FBO}, the secondary IC initiates FB open-loop protection (FBOLP) after a validation time (t_{FBO}).

The internal leakage current (I_{FB}) guarantees that the FB voltage is always pulled to SGND when the FB pin is open.

SR Gate Open/Short Protection (SGOP/SGSP)

If SDRV is set but the SRD voltage remains low during the conduction period, this indicates that the SR may not be successfully turned on due to an unexpected fault condition, such as an open gate or a broken MOSFET. The MPX2002 implements SR gate open protection (SGOP) to protect the circuitry from being further damaged under these conditions.

The threshold for SR driver open detection is V_{SGO}, and the condition must remain for 8 consecutive switching cycles for validation. If SGOP is triggered, the secondary IC does not recover until there is another primary IC self start-up.

If SDRV detects that the connected resistor is below 1kΩ once V_{DD} reaches V_{DD-ON}, this means that SDRV is shorted to SGND. Switching stops until the primary IC starts up again.

SRD Abnormal Protection (SRDP)

If the power supply of the secondary IC is successfully set up and there are 7 consecutive primary switching pulses but the SR gate is not triggered by SRD detection, SRD abnormal protection (SRDP) is triggered. Switching stays off and COMP is pulled to ground. The secondary IC does not recover until the secondary IC or primary IC trigger UVLO. Then the secondary IC starts switching once a valid signal is detected on SRD.

Secondary Over-Temperature Protection (SOTP)

To prevent any thermal damage on the chip, secondary over-temperature protection (SOTP) sets the SOTP flag high if the junction temperature exceeds T_{OTP-S}. The protection flag is latched until the junction temperature drops by $T_{\Delta-S}$.

APPLICATION INFORMATION

Selecting the VCC Capacitor

Figure 13 shows the start-up circuit.

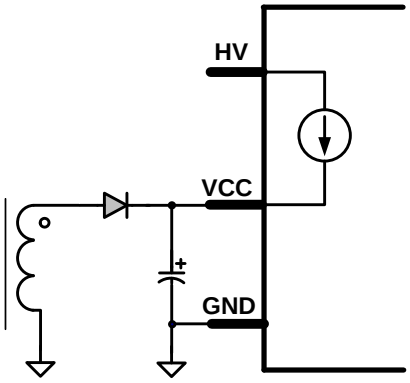


Figure 13: Start-up Circuit

V_{CC} is initially charged by HV. When V_{CC} reaches $V_{CC-IOFF}$, HV stops charging V_{CC} and the IC starts to operate. To guarantee a successful start-up, the output voltage should be set up before V_{CC} drops to V_{CC_MIN}. For most applications, choose a VCC capacitor value that is about 22μF. To ensure safe operation across the entire input and output range (especially under no load conditions), V_{CC} should have some margin. Usually, the minimum V_{CC} is recommended to be about 1V greater than the minimum operating voltage (V_{CC-MIN}). The recommended VCC capacitor (C_{VCC}) value can be calculated with Equation (1):

$$C_{VCC} > \frac{I_{OP} \times t_{START-UP}}{V_{CC-IOFF} - V_{CC-MIN}} \quad (1)$$

Designing the Transformer's Magnetizing Inductance

The MPX2002's maximum switching frequency (f_{SW}) is recommended to be 80kHz at maximum. With internal slope compensation, the MPX2002 supports CCM when the duty cycle exceeds 50%. Set a ratio (K_P) for the primary inductor's ripple current amplitude vs. the peak current value to $0 < K_P \leqslant 1$, where $K_P = 1$ for DCM.

Figure 14 shows the relevant waveforms. A larger inductor leads to a smaller K_P, which can reduce the RMS current but increase transformer size. An optimal K_P value is between 0.6 and 0.8 for the universal input range, or 0.8 to 1 for $230V_{AC}$ input range.

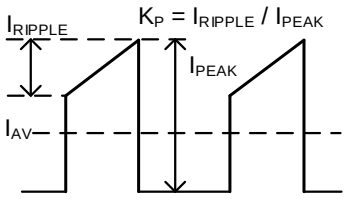


Figure 14: Typical Primary Current Waveform

The input power (P_{IN}) at the minimum input can be estimated with Equation (2):

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (2)$$

Where V_{OUT} is the output voltage, I_{OUT} is the rated output current, and η is the estimated efficiency (typically between 0.85 and 0.9 depending on the input range and output application).

During CCM at the minimum input, the converter's maximum duty cycle can be calculated with Equation (3):

$$D_{MAX} = \frac{(V_{OUT} + V_{FWD}) \times N_{PS}}{(V_{OUT} + V_{FWD}) \times N_{PS} + V_{IN(MIN)}} \quad (3)$$

Where V_{FWD} is the secondary SR MOSFET regulated forward voltage, N_{PS} is the transformer's primary-secondary turn ratio, and $V_{IN(MIN)}$ is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time can be estimated with Equation (4):

$$t_{ON} = D \times t_S \quad (4)$$

Where t_S is the frequency jitter's dominant switching period. The relationship between t_{SMIN} and f_{SW-MAX} can be calculated with Equation (5):

$$\frac{1}{t_{SMIN}} = f_{SW-MAX} = 80kHz \quad (5)$$

The average value for the primary current can be estimated with Equation (6):

$$I_{AV} = \frac{P_{IN}}{V_{IN(MIN)}} \quad (6)$$

The peak value for the primary current can be calculated with Equation (7):

$$I_{PEAK} = \frac{I_{AV}}{(1-\frac{K_P}{2})\times D} \quad (7)$$

The ripple value for the primary current can be estimated with Equation (8):

$$I_{RIPPLE} = K_P \times I_{PEAK} \quad (8)$$

The valley value for the primary current can be calculated with Equation (9):

$$I_{VALLEY} = (1-K_P)\times I_{PEAK} \quad (9)$$

The magnetizing inductance can be estimated with Equation (10):

$$L_M = \frac{V_{IN(MIN)} \times t_{ON}}{I_{RIPPLE}} \quad (10)$$

Selecting the **Current-Sense Resistor**

Figure 15 shows the peak current comparator logic.

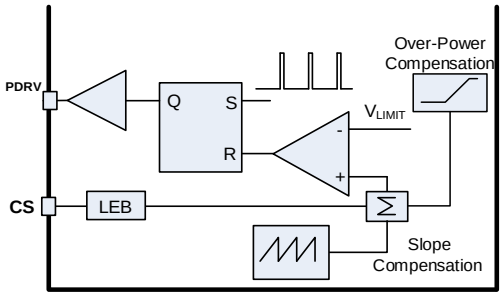


Figure 15: Peak-Current-Comparator Circuit Logic

Figure 16 shows the peak current comparator waveform.

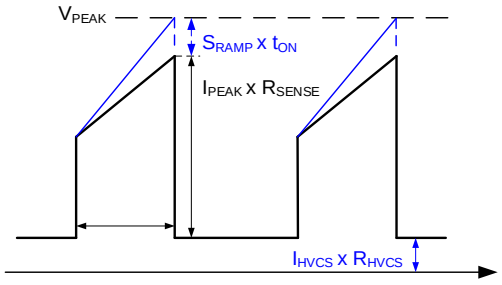


Figure 16: Peak Current Comparator Waveform

When the sum of the voltage on the current-sense resistor, the voltage on the over-power compensation resistor, and the voltage generated by the slope compensation block reach V_{PEAK}, the comparator goes high to reset the RS flip-flop, and DRV is pulled down to turn off the MOSFET (see Figure 15). The maximum current limit is $V_{IPK-MAX}$. The slope compensator is S_{RAMP}, and at low line the over-power compensation is zero. Given a certain margin, V_{PEAK} is equal to 0.95 x $V_{IPK-MAX}$ under full load. The voltage on the current-sense resistor can be calculated with Equation (11):

$$V_{SENSE} = 95\% \times V_{IPK-MAX} - S_{RAMP} \times t_{ON} \quad (11)$$

The current-sense resistor can be estimated with Equation (12):

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK}} \quad (12)$$

Select a current-sense resistor with an appropriate power rating. The current-sense resistor's power loss can be calculated with Equation (13):

$$P_{SENSE} = \left[\left(\frac{I_{PEAK}+I_{VALLEY}}{2}\right)^2 + \frac{1}{12}\left(I_{PEAK}-I_{VALLEY}\right)^2\right] \times D \times R_{SENSE} \quad (13)$$

Over-Power Compensation and Selecting the Low-Pass Filter on CS

The MPX2002 has an over-power compensation (OPC) function that draws current from CS. The purpose of OPC is to minimize the OLP difference caused by different input voltages. The offset current is proportional to the input peak voltage sensed by HV.

Assume the resistor in the current-sense loop is R_{HVCS} and the bus voltage is V_{HV}. The compensation voltage on the CS pin can be estimated with Equation (14):

$$V_{OPC} = R_{HVCS} \times I_{HVCS} \quad (14)$$

The compensation criteria makes the COMP pin voltage under high-line, full-load conditions similar to its voltage under low-line, full-load conditions. Generally, R_{HVCS} is recommended to be between hundreds of Ohms to one thousand Ohms.

A small capacitor is connected to the CS pin and R_{HVCS} to form a low-pass filter for noise filtering when the MOSFET turns on and off (see Figure 17 on page 28).

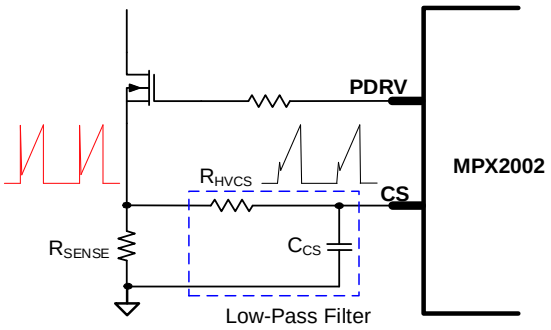


Figure 17: Low-Pass Filter on CS

The low-pass filter's R x C constant should not exceed 1/3 of the leading-edge blanking period for SCP (t_{LEB-S}, typically 250ns). Otherwise, the filtered sensed voltage cannot reach the SCP point to trigger SCP if an output short circuit occurs.

Ramp Compensation

When adopting peak current control, subharmonic oscillations occur when the duty cycle exceeds 50% (D > 0.5) in CCM. The MPX2002 provides internal ramp compensation to solve this issue. Use the coefficient α to determine whether the ramp compensation is appropriate. α can be calculated with Equation (15):

$$\alpha = \frac{\frac{D_{MAX} \times V_{IN(MIN)}}{(1-D_{MAX}) \times L_M} \times R_{SENSE} - S_{RAMP}}{\frac{V_{IN(MIN)}}{L_M} \times R_{SENSE} + S_{RAMP}} \quad (15)$$

Where S_{RAMP} is the minimum internal slope value of the compensation ramp. For stable operation, α must be less than 1. The primary-side slew rate can be estimated with Equation (16):

$$\frac{V_{IN(MIN)}}{L_M} \times R_{SENSE} \quad (16)$$

The equivalent secondary-side voltage sensed by the CS resistor can be calculated with Equation (17):

$$\frac{D_{MAX} \times V_{IN(MIN)}}{(1-D_{MAX}) \times L_M} \times R_{SENSE} \quad (17)$$

External Protection through the PEP Pin

The PEP pin can be used to implement an over-temperature protection (OTP) function for external power devices (e.g. the primary MOSFET) by connecting a negative temperature coefficient (NTC) resistor to this pin (see the Primary External Protection (PEP) section on page 22). Figure 18 shows OTP through the PEP pin.

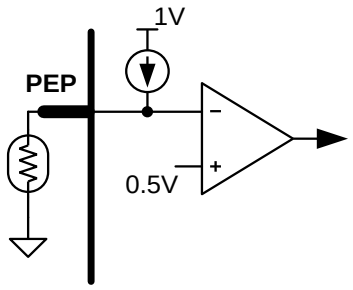


Figure 18: OTP through PEP

The sourcing current for PEP is I_{PEP}. At working temperatures, the NTC resistor should satisfy a particular relationship, estimated with Equation (18):

$$I_{PEP} \times R_{PEP} > V_{PEP-T} \quad (18)$$

When the temperature increases, the NTC resistance decreases. Figure 19 shows the typical waveform for NTC resistance vs. temperature.

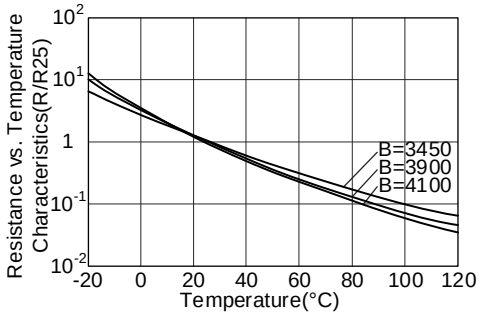


Figure 19: NTC Resistance vs. Temperature

I_{PEP} can also meet the condition at the protected temperature value, calculated with Equation (19):

$$I_{PEP} \times R_{PEP} < V_{PEP-T} \quad (19)$$

The PEP pin can also provide over-voltage protection (OVP) using several passive components. The breakdown voltage (BV) of the Zener diode should be equal to the over voltage threshold when an over-voltage condition occurs. For example, the BV of Zener diode is equal to the V_{CC} over-voltage threshold when a secondary over-voltage condition occurs.

Figure 20 shows OVP through the PEP pin.

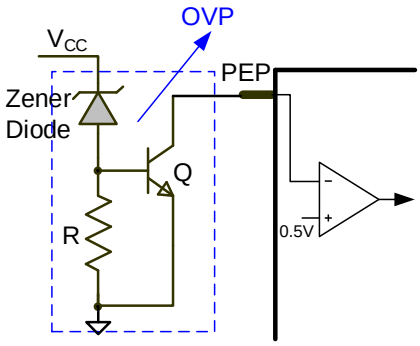


Figure 20: OVP through PEP

Cable Drop Compensation

The CP voltage is proportional to the IS voltage (V_{IS}). The default ratio between V_{IS} and the compensation voltage on FB is 3:3.7, which means that when the IS voltage reaches its maximum value (40mV), the compensation voltage on the FB reference is about 50mV. The cable drop's compensation voltage on the output voltage can be calculated with Equation (20):

$$V_{CP} = R_{IS} \times I_{OUT} \times \frac{3.7}{3} \times \frac{(R_H + R_L)}{R_L} \quad (20)$$

Cable drop compensation is disabled when the IS pin is shorted to GND on the secondary side.

Overload Protection through the IS Pin

Overload protection can be achieved through the IS pin. Place one high-precision current-sense resistor in the output power loop and measure the voltage drop on this resistor through the IS pin. When V_{IS} exceeds V_{OLP}, the MPX2002 enters secondary OLP (SOLP) after a certain time (t_{OLP}). This sensing resistor follows the relationship estimated with Equation (21):

$$R_{IS} = (0.8 \sim 0.9) \times \frac{V_{OLP}}{I_{OUT}} \quad (21)$$

Figure 21 shows OLP through the IS pin.

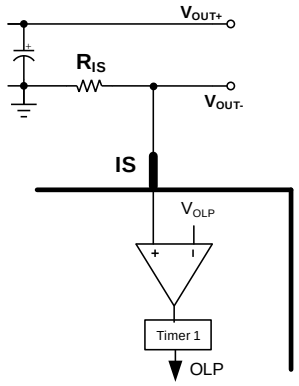


Figure 21: OLP through the IS Pin

If R_{IS} can be shorted, OLP through the IS pin is disabled.

Selecting the SR MOSFET

Power MOSFET selection is a tradeoff between $R_{DS(ON)}$ and Q_G. To improve efficiency, use a MOSFET with a lower $R_{DS(ON)}$. Generally, a MOSFET with a lower $R_{DS(ON)}$ has a higher Q_G, which reduces the turn-on/off speed and increases switching loss.

If Q_G is not optimized, the gate driving signal may turn off prematurely. A MOSFET with an $R_{DS(ON)}$ that is too low is not recommended because the gate driver is pulled low when the MOSFET's drain-source voltage (V_{DS}, calculated by $-I_{SD} \times R_{DS(ON)}$) exceeds $-V_{FWD}$.

The MOSFET's $R_{DS(ON)}$ does not contribute to conduction loss, because V_{DS} is adjusted at $-V_{FWD}$ during the driving period (when the switching current is fairly small). The conduction loss can be calculated with Equation (22):

$$P_{CON} = -V_{DS} \times I_{SD} \approx I_{SD} \times V_{FWD} \quad (22)$$

Figure 22 on page 30 shows the typical waveform when a flyback application works in DCM. Assume a 50% duty cycle, and the output current is I_{OUT}.

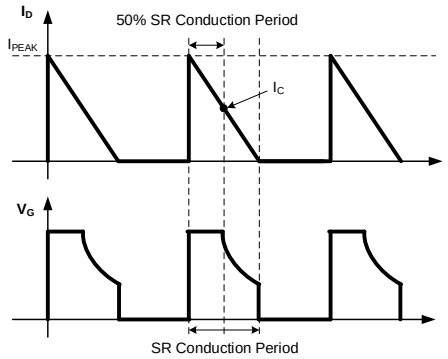


Figure 22: SR Waveforms in QR Mode

To effectively utilize the MOSFET's $R_{DS(ON)}$, the MOSFET should be completely turned on for at least 50% of the SR conduction period. V_{DS} can be estimated with Equation (23):

$$V_{DS} = -I_C \times R_{ON} = -2 \times I_{OUT} \times R_{ON} \leq -V_{FWD} \quad (23)$$

Where V_{FWD} is the forward voltage threshold.

The MOSFET's $R_{DS(ON)}$ should not be lower than 12 / I_{OUT} (in mΩ). For example, for a 5A application, $R_{DS(ON)}$ should not be below 2.4mΩ.

Design Example

Table 1 shows a design example when using the MPX2002 for a 65W PD charger application.

Table 1: Design Specifications

Parameter	Symbol	Value
Input specifications	V_{IN}	90V_{AC} to 265V_{AC}, 47Hz to 63Hz
Output specifications	V_{OUT} / I_{OUT}	5V_{DC} / 0A to 3A, 9V_{DC} / 0A to 3A, 12V_{DC} / 0A to 3A, 15V_{DC} / 0A to 3A, 20V_{DC} / 0A to 3.25A

PCB Layout Guidelines

PCB layout is vital to achieve reliable operation, excellent EMI performance and efficient thermal performance. For the best results, follow the guidelines below and refer to Figure 23 and Figure 24 on page 32:

1. Minimize the power stage loop area, including the primary power loop (C1, C2, C3, C4 - T1-Q1 - R1, R2, R3 - C1), the snubber loop (T1-B1 - R4 - D1 - R5 ,C6 - T1), and the secondary power loop (T1 - C18, C19 - Q3 - T1).
2. Separate the IC GND and power GND.
3. Connect the heat sink to the primary GND plane to improve EMI and thermal dissipation.
4. Place the decoupling capacitors (for VCC, PEP, CS, COMP, VDD, and FB) close to the IC.
5. Route the EMI filter far from the hopping point.
6. Ensure that there is no trace beneath the IC for isolation requirements.
7. Keep the Y-capacitor as close as possible to the IC to reduce CM noise.

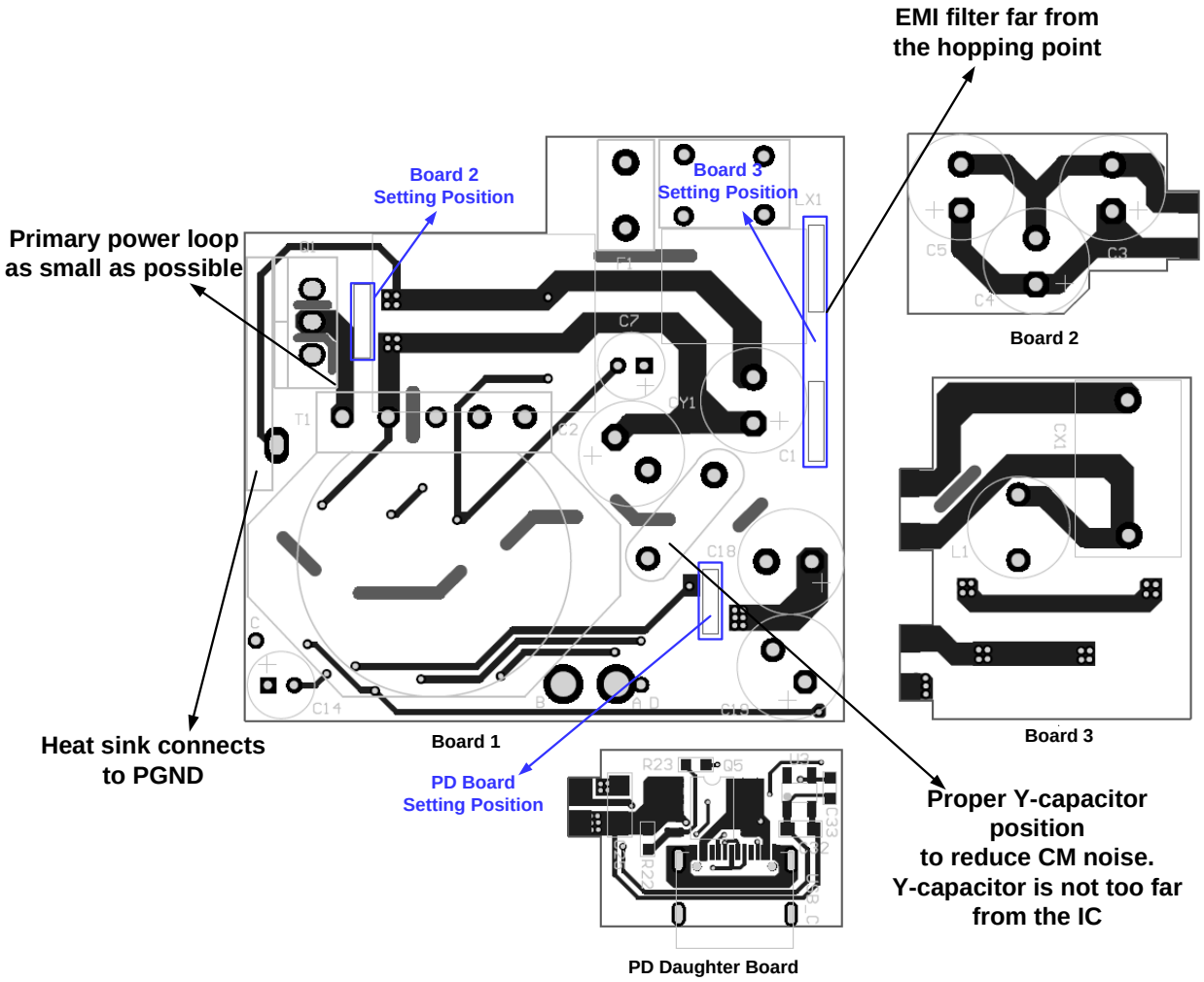


Figure 23: Recommended PCB Layout for 65W PD Adapter Design (Top-Side)

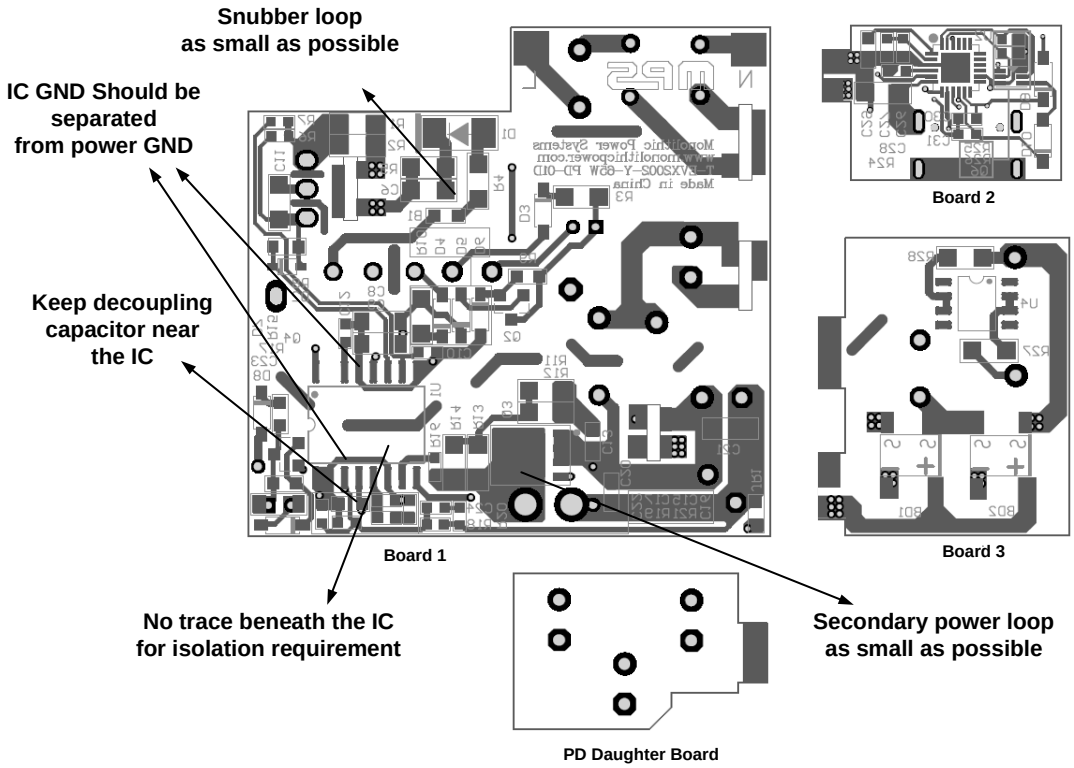


Figure 24: Recommended PCB Layout for 65W PD Adapter Design (Bottom-Side)

TYPICAL APPLICATION CIRCUIT

Figure 25 shows the MPX2002's typical application circuit with a universal input and 65W output specification.

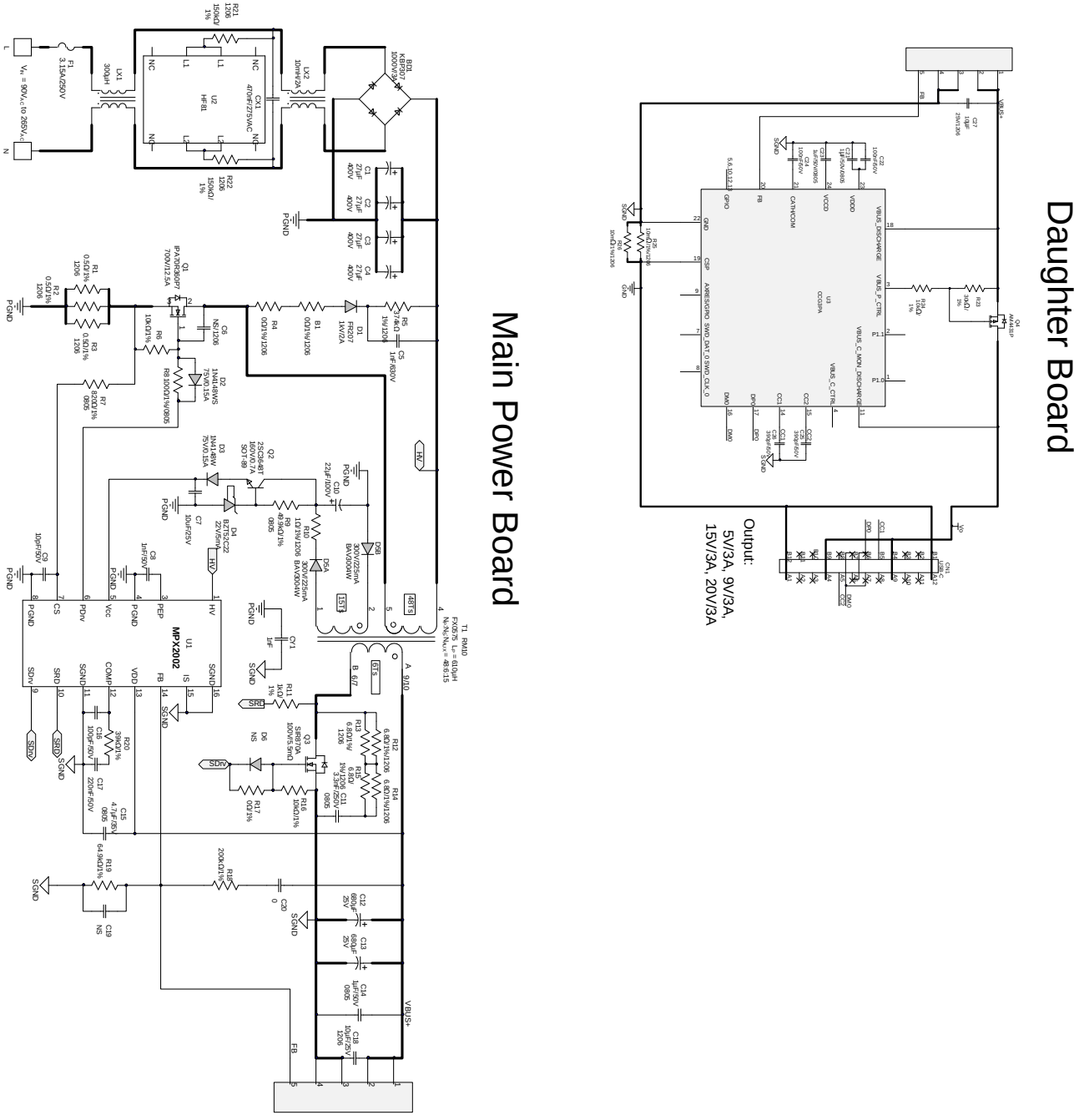
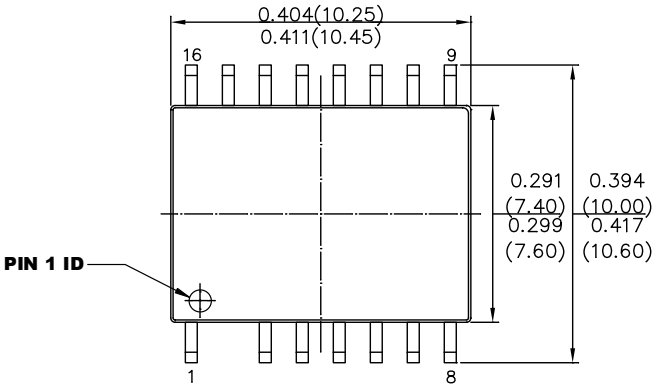


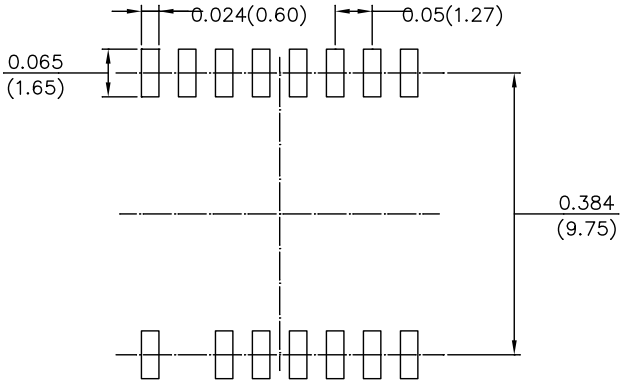
Figure 25: Example of the 65W PD Typical Application

PACKAGE INFORMATION

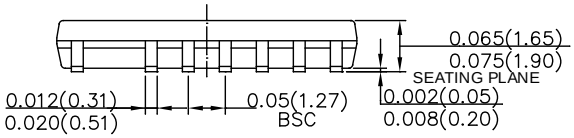
TSOICW16-15



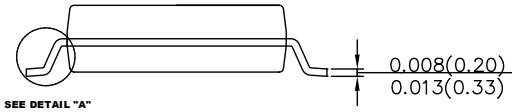
TOP VIEW



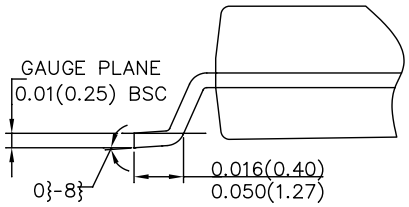
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



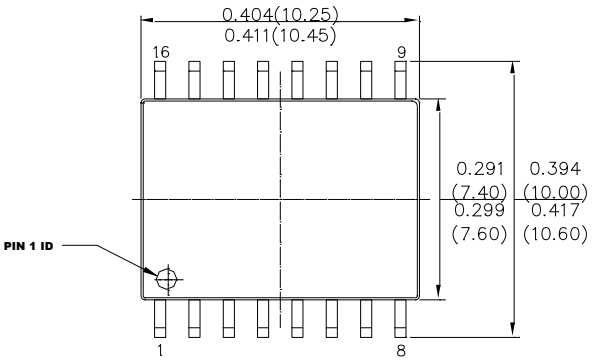
DETAIL "A"

NOTE:

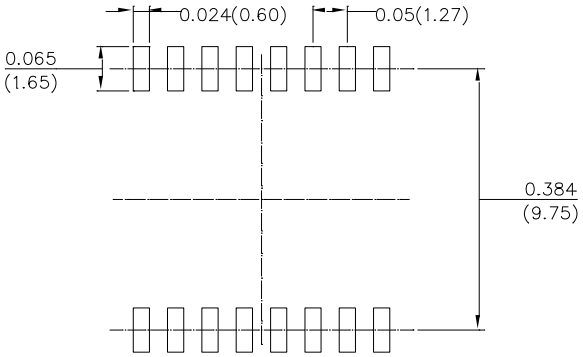
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

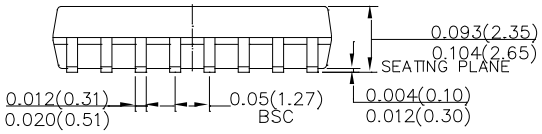
SOICW-16



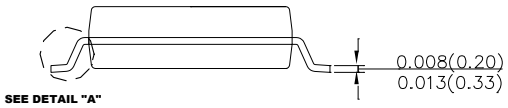
TOP VIEW



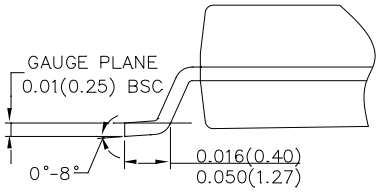
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

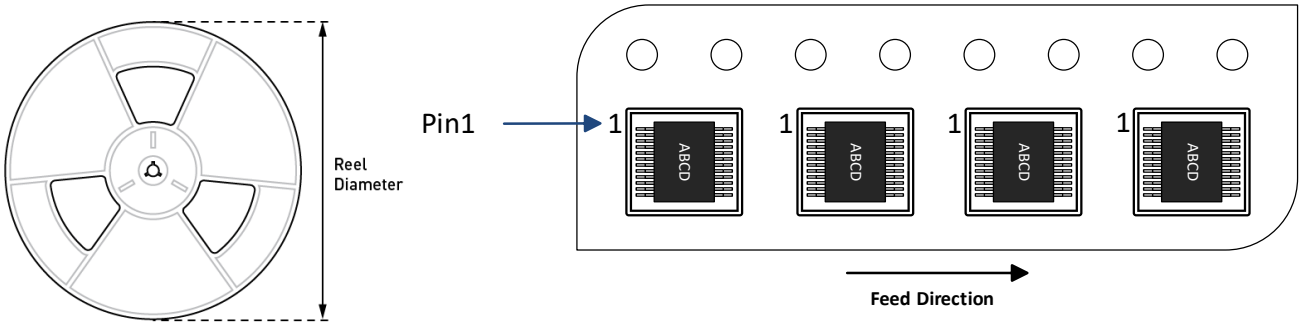


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPX2002GYT-Z	TSOICW16-15	1000	47	13in	24mm	12mm
MPX2002GY-Z	SOICW-16					

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-
1.1	8/23/2022	Added “DIN VDE V 0884-17 in Progress” to the Features section	1