FAIRCHILD

SEMICONDUCTOR™

NM25C160
16,384-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C160 is a 16,384-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C160 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C160 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE program disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against accidental data changes. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

■ 2.1 MHz clock rate @ 2.7V to 5.5V

■ 16,384 bits organized as 2,048 x 8

■ Multiple chips on the same 3-wire bus with separate chip select lines

■ Self-timed programming cycle

■ Simultaneous programming of 1 to 16 bytes at a time

■ Status register can be polled during programming to monitor READY/BUSY

■ Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection

■ Block write protect feature to protect against accidental writes

■ Endurance: 1,000,000 data changes

■ Data retention greater than 40 years

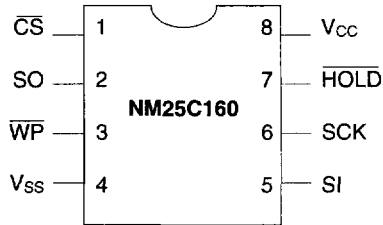■ Packages available: 8-pin DIP, 8-pin SO, or 8-pin TSSOP

Block Diagram
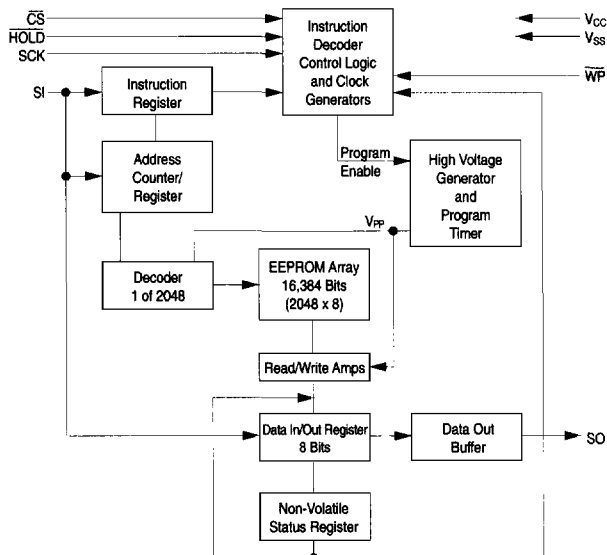
DS012402-1

Connection Diagram

**Dual-In-Line Package (N), SO Package (M8),
and TSSOP Package (MT8)**

```
        ___
        CS  ──┤ 1        8 ├── V_CC
                               ____
        SO  ──┤ 2        7 ├── HOLD
        ___       NM25C160
        WP  ──┤ 3        6 ├── SCK

       V_SS ──┤ 4        5 ├── SI
```

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Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

NM 25 C XX LZ E XX

Letter	Description
Package	
N	8-pin DIP
M8	8-pin SO
MT8	8-pin TSSOP
Temp. Range	
None	0 to 70°C
V	-40 to +125°C
E	-40 to +85°C
Voltage Operating Range	
Blank	4.5V to 5.5V
L	2.7V to 5.5V
LZ	2.7V to 5.5V and <1µA Standby Current
Density	
160	16K, mode 0
C	CMOS technology
Interface	
25	SPI - 3 Wire
NM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage $4.5 \leq V_{CC} \leq 5.5V$ Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C160	0°C to +70°C
NM25C160E	-40°C to +85°C
NM25C160V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS} = V_{IL}$		3	mA
I_{CCSB}	Standby Current	$\overline{CS} = V_{CC}$		50	μA
I_{IL}	Input Leakage	$V_{IN} = 0V$ to V_{CC}	-1	+1	μA
I_{OL}	Output Leakage	$V_{IN} = 0V$ to V_{CC}	-1	+1	μA
V_{IL}	CMOS Input Low Voltage		-0.3	$V_{CC} * 0.3$	V
V_{IH}	CMOS Input High Voltage		$V_{CC} * 0.7$	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -0.8$ mA	$V_{CC} - 0.8$		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	μs
t_{FI}	Input Fall Time			2.0	μs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		V
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	CS Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay from Clock Low	$C_L = 200$ pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			100	ns
t_{DF}	Output Disable Time	$C_L = 200$ pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–16 Bytes		10	ms

Capacitance $T_A = 25°C$, $f = 1$ MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	$C_L = 200$ pF
Input Pulse Levels	$0.1 * V_{CC} - 0.9 * V_{CC}$
Timing Measurement Reference Level	$0.3 * V_{CC} - 0.7 * V_{CC}$

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in an SCK clock cycle, $t_{CLH} + t_{CLL}$ must be greater than or equal to 476 ns. For example, if $t_{CLL} = 190$ ns, then the minimum $t_{CLH} = 286$ ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V$_{CC}$ ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C160L/LZ	0°C to +70°C
NM25C160LE/LZE	-40°C to +85°C
NM25C160LV	-40°C to +125°C
Power Supply (V$_{CC}$)	2.7V–5.5V

DC and AC Electrical Characteristics 2.7V ≤ V$_{CC}$ ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C160LE Min.	25C160LE Max.	25C160LV Min	25C160LV Max	Units
I$_{CC}$	Operating Current		$\overline{CS}$ = V$_{IL}$		3		3	mA
I$_{CCSB}$	Standby Current	L	$\overline{CS}$ = V$_{CC}$		10		10	µA
		LZ			1		N/A	µA
I$_{IL}$	Input Leakage		V$_{IN}$ = 0 to V$_{CC}$	-1	1	-1	1	µA
I$_{OL}$	Output Leakage		V$_{OUT}$ = GND to V$_{CC}$	-1	1	-1	1	µA
V$_{IL}$	Input Low Voltage			-0.3	V$_{CC}$ * 0.3	-0.3	V$_{CC}$ * 0.3	V
V$_{IH}$	Input High Voltage			V$_{CC}$ * 0.7	V$_{CC}$ + 0.3	V$_{CC}$ * 0.7	V$_{CC}$ + 0.3	V
V$_{OL}$	Output Low Voltage		I$_{OL}$ = 2.1 mA		0.4		0.4	V
V$_{OH}$	Output High Voltage		I$_{OH}$ = −0.8 mA	V$_{CC}$ - 0.8		V$_{CC}$ - 0.8		V
f$_{OP}$	SCK Frequency				2.1		1.0	MHz
t$_{RI}$	Input Rise Time				2.0		2.0	µs
t$_{FI}$	Input Fall Time				2.0		2.0	µs
t$_{CLH}$	Clock High Time		(Note 6)	190		410		ns
t$_{CLL}$	Clock Low Time		(Note 6)	190		410		ns
t$_{CSH}$	Min. $\overline{CS}$ High Time		(Note 7)	240		500		ns
t$_{CSS}$	$\overline{CS}$ Setup Time			240		500		ns
t$_{DIS}$	Data Setup Time			100		100		ns
t$_{HDS}$	$\overline{HOLD}$ Setup Time			90		500		ns
t$_{CSN}$	$\overline{CS}$ Hold Time			240		500		ns
t$_{DIN}$	Data Hold Time			100		100		ns
t$_{HDN}$	$\overline{HOLD}$ Hold Time			90		240		ns
t$_{PD}$	Output Delay from Clock Low		C$_L$ = 200 pF		240		240	ns
t$_{DH}$	Output Hold Time			0		0		ns
t$_{LZ}$	$\overline{HOLD}$ Output Low Z				100		240	ns
t$_{DF}$	Output Disable Time		C$_L$ = 200 pF		250		500	ns
t$_{HZ}$	$\overline{HOLD}$ to Output Hi Z				100		240	ns
t$_{WP}$	Write Cycle Time		1-16 Bytes		10		10	ms

Capacitance T$_A$ = 25°C, f = 1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C$_{OUT}$	Output Capacitance	3	8	pF
C$_{IN}$	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	I$_{OL}$ = 10 µA, I$_{OH}$ = 10 µA
Input Pulse Levels	0.3V to 3.5V
Timing Measurement Reference Level	
Input	0.4V and 1.6V
Output	0.8V and 1.6V

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 6: Minimum Clock period. Specified minimum clock period for SCK frequency varies with temperature range. Extended temperature range ("E"), the minimum clock period is 476ns. In the automotive temperature range, the minimum clock period is 1000ns. For example, using the extended temperature range minimum, if t$_{CLL}$ = 190ns, the minimum t$_{CLH}$ is 286ns (190ns + 286ns = 476ns).

Note 7: $\overline{CS}$ must be brought high for a minimum of 250 ns (t$_{CSH}$) between consecutive instruction cycles.

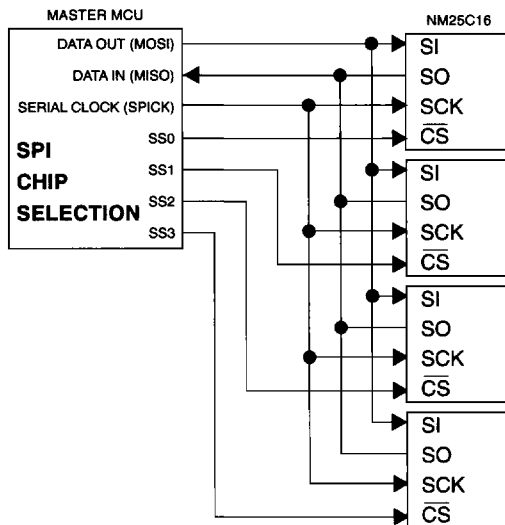**Note 8:** This parameter is periodically sampled and not 100% tested.

AC Test Conditions (Continued)

Synchronous Data Timing Diagram (Figure 1)
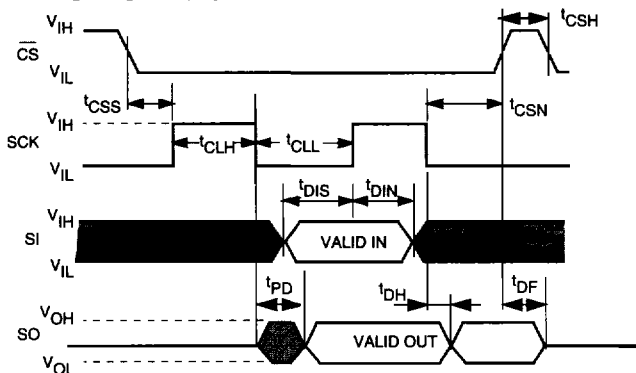
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SPI Serial Interface (Figure 2)

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Functional Description

MASTER: The device that generates the serial clock is designated as the master. The NM25C160 can never function as a master.

SLAVE: The NM25C160 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C160 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C160 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, HOLD may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. Pins SI, SCK and SO are at a high impedance state during $\overline{HOLD}$. See Figure 5.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C160, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 3.

Invalid Op-Code (Figure 3)

$\overline{CS}$

SI   INVALID CODE

SO
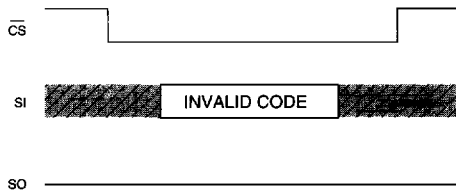
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Instruction Set (Table 1)

Instruction Name	Instruction Format	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

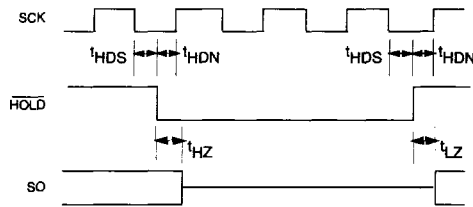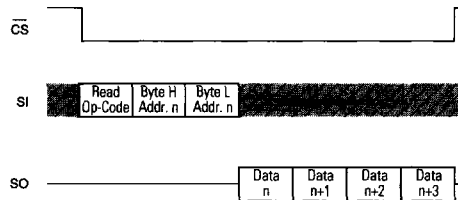## Functional Description (Continued)

SPI Protocol (Figure 4)
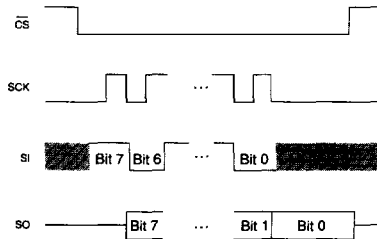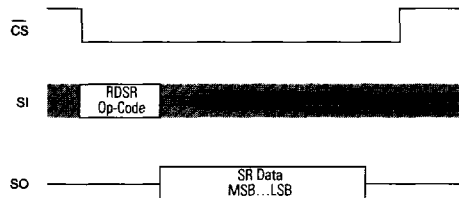

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HOLD Timing (Figure 5)

DS012402-6

Read Sequence (Figure 6)

DS012402-8

Read Status (Figure 7)

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Functional Description (Continued)

READ SEQUENCE: (One or More Bytes): Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the high order address byte (A10–A8), and the low order address byte (A7–A0). The leading three bits in the high order address byte will be ignored. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (7FFF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

Status Register Format (Table 2)

| Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See Figure 7.

Block Write Protection Levels (Table 3)

| Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	600-7FF
2	1	0	400-7FF
3	1	1	000-7FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. See Figure 8.

Write Enable (Figure 8)

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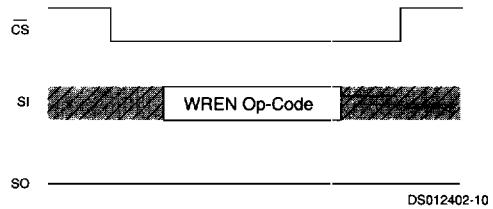
WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

Write Disable (Figure 9)

DS012402-11
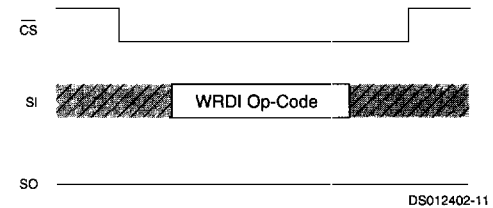
WRITE SEQUENCE: To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the high order address byte (A10-A8) and the low order address byte (A7-A0). The leading five bits in the high order address byte will be ignored. The address is followed by the data (D7–D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C160 is capable of a 16 byte PAGE WRITE operation. After receipt of each byte of data the four low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 16 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.
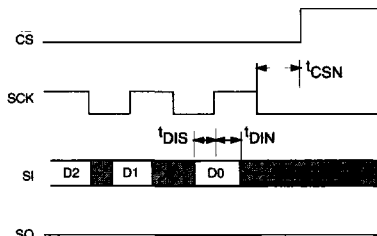
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication.
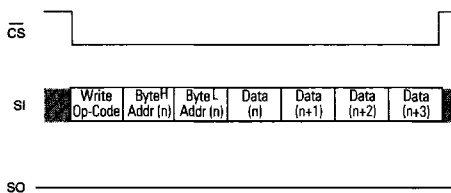
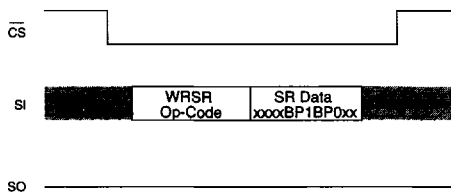# Functional Description (Continued)

Write Sequence (Figure 10)

CS

tCSN

SCK

tDIS tDIN

SI | D2 | D1 | D0 |

SO

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Start Write Condition (Figure 11)

CS

SI | Write Op-Code | ByteH Addr (n) | ByteL Addr (n) | Data (n) | Data (n+1) | Data (n+2) | Data (n+3) |

SO

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Write Status Register (Figure 12)

CS

SI | WRSR Op-Code | SR Data xxxxBP1BP0xx |

SO

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Start WRSR Condition (Figure 13)

CS

tCSN

SCK

tDIS tDIN

SI | BP0 |

SO
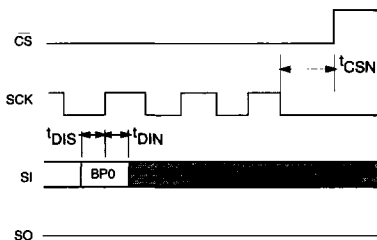
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WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.