MP100L EasyPower™

Offline Inductor-Less Regulator For Low Power Application

DESCRIPTION

The MP100L is a compact, inductor-less, good-efficiency, off-line regulator. It steps down the AC line voltage to an adjustable DC output. It is a simple solution to provide a bias voltage to ICs in off-line applications. Its integrated smart-control system uses AC line power only when necessary, thus minimizing device losses to achieve good efficiency. This device can help system designs meet new standby power specifications.

The MP100L provides various protections, such as Thermal Shutdown (TSD), VD Over Voltage Protection (OVP), VD Shrot to GND Protection, Over Load Protection (OLP), Short Circuit Protection (SCP).

The MP100L is available in SOIC8E package.

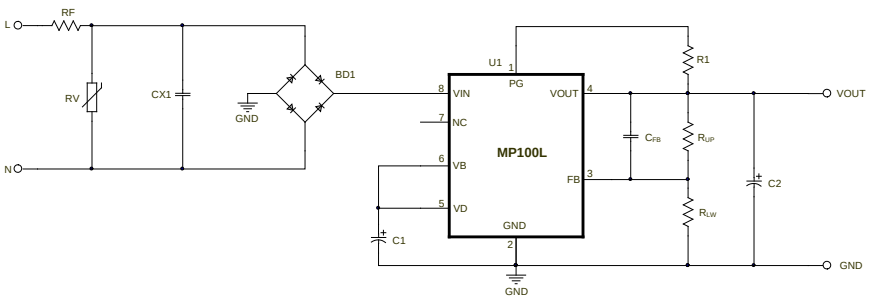
FEATURES

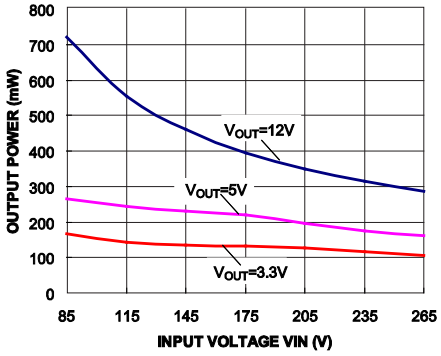
- Universal AC Input (85VAC-to-305VAC)
- Inductor-Less
- Less than 100mW Standby Power
- Good EMI
- Low BOM Cost
- Smart Control to Maximum Efficiency
- Adjustable Output Voltage from 1.5V to 15V
- Good Line and Load Regulation
- Thermal Shutdown Protection
- Short-Circuit Protection
- Provide Power-Good Signal

APPLICATIONS

- Wall Switches and Dimmers
- AC/DC Power Supply for Wireless System, like ZigBee,Z-Wave
- Standby Power for General Off-Line Applications

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP100LGN	SOIC-8 EP	MP100L

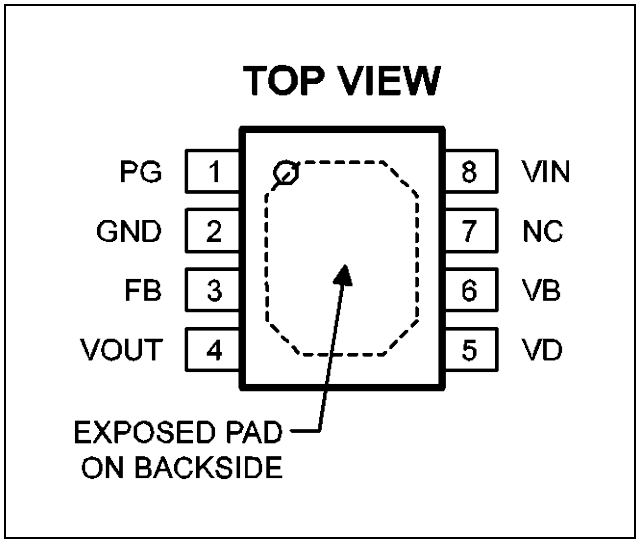
* For Tape & Reel, add suffix –Z (e.g. MP100LGN–Z);

TOP MARKING

MP100L
LLLLLLLL
MPSYWW

MP: MPS prefix:
100L: first four digits of the part number;
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -1V to 700V
VOUT ..... -0.3V to 28 V
VB..... -0.3V to 35V
FB..... -0.3V to 6.5V
PG ..... -0.3V to 14V
Continuous Power Dissipation (T_A = +25°C) **(2)**
SOIC-8 EP.....2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

50/60HZ AC RMS Voltage ..... 85V to 305V
VB..... 8V to 30V
Operating Junction Temp. (T_J) . -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC-8 EP……..50	10	°C/W	

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

C_{VD} = 4.7μF/50V, C_{OUT} =2.2μF/50V, T_J = -40°C~+125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN Section						
Input Voltage	V_{IN}	T_J=25°C	700			V
		T_J=-40°C ~ +125 °C	650			V
Input Supply Current (Quiescent)	IIN_{QC}	V_{IN} = 95V down to 90V & VD=30V, No Load		20	40	μA
Input Voltage Threshold (Fast)	VIN_{THF}	V_{IN} Rising	70	86	95	V
Input Voltage Slow Threshold	VIN_{THS}	V_{IN} Rising	31	34	37	V
Input Voltage Slow Threshold Hysteresis	$VIN_{THS-HYS}$			2.5		V
MOSFET ON Resistance	R_{ON}	I_{IN}=400mA,VB=5V		9.5		Ω
Input Current Rise Time	$IIN_{RISERATE}$			140	200	μs/Amp
Input Current Fall Time	$IIN_{FALLRATE}$			130	180	μs/Amp
VD Section						
VD peak voltage limit(OVP)	VD_{PKLMT}		19	21	23	V
VD Under Voltage Lock Out	VD_{UVLO}		6.2	7.0	7.7	V
VD Output Enable Threshold	VD_{THOUT}		13.2	15.4	17.5	V
Active Bleeder ON	VD_{BLDON}		12.2	14.4	16.5	V
Active Bleeder ON Hysteresis	$VD_{BLDON-HYS}$			1.3		V
Active Bleeder Current	ID_{BLD}		180	270	360	μA
VOUT Section						
VOUT Regulated Voltage	VOUT	VD=30V, I_{OUT}=40mA	11.5	12	12.5	V
Output Current Limit	$IOUT_{LMT}$		120	220	320	mA
Line Regulation[5]		VD=15V to 30V, I_{OUT}=100μA		0.05	0.1	%
Load Regulation[6]		VD=30V, I_{OUT}=100μA to 40mA		0.1	0.3	%
Dropout Voltage[7]	V_{DROP}	I_{OUT}=40mA	0.45	0.75	1.05	V
Ground Pin Current	I_G	I_{OUT}=40mA	0.95	1.1	1.25	mA
PSRR[8]	$\lvert PSRR \rvert$	f=10Hz to 50kHz,VD=20V, C_{VD}=1μF,C_{OUT}=4.7μF		>60		dB
FB Section						
Reference Voltage	VFB_{REF}		1.204	1.235	1.266	V
PG Section						
Power Good Pull Down Current	IPG		2			mA
Power Good Threshold	VPG_{TH}		1	1.12	1.24	V
Power Good Hysteresis	VPG_{TH-HYS}			85		mV
Power Good Delay	TPG_{DELAY}		180	245	310	μs

ELECTRICAL CHARACTERISTICS

C_{VD} = 4.7μF/50V, C_{OUT} =2.2μF/50V, T_j = -40°C~+125°C, unless otherwise noted.

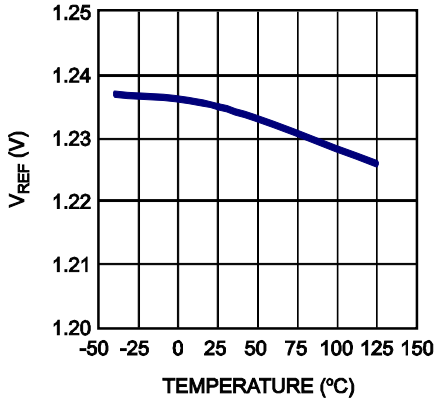
Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}			160		ºC
Thermal Shutdown Threshold Hysteresis	T_{SD-HYS}			20		ºC

Notes:

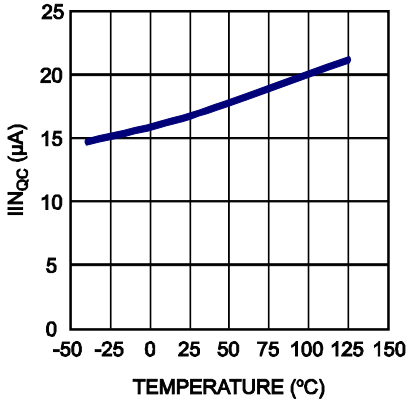
5) Line Regulation = (VOUT@VB=30V,100uA Load – VOUT@VB=15V,100uA Load) /12V*100.
6) Load Regulation = (VOUT@VB=30V,40mA Load – VOUT@VB=30V,100uA Load)/12V*100.
7) The drop out voltage is defined as VD-VOUT.
8) Guarantee by design.

TYPICAL CHARACTERISTICS

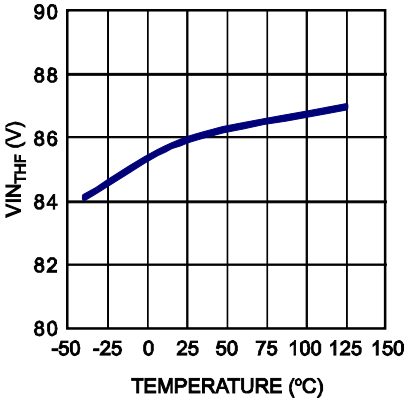
Reference Voltage vs.Temperature



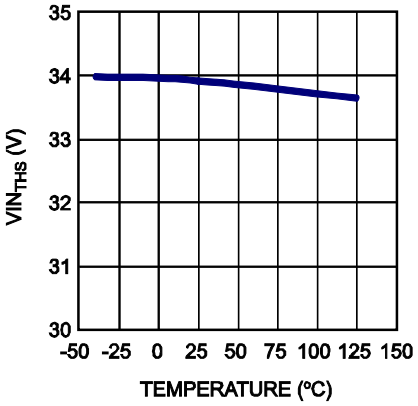
Input Supply Quiescent Current vs.Temperature



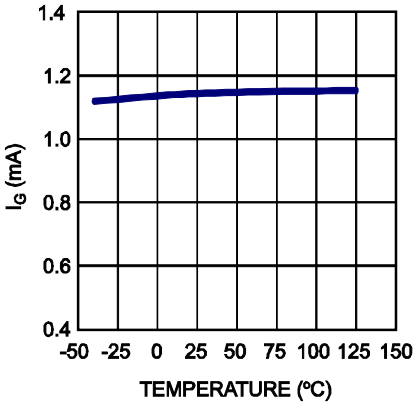
Input Voltage Fast Threshold vs.Temperature



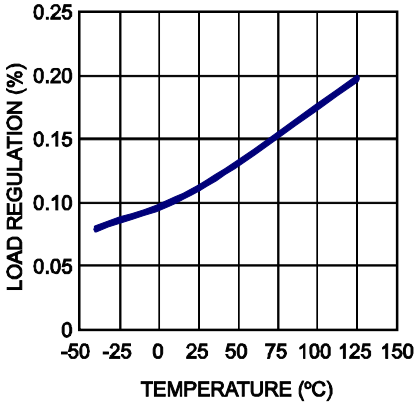
Input Voltage Slow Threshold vs.Temperature



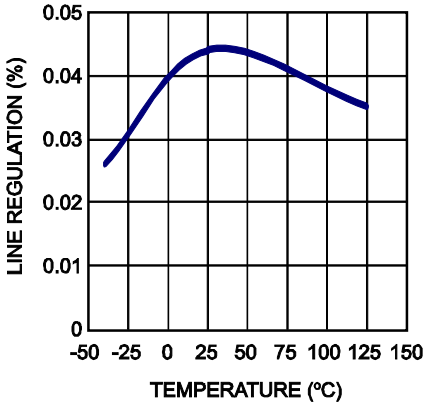
Ground Pin Current vs. Temperature



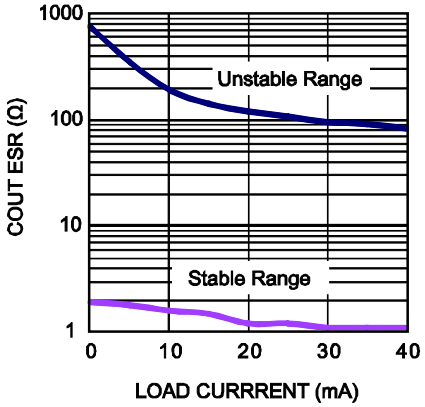
Load Regulation vs. Temperature



Line Regulation vs. Temperature

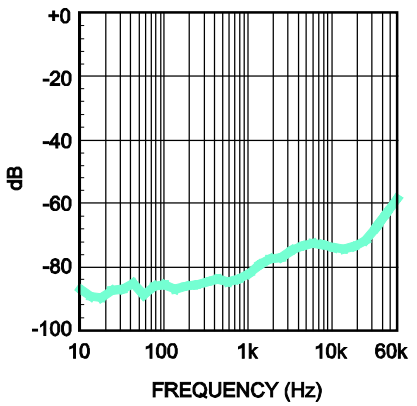


Region of Stable C_{OUT} ESR vs.Load Current



PSRR Test

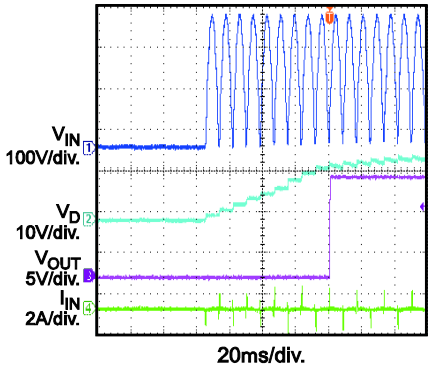
V_D=20V,V_{OUT}=5V,
I_{OUT}=0mA, C_{VD}=1µF, C_{OUT}=4.7µF



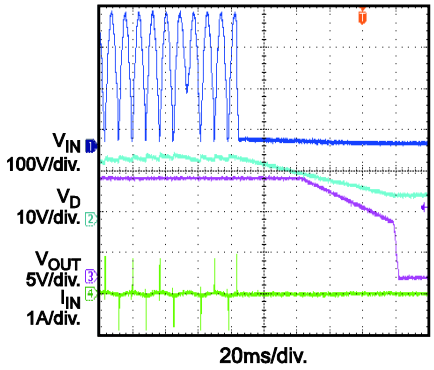
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN}=230VAC, V_{OUT}=12V, I_{OUT}=20mA, C_{VD}=220μF/35V, T_A=+25°C, unless otherwise noted.

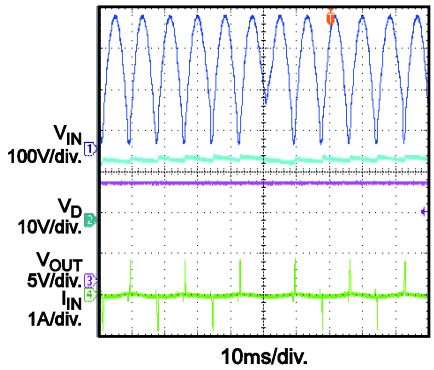
Input Power Start Up



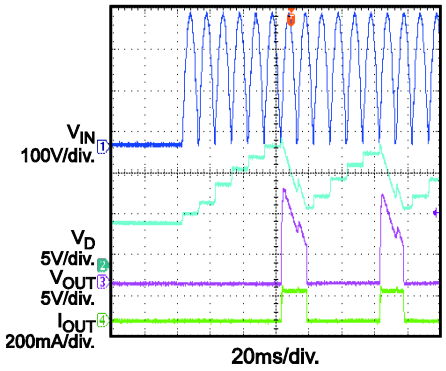
Input Power Shut Down



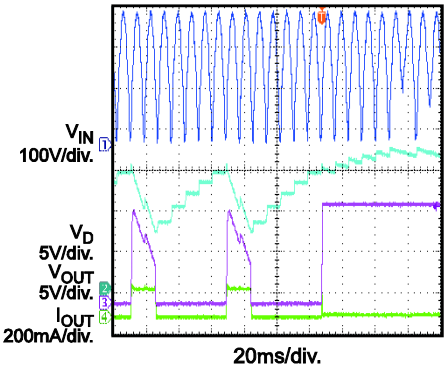
Steady State



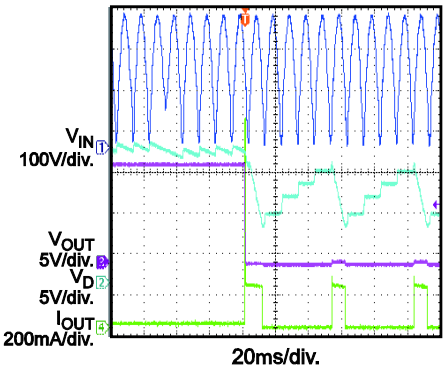
Over Load Protection Entry



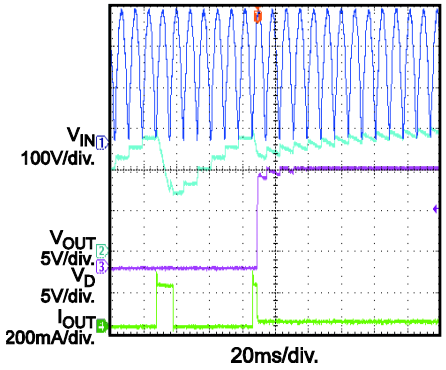
Over Load Protection Recovery



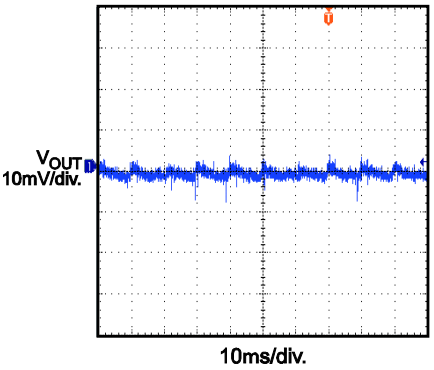
Short Circuit Protection Entry



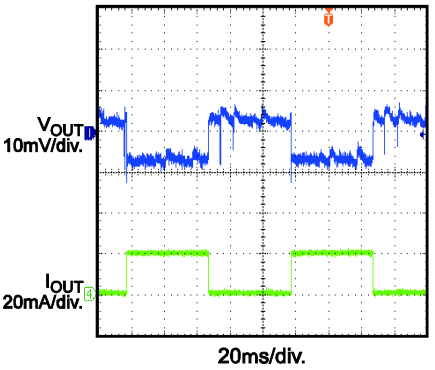
Short Circuit Protection Recovery



Output Ripple



Load Transient



PIN FUNCTIONS

SOIC-8 EP Pin #	Name	Description
1	PG	Power Good. Requires an external pull-up resistor because it is an open drain. When VOUT reaches 80% of its normal output voltage, PG goes high after a 245μs delay.
2	GND	Ground.
3	FB	Output Voltage Feedback. Connect to a capacitor to VOUT to improve low dropout stability. Internally voltage divider set the output to be 12V. Connect to the tap of a resistor divider to adjust the output voltage.
4	VOUT	Output Voltage.
5	VD	Connect a cap from this pin to GND to store energy for the low drop-out stage.
6	VB	Connect with VD directly.
7	NC	Not Connected.
8	VIN	Voltage Input Supply. Providing energy when the voltage falls within the charging window.
Expose pad		Connect to a large copper surface connected to GND to enhance thermal dissipation.

BLOCK DIAGRAM

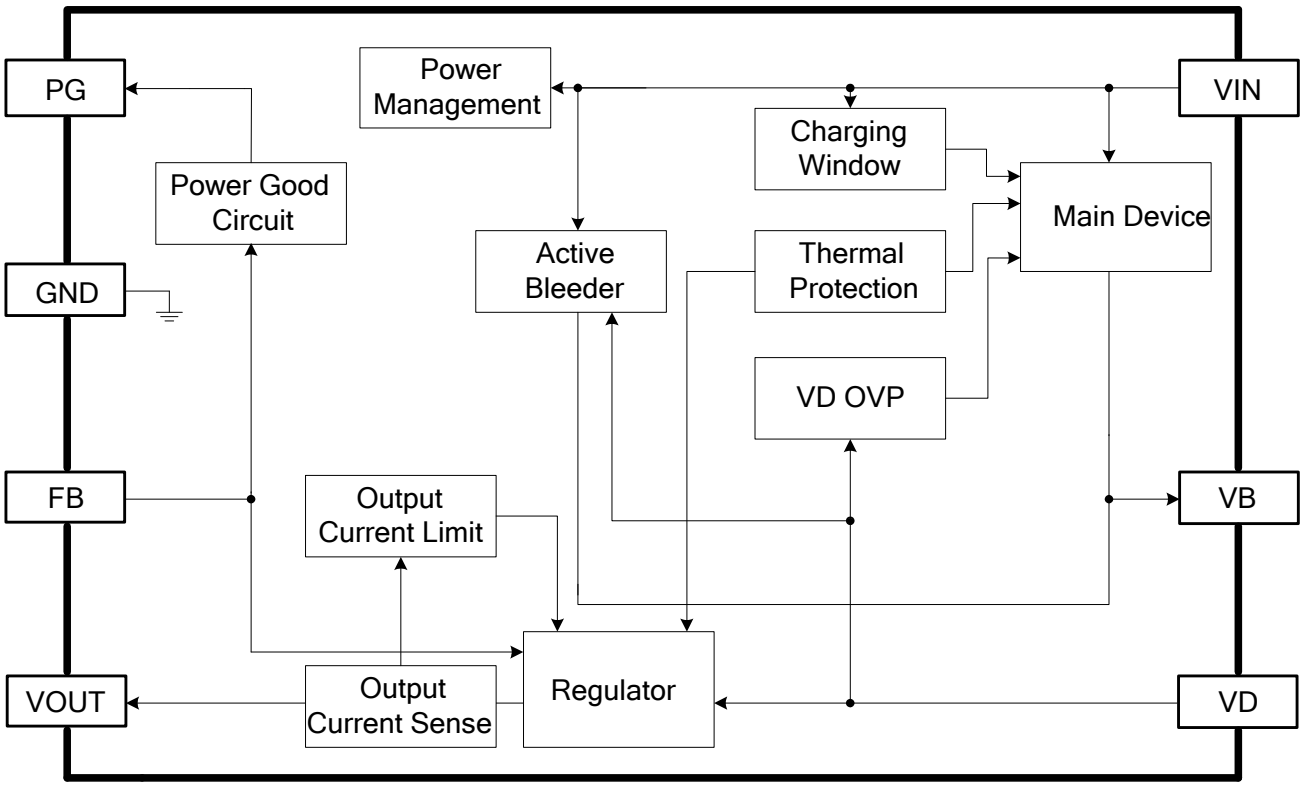


Figure 1: Functional Block Diagram

OPERATION

MP100L employs a smart inductor-less regulator design (patent pending) to charge the VD capacitor (C1 in Typical Application Section) from the offline AC input, and then to deliver the stored energy to the load with a stable output voltage. When VIN is less than its 34V threshold, VD can be charged up by up to 1A input current. An internal LDO regulates VOUT to 12V and can supply up to 20mA load when VIN is between 85VAC and 305VAC. The proprietary design allows the universal AC input to efficiently power the IC directly.

Startup

During the startup, the internal switch connected between VIN and VB turns on when the input voltage is within its charging window (typically below 34V), thus gradually charging the VD voltage. The LDO will not resume with a soft-start until the VD voltage reaches 15.4V.

Internal NMOS Switching

The EMI performance of MP100L greatly relates to the turn-on and turn-off speed of internal switch connected between VIN and VB. To pass related emissions standards with only an X-cap connected to the input ports, the MP100L slowly turns off the internal switch when the VIN voltage reaches 34V, and turns the switch off immediately when VIN reaches 86V during the turn-off period. During the turn-on period, when VIN falls to 31.5V, the internal switch turns on slowly. The turn on and turn off slope is130us/A.

To avoid mis-triggered of internal switch when there is noise or inductive kick in input voltage, when Vin falls to 31.5V, the internal switch starts to turn on, and there will be 110us blanking to filer the noise of VIN to let the switch on, when VIN rises to 34V, the internal switch starts to turn off, and there is 300us blanking to prevent the switch return on.

Active Bleeder Circuit

The input voltage may not enter its charging window during normal operation due to parasitic capacitance from VIN to GND. An active bleeder circuit is enabled to pull down the VIN voltage whenever the VD voltage falls below 14.4V to guarantee that the output gets enough energy from the input ports. In addition, when the power supply shuts down, the active bleeder circuit discharges the energy stored in the parasitic capacitor to ensure that the circuit can restart easily.

VD Over-Voltage Protection

The VD capacitor provides energy for the output load. If the voltage of VD exceeds 21V, the internal switch between VIN and VB turns off immediately to prevent the VD voltage from rising too high, which can damage the LDO stage.

VD Short-Circuit Protection

The output current is limited to 220mA if the output is shorted to ground, which also decreases the VD voltage. When VD drops below 7.0V, LDO turns off. The input voltage then gradually charges VD up to 15.4V to enable the LDO. When LDO turns on, the output current drops the VD voltage to 7.0V again. This process will continue until the output short condition ceases.

VOUT Over-Current Protection

The VD and VOUT voltages will drop simultaneously if the output current exceeds its normal value. When the VD voltage falls to 7.0V, the second stage LDO shuts down immediately. Then the input voltage charges VD to 15.4V to enable the LDO. Due to the output current limit circuit, the maximum current is typically limited to 220mA.

Thermal Shutdown Protection

Accurate temperature protection prevents the chip from operating at exceedingly high temperature. When the silicon die temperature exceeds 160°C, the whole chip shuts down. When the temperature falls below its lower threshold of 140°C, the chip is enabled again.

Power-Good

The MP100L integrates a power-good circuit to signal that the output meets the controller IC's requirements. It is an open drain structure and requires a pull-up resistor to VOUT. During start up, the VOUT voltage rises smoothly. When it reaches 80% of its normal value, the power-good signal goes high after a 245µs delay to indicate a normal output.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set to 12V by internal large feedback resistors. Adjust VOUT by choosing appropriate external feedback resistors. The recommended output voltage is between 1.5V and 15V. Defining the upper and lower feedback resistors as R_{UP} and R_{LW} respectively (refer to the picture in Typical Application section):

$$R_{UP} = R_{LW} \times (\frac{VOUT}{1.235} - 1)$$

For the external resistors to dominate over the internal resistors, select relatively small values of R_{UP} and R_{LW} compared to the internal resistors. However, to minimize the load consumption, avoid very small external resistors. For most applications, choose R_{LW}=10.2kΩ. To accurately set the output voltage, select an R_{UP} that can counter the internal upper-feedback resistor value of 1MΩ. The table below lists typical resistor values for different output voltages:

Table 1: Resistors Selecting vs. Output Voltage Setting

VOUT(V)	R_{UP}(kΩ)	R_{LW}(kΩ)
1.5	2.21(1%)	10.2(1%)
3.3	16.9(1%)	10.2(1%)
5	30.9(1%)	10.2(1%)
15	121(1%)	10.2(1%)

SELECTION OF VD CAPACITOR

The bypass capacitor on the VD pin needs to be sufficiently large to provide a stable current. Calculate the capacitance (in μF) based on the following equation:

$$C_{VD} = \frac{I_{load} \times \tau_s}{V_{ripple}}$$

Where, I_{load} is the output current (mA); τ_s is based on the type of input rectifier—for example, τ_s is 20ms for a half-wave rectifier, and 10ms for a full-bridge rectifier, V_{ripple} is the voltage ripple on the VD capacitor—normally the ripple is limited to 2V to 3V. For best results, use a small ceramic capacitor and a large aluminum capacitor in parallel.

Output Power Capability

The maximum input power to the VD capacitor is limited by the fixed charging window. Considering the LDO power loss, the MP100L has a limited maximum output power.

The following factors influence the MP100L's maximum output power: the input rectifier (full bridge or half-wave); the VD capacitor connected between VD and GND; the output voltage; and the MP100L's temperature-rise requirement, which is relative to the different application environments.

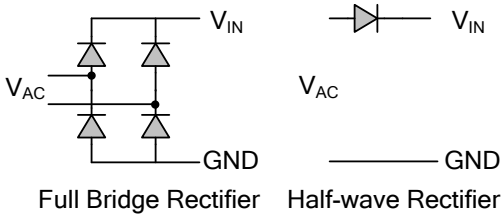


Figure depicts the relationship between the maximum output power and the VIN voltage when the output voltage is 12V, 5V and 3.3V, respectively. The plots account for full bridge rectifiers, the temperature rise of MP100L is less than 60°C on the test board in 25°C room temperature test in the open frame.

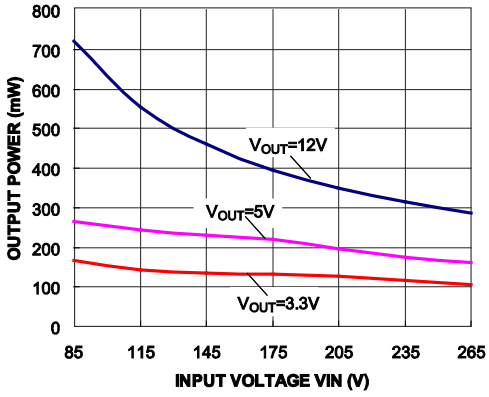


Figure 2: Output Power vs. Input Voltage

Line Transformer

MP100L can work well when connected to AC line or programmable AC source. But when using an isolation transformer or a variable transformer as source, because of the high inductance of the

transformer (usually in the mH's), high voltage spikes occur when MP100L turns off the internal switch connected between VIN and VB, which may damage the IC. An X- capacitor must be installed before the rectifier to guarantee the reliability of the system.

EMI

To meet the relevant conducted emissions standard, the internal switch connected between VIN and VB is designed to turn on and off slowly. By adopting this method, a small X cap connected between the input ports will pass EMI with enough margins. For general application, 220nF X-capacitor between the input ports is enough to pass EMI, which will make the whole system compact.

Surge

From its working principle, mP100L is working just when VIN falls into its charging window, so when surges happen at this moment, then a lot of energy will be by MP100L due to the slow turn off process. To protect it from damage, a fast turn off threshold (typically it is 86V) of VIN is set specially to shut down the switch connected between VIN and VB quickly.

Since there is no bulk capacitor to absorb AC line transients, MOV should be used to protect the IC to survive the transient test. Besides the value of fuse resistor will also affect the surge result, the larger value used, the better to facilitate to pass the surge test, but the more power consumption will be caused, in the meanwhile, the larger value used, the easier to trigger its fast turn off threshold, 20 ohm fuse resistor is recommended in real application.

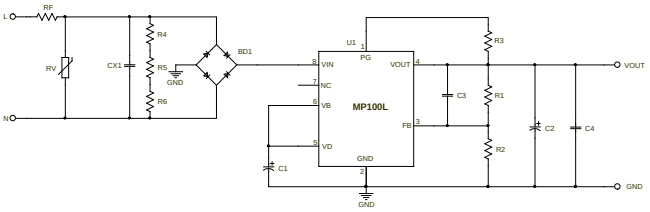
Besides, the thermal pad must be connected to the GND for better surge performance.

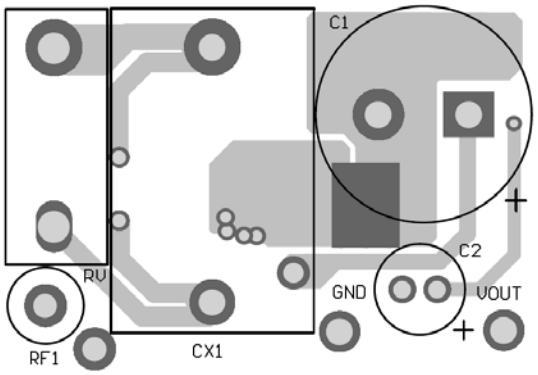
PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

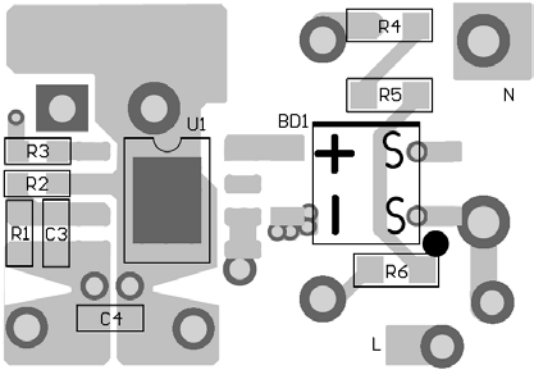
If change is necessary, please follow these guidelines and take Figure 3 for reference.

1) Minimize the loop area formed by positive output of rectifier, VIN,VB and GND.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Output capacitor should be put close to the output terminal.
4) Connect the exposed pad with GND to a large copper area to improve thermal performance and long-term reliability





Top Layer



Bottom Layer

Figure 2: PCB Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	85V to 265V
V_{OUT}	12V
I_{OUT}	20mA

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device application, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

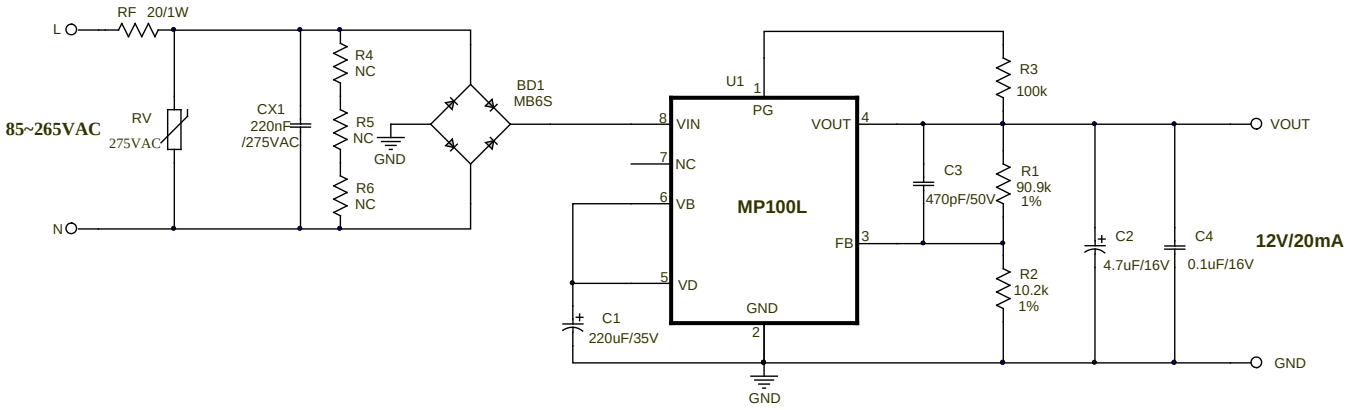
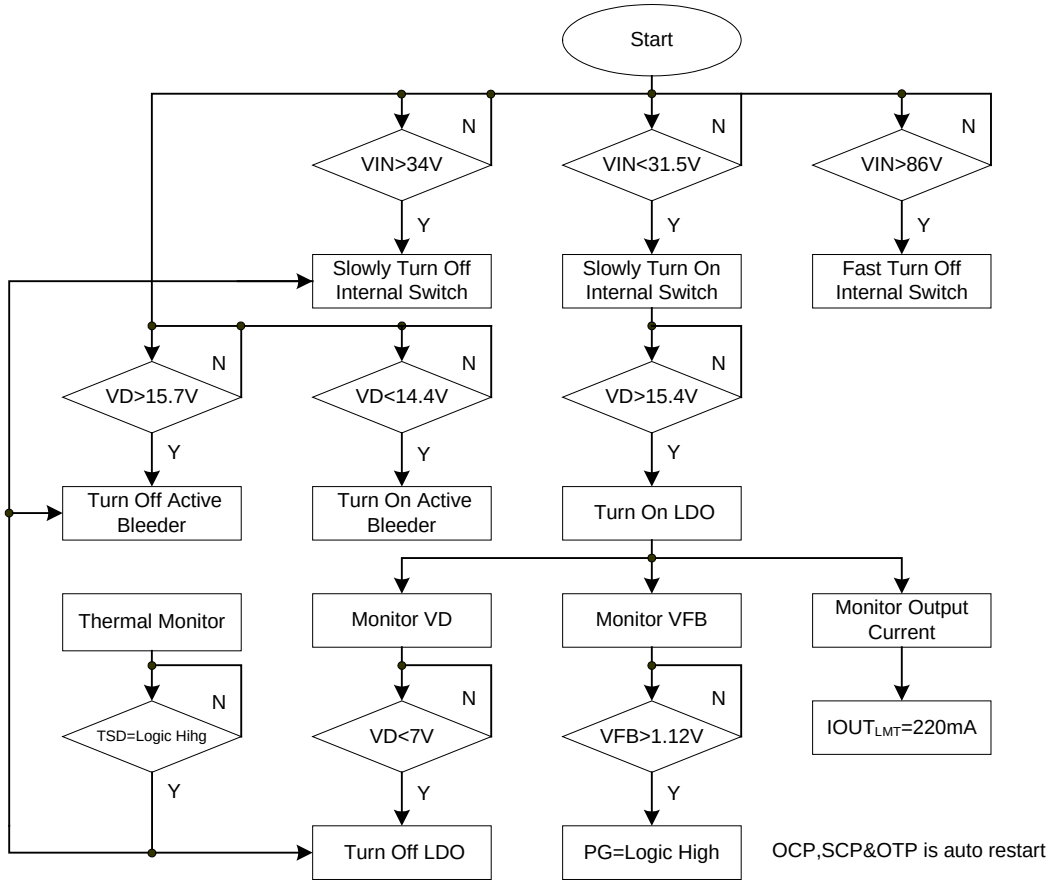
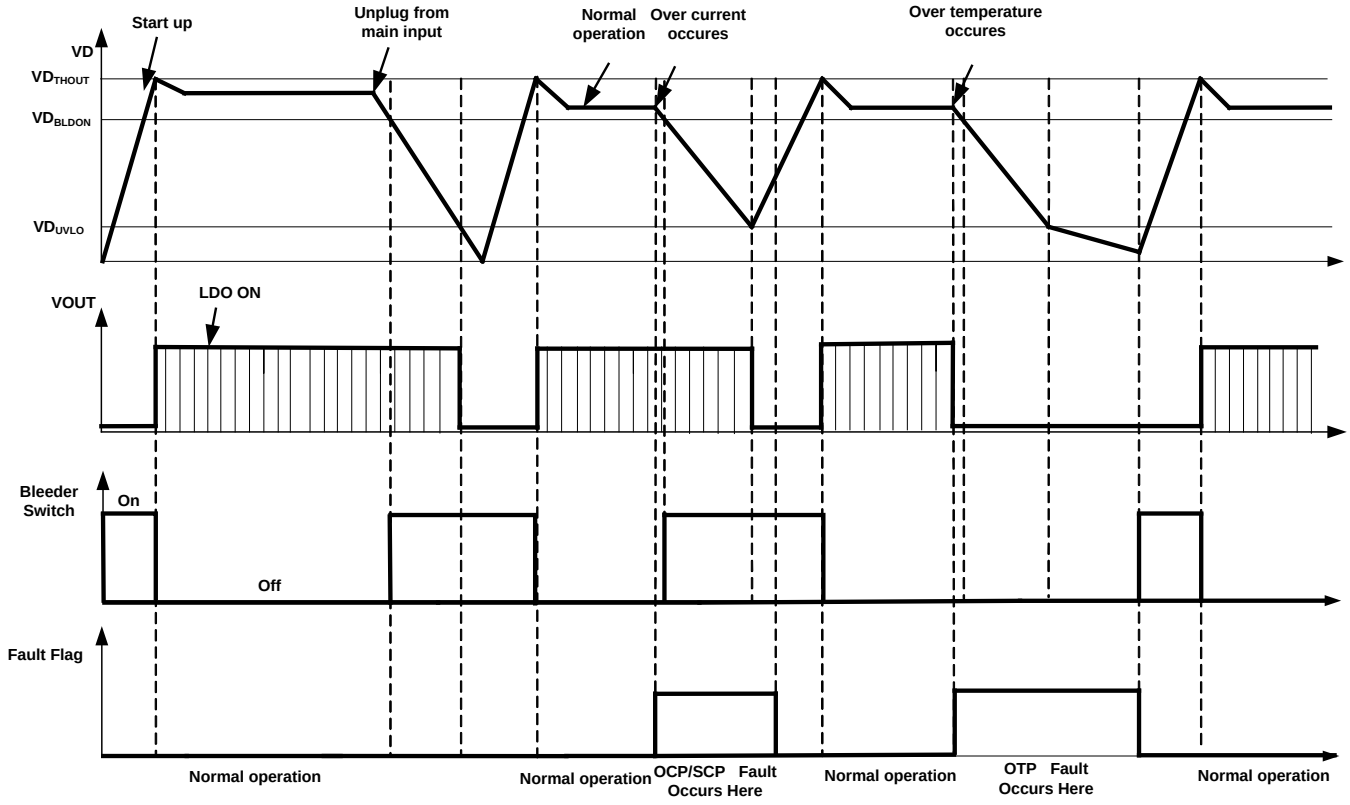


Figure 4: Typical Application

FLOW CHART

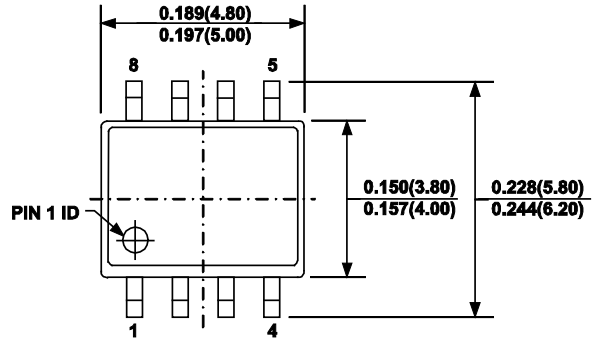


SIGNAL EVOLUTION IN THE PRESENCE OF FAULTS

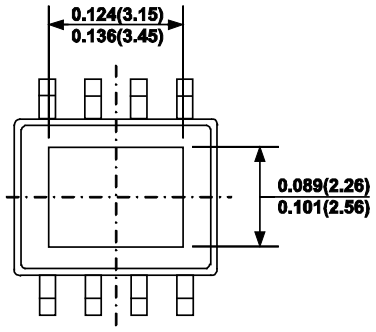


PACKAGE INFORMATION

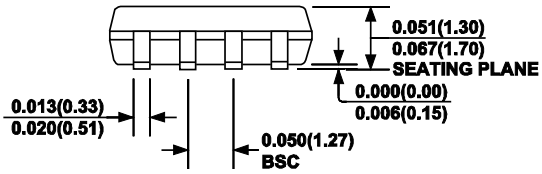
SOIC8E



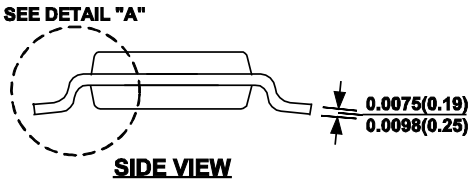
TOP VIEW



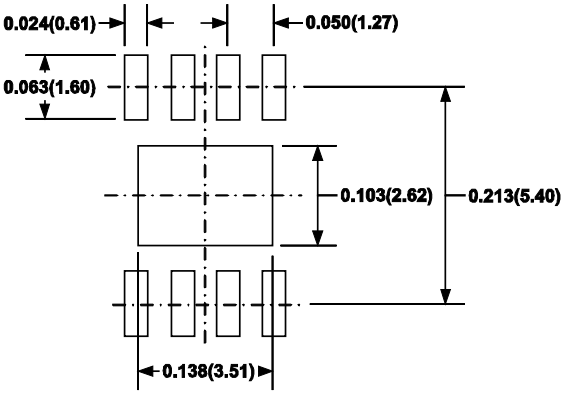
BOTTOM VIEW



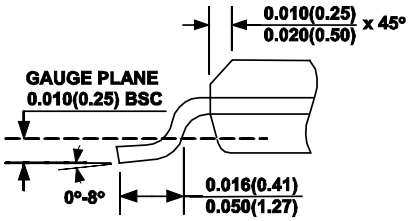
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.