Rockchip RK860 Datasheet

Revision History

Date	Revision	Description
2022-11-17	1.6	Update the Typical Application and layout information
2022-11-01	1.5	Update the ordering and layout information
2022-04-27	1.4	1，Modify layout recommendation description 2，Modify the dimension information
2022-02-22	1.3	1，Modify Package Thermal Characteristics description 2，Modify more description of the output current capability
2021-10-11	1.2	Update RK860-3 description
2021-06-23	1.1	Update Thermal Management information
2021-05-11	1.0	Initial release

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Chapter 1 Introduction

1.1 Overview

The RK860 is a high efficiency 2.4MHz synchronous step down DC/DC regulator IC capable of delivering up to 7A output current. It can operate over a wide input voltage range from 2.7V to 5.5V. And, it integrates a main switch and a synchronous switch with both very low $R_{DS\ (ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.7125V to 1.5V with 12.5mV/step or 0. 5V to 1.5V with 6.25mV/step through I^2C interface.
The RK860 is in a space saving, low profile WLCSP 1.65mm*2.05mm-20 package.

1.2 Feature

- Input voltage range：2.7V-5.5V
- 2.4MHz switching frequency minimizes the external components
- Typical 70uA quiescent current when VIN=3.8V and Temp=25℃
- Low $R_{Ds(ON)}$ for internal switches(PFET/NFET):24mohm/16ohm @ VIN=3.8V
- Programmable output voltage:0.7125V to 1.5V with 12.5mV/step or 0.5V to 1.5V with 6.25mV/step
- 7A continuous output current capability
- Capable for 0.24uH inductor and 22uF*2 ceramic capacitor
- Hic-cup mode protection for hard short condition
- Integrate inner protection：Cycle by cycle OCP and VIN-OVP/UVLO/DIE-TSD
- RoHS compliant and Halogen free
- Compact package: WLCSP 1.65*2.05-20

1.3 Typical Application Diagrams

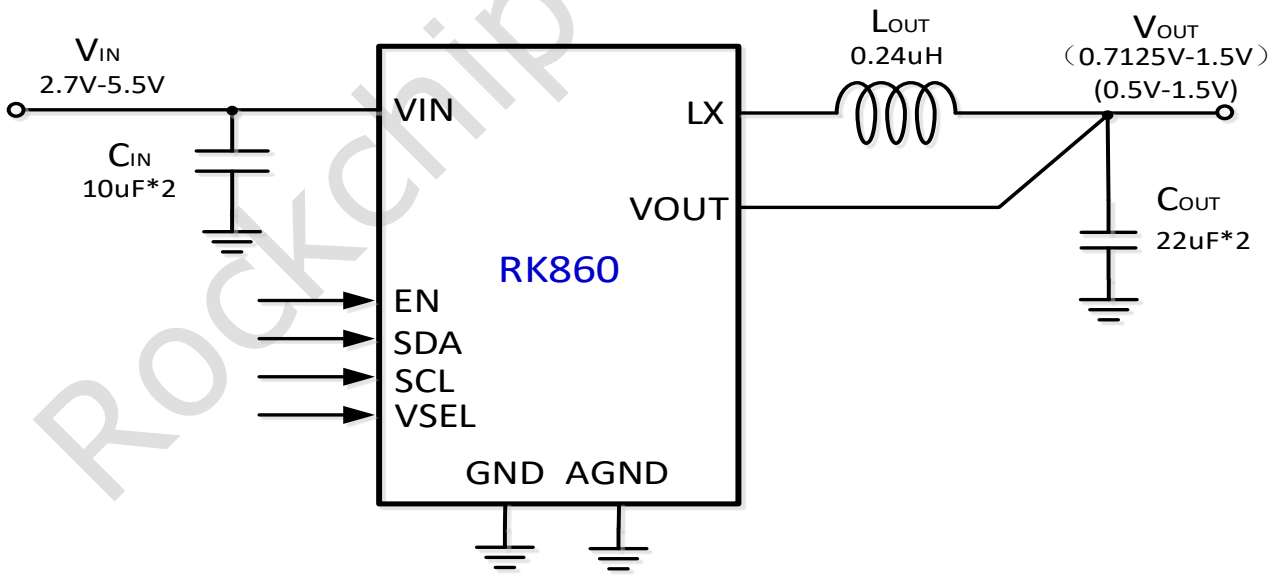


Fig. 1-1 RK860 General Application

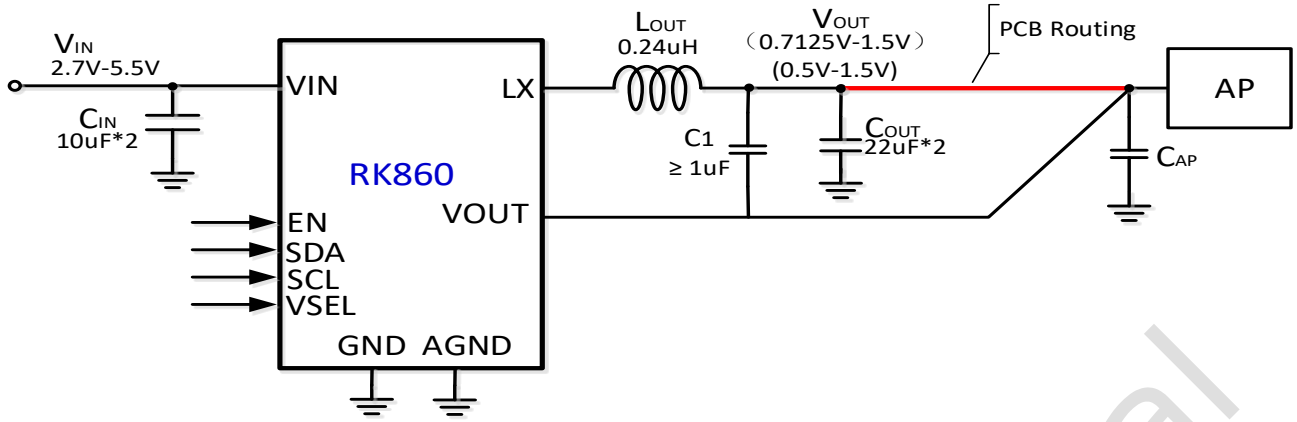


Fig. 1-2 RK860 Application In Particular Cases

1.4 Pin Assignment

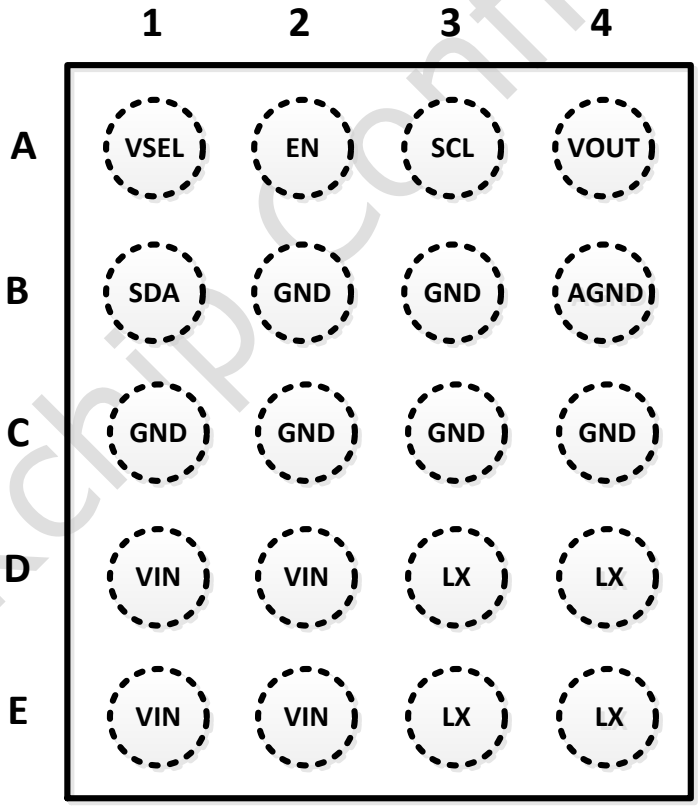


Fig. 1-3 Pin Assignment（Top view）

1.5 Pinout Number Order

Number	Name	Function	I/O
D1,D2,E1,E2	VIN	Power input pins. These pins must be decoupled to ground by 2 10uF ceramic capacitor as input filter at least.The input	Power

Number	Name	Function	I/O
		capacitor should be placed as close as possible between VIN and GND pins.	
D3,D4,E3,E4	LX	Switching node pin. Connect these pins to switching node of inductor.	Output
B2,B3,C1,C2,C3,C4	GND	Power ground pins.	Ground
B4	AGND	Analog ground pin.	
A1	VSEL	Voltage select pin. When this pin is low, V_{OUT} is set by the VSEL0 register. When this pin is high, V_{OUT} is set by the VSEL1 register.	Input
A2	EN	Enable control pin. Active high. Do not leave it floating.	Input
A3	SCL	I^2C interface clock line.	Input
B1	SDA	I^2C interface Bi-directional Data line. (Open darin)	I/O
A4	VOUT	Sense pin for output. Connect to the output capacitor side	Output

Chapter 2 Electrical Characteristics

Note 1.Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The device is not guaranteed to function outside its operating conditions.

2.1 Absolute Maximum Ratings (Note 1)

Parameter	Value	Units
Voltage range on pins VIN：	6.0	V
Voltage range on other pins	VIN+0.6	V
Continuous power dissipation, PD @ TA=25'C,WCSP4*5-20	0.5	W
Junction temperature range, T_J	-40~150	℃
Lead Temperature(soldering 10 sec),T_{SOLDER}	260	℃
Storage temperature range, T_S	-65~150	℃
ESD Susceptibility		
ESD HBM	2000	V
ESD CDM	1000	V

2.2 Recommended Operating Conditions (Note 2)

Parameter	Symbol	value	Units
Supply Input Voltage	V_{IN}	2.7~5.5	V
Output Voltage	V_{OUT}	0.5~1.5	V
Inductor	L	0.22~0.47	uH
Input Capacitor	C_{IN}	>10	uF
Output Capacitor	C_{OUT}	44~88	uF
Junction temperature range	T_j	-40~125	℃
Ambient temperature range	T_a	-40~85	℃

2.3 Electrical Characteristics

(With typical application circuit shown in below part, V_{IN}=3.8V, V_{OUT}=1.0V, L=0.24uH, C_{OUT}=22uF*2, T_A=25℃ unless otherwise specified.)

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
The UVLO threshold voltage of VIN	V_{IN_UVLO}	Vin rising		2.55	2.65	V
The UVLO Hysteresis voltage of VIN	$V_{IN\_UVLO\_HYS}$	Vin falling		150		mV
The OVP threshold voltage of VIN	V_{IN_OV}	Vin rising		6		V
The OVP Hysteresis voltage of VIN	$V_{IN\_OV\_HYS}$	Vin falling		200		mV
Quiescent Current	Iq	No switching, vfb=105%Vref.		70		uA
Shutdown current	Isd	EN=L		0.1		uA
Software shutdown current	Isd_soft	EN=H, BUCK_EN=L		25		uA
Internal soft-start time	Tss	Vout=1.0V， from BUCK_EN rising edge to Vout>92%.		260		uS

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Oscillator Frequency	Fclk	PWM mode or FPWM mode	2.2	2.4	2.6	MHz
Discharge resistance	Rdisc	EN=L/BUCK_EN=0		150		Ω
Input logic high threshold of signal (EN/VSEL)	VIH		1.1			V
	VIL				0.4	V
Input logic high threshold of signal (SDA/SCL)	VIH		1.26			V
	VIL				0.54	V
Vout Accuracy when FPWM	V_{REG1}(The output Voltage error)	Forced PWM, VOUT=1.0V	-0.6		+0.6	%
Vout Accuracy when PFM	V_{REG2}(The output Voltage error)	Auto PFM, VOUT=1.0V	-1.5		1.5	%
PMOS RDS(ON)	RDS(ON)P	VIN PIN to LX PIN,VIN=3.8V		24		mΩ
NMOS RDS(ON)	RDS(ON)N	LX PIN to GND PIN,VIN=3.8V		16		mΩ
Maximum current of PMOS	Ipeak		8.5			A
Maximum current of NMOS	Ivalley		7.0			A
Thermal shutdown temperature	TSD	Rising TSD threshold		150		℃
Thermal shutdown Hysteresis	TSD_HYS			25		℃

Chapter 3 Chip Version Description

DIE-ID	I2C-ADDR (7-bit)	Vout Range/V	Default Vout/V	STEP/ mV	DIE_ID
RK860-0	40H	0.7125-1.5	1.0	12.5	0X8
RK860-1	41H	0.7125-1.5	1.0	12.5	0X8
RK860-2	42H	0.5-1.5	0.8	6.25	0XA
RK860-3	43H	0.5-1.5	0.8	6.25	0XA

Chapter 4 Register Description

VSEL0_A
Address: (0x00)

Bit	Attr	Reset Value	Description
7	RW	0x1	BUCK_EN0: Software buck enable. 1:enable BUCK work; 0:shut off BUCK (When external EN pin is low. The regulator is off. When external EN pin is high, BUCK_EN bit takes precedent.)
6	RW	0x0	MODE0: 0=Allow auto-PFM mode during light load 1=Forced PWM mode
5:0	RW	0x17	NSEL0 : 12.5mV/step (just for DIE_ID=0X8) 000000=0.7125V; 000001=0.7250V; 000010=0.7375V; ..... 010111=1.0000V; ..... 111111=1.5V;

VSEL1_A
Address: (0x01)

Bit	Attr	Reset Value	Description
7	RW	0x1	BUCK_EN1: Software buck enable. 1:enable BUCK-LOOP work; 0:shut off BUCK-LOOP (When external EN pin is low. The regulator is off. When external EN pin is high, BUCK_EN bit takes precedent.)
6	RW	0x0	MODE1: 0=Allow auto-PFM mode during light load 1=Forced PWM mode

Bit	Attr	Reset Value	Description
5:0	RW	0x17	NSEL1 : 12.5mV/step (just for DIE_ID=0X8) 000000=0.7125V; 000001=0.7250V; 000010=0.7375V; ..... 010111=1.0000V; ..... 111111=1.5V;

Control_Register
Address: (0x02)

Bit	Attr	Reset Value	Description
7	RW	0x1	Output Discharge: 0=discharge resistor is disabled. 1=discharge resistor is enabled.
6:4	RW	0x0	Slew Rate: Set the slew rate for positive voltage transitions. 000 = 10mV/0.15us 001 = 10mV/0.3us 010 = 10mV/0.6us 011 = 10mV/1.2us 100 = 10mV/2.4us 101 = 10mV/4.8us 110 = 10mV/9.6us 111 = 10mV/19.2us
3:0	RW	0x0	Always reads back 0. RESET：Setting to 1 resets all registers to default values.

ID1 Register
Address: (0x03)

Bit	Attr	Reset Value	Description
7:5	R	0x4	VENDOR: IC vendor Rockchip code.
4	R	0x0	Reserved: Always reads back 0.
3:0	R	0x8/0xA	DIE_ID: 0x8: Output Voltage from 0.7125V to 1.5V with 12.5mV/step 0xA: Output Voltage from 0.5V to 1.5V with 6.25mV/step

ID2 Register
Address: (0x04)

Bit	Attr	Reset Value	Description
7:4	R	0x0	Reserved: Always reads back 0.
3:0	R	NA	NA

PGOOD Register
Address: (0x05)

Bit	Attr	Reset Value	Description
7	R	0x0	PGOOD: 1:Buck is enabled and soft-start is completed. （Vout>92% normal set-value） 0：Vout is abnormal
6	R	0x0	TSD: thermal shut down BUCK. 1: Tdie>150'C，0: Tdie<125'C
5	R	0x0	IOVP: Over input voltage shut-off protection state. 1: VIN>6V, 0: VIN<5.8V
4	R	0x0	UVLO: Input voltage under-lock state. 1: VIN<2.4V，0:VIN>2.55V
3:0	R	0x0	Reserved

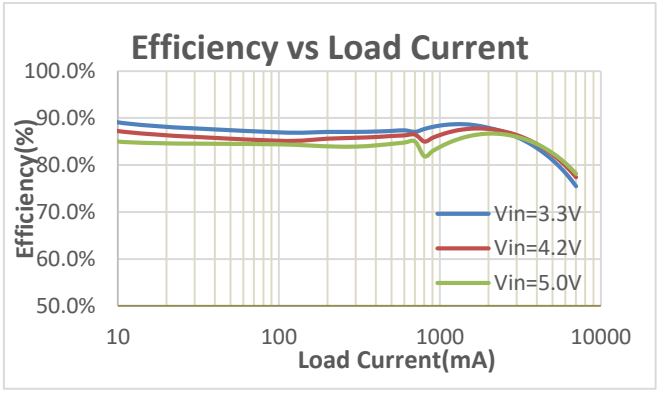
VSEL0_B Register
Address: (0x06)

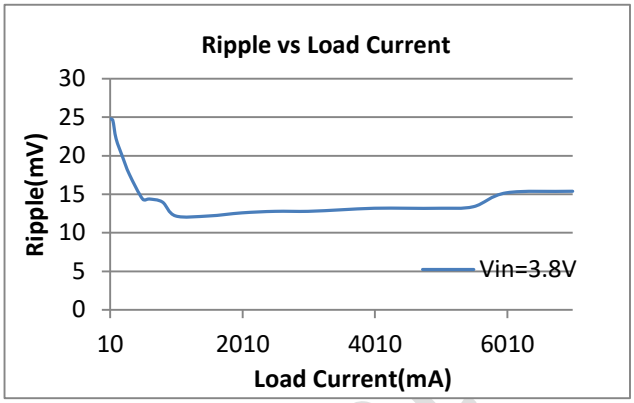
Bit	Attr	Reset Value	Description
7:0	R/W	0x30	NSEL0: when VSEL=L option just for DIE_ID=0XA 00,000,000 = 0.5V 00,000,001 = 0.50625V 00,000,010 = 0.51250V …… 00,110,000 = 0.8V …… 10,100,000 =1.5V >10,100,000=1.5V

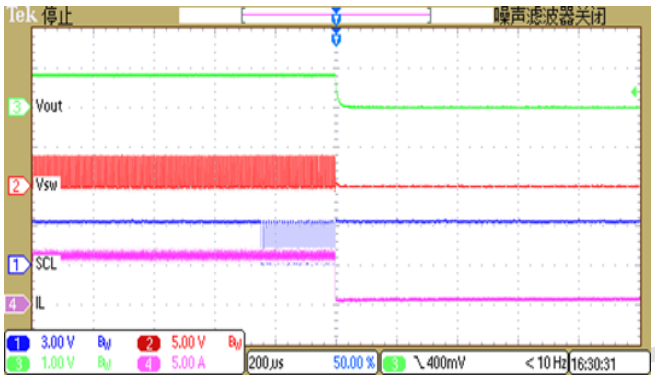
VSEL1_B Register
Address: (0x07)

Bit	Attr	Reset Value	Description
7:0	R/W	0x30	NSEL1: when VSEL=H option just for DIE_ID=0XA 00,000,000 = 0.5V 00,000,001 = 0.50625V 00,000,010 = 0.51250V …… 00,110,000 = 0.8V …… 10,100,000 =1.5V >10,100,000=1.5V

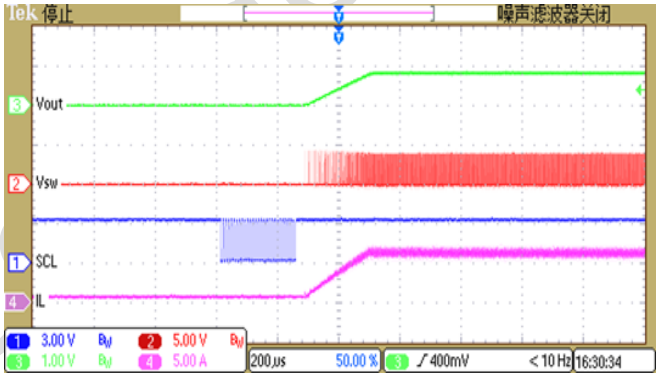
Chapter 5 Typical Performance Characteristics



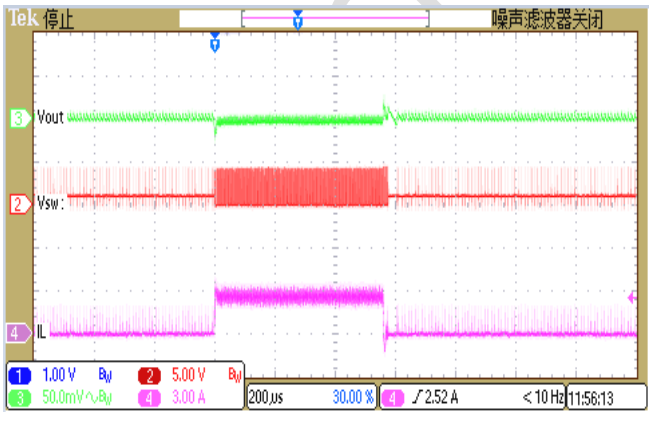




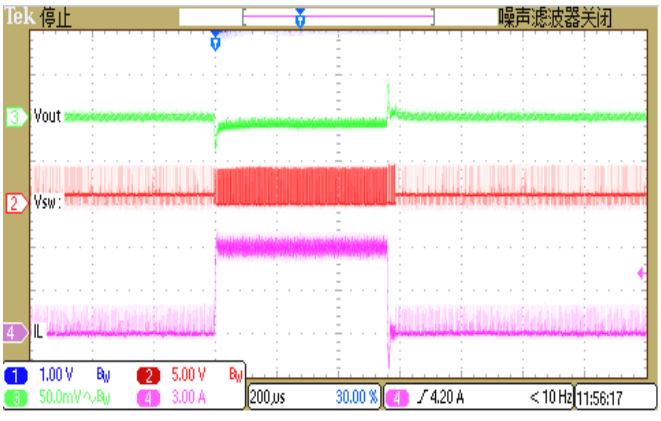
Shutdown from Enable
(Vin=3.8V,Vout=0.8V,Iout=7A)



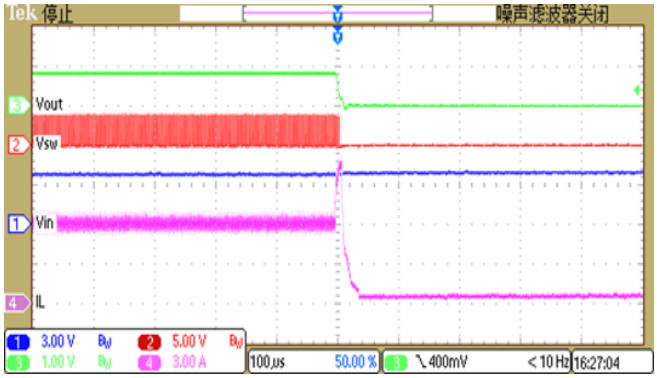
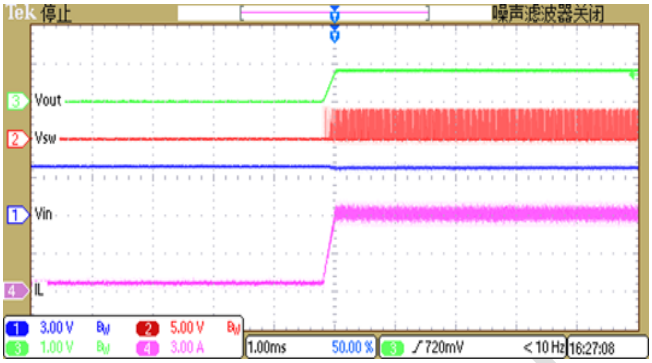
Startup from Enable
(Vin=3.8V,Vout=0.8V,Iout=7A)



Load Transient
(Vin=3.8V,Vout=0.8V,Iout=0.05~3A,1A/uS)



Load Transient
(Vin=3.8V,Vout=0.8V,Iout=0.1~7A,1A/uS)

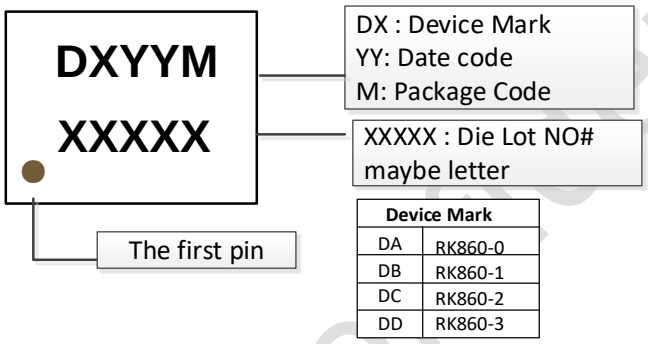
	
Short Circuit Protection (Vin=3.8V,Vout=0.8V,Iout=7A~short)	Short Circuit Protection (Vin=3.8V,Vout=0.8V,Iout=short~7A)

Chapter 6 Package information

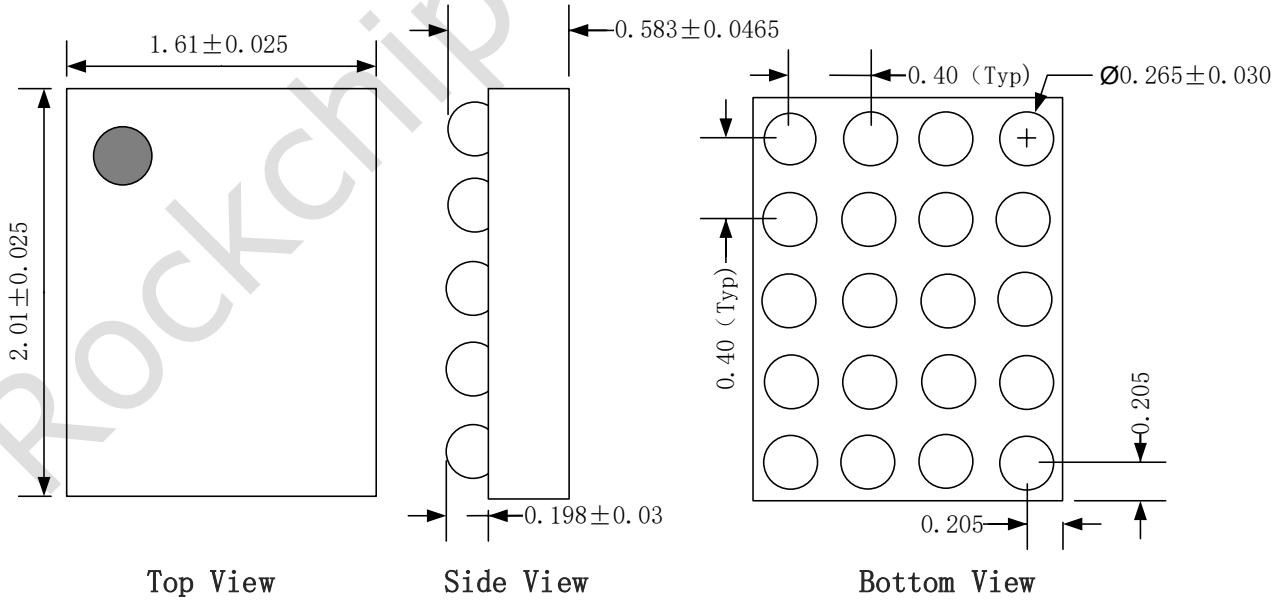
6.1 Ordering information

Orderable Device	Device Mark	RoHS status	Package	Package Qty
RK860-0	D0	RoHS pass	WLCSP20(pitch 0.4mm)	5000 pcs/tape
RK860-1	D1	RoHS pass	WLCSP20(pitch 0.4mm)	5000 pcs/tape
RK860-2	D2	RoHS pass	WLCSP20(pitch 0.4mm)	5000 pcs/tape
RK860-3	D3	RoHS pass	WLCSP20(pitch 0.4mm)	5000 pcs/tape

6.2 Top Marking



6.3 Dimension



Notes: All dimension in MM

Fig. 6-1 WLCSP20（Pitch is 0.4mm）

Note:

- *Coplanarity applies to leads, corner leads and die attach pad.*
- *Dimension ϕb applies to metalized terminal and is measured between 0.15mm and 0.30mm*

from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension ϕb should not be measure in that radius area.

- *0.15mm of dimension ϕb is recommended in PCB layout.*

6.4 Layout recommendation

Reasonable PCB wiring directly affects the performance of the chip. So we need to pay special attention to the following points in PCB Layout.

- The capacitor of the CIN must be placed close enough to the pins. To minimize input interference as much as possible.
- The PCB copper area associated with SW pin must be minimized to reduce SW noise.
- The feedback trace connecting COUT to the VOUT pin must not be adjacent to the SW node on the PCB layout to minimize the noise coupling to VOUT pin.
- To ensure adequate heat dissipation and interference shielding, we must maximize the copper area of the PCB connected to GND. It is recommended to set reasonable through via underneath the ground pad to improve the performance of the circuit loop.
- The GND PAD of the CIN , COUT and Chip must be on the same side (or close enough).
- If your feedback circuit so long and the PCB layout must be follow Fig. 6-2 . The capacitor of the C1 must be placed close to the COUT. And the Pin of the VOUT must be connect from the capacitor of the CAP.

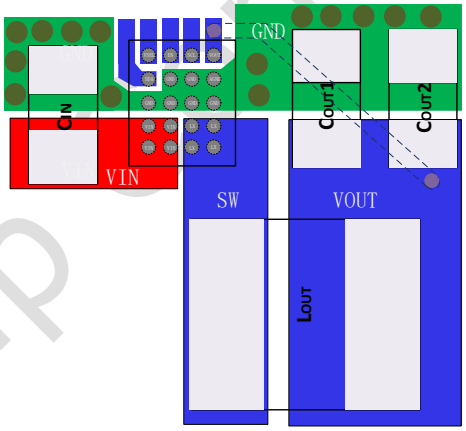


Fig. 6-3 General PCB Layout Suggestion

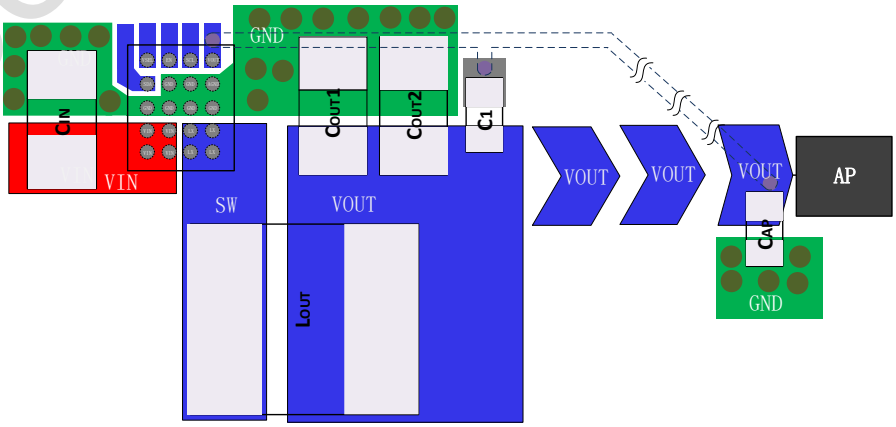


Fig. 6-4 PCB Layout Suggestion In Particular Cases

Chapter 7 Thermal Management

7.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK860 has to be below 150℃.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

7.2 Package Thermal Characteristics

Table 1-1 provides the thermal resistance characteristics for the package used on this device.

Table 7-1 Thermal Resistance Characteristics

PACKAGE (WLCSP 20)	Continuous power dissipation, PD @ TA=25'C,WCSP4*5-20(W)	θJA, 2-layer PCB Thermal resistance from junction to ambient $\boldsymbol{\theta_{JA}}$(℃/$\boldsymbol{W}$)	θJC, 2-layer PCB Thermal resistance from junction to component $\boldsymbol{\theta_{JC}}$(℃/$\boldsymbol{W}$)
RK860	0.5	64.44	17.76

Table 7-2 SnPb Eutectic Process-Classification Temperatures (TC)

Package Thickness	**Volume mm³ <350**	**Volume mm³ ⩾350**
<2.5 mm	235 ℃	220℃
⩾2.5 mm	220 ℃	220℃

Table 7-3 Pb-Free Process-Classification Temperatures (TC)

Package Thickness	**Volume mm³ <350**	**Volume mm³ 350-2000**	**Volume mm³ >2000**
<1.6 mm	260 ℃	260 ℃	260℃
1.6 mm-2.5 mm	260℃	250 ℃	245℃
>2.5 mm	250 ℃	245 ℃	245℃

Note 1:At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (TP) can exceed the values specified in Tables 1-2or 1-3. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Tables 4.2 and 1-4, whether or not Pb-free.

Note 5: SMD packages classified to a give moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112(rescinded),IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 7-4 Classification Reflow Profiles

Profile Feature	**Sn-Pb Eutectic Assembly**	**Pb-Free Assembly**
Preheat & Soak Temperature min (T smin) Temperature max(Tsmax) Time (Tsmin to Tsmax)(ts)	 100℃ 150℃ 60-120 seconds	 150℃ 200℃ 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3 ℃ /second max.	3 ℃ /second max.
Liquidous temperature (TL) Time at liquidous (tL)	183 ℃60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (Tp)*	See classification temp in Table 1-2	See classification temp in Table 1-3
Time(tp)* * within 5℃ of the specified classification temperature (Tc)	20** seconds	30** seconds
Average ramp-down rate (Tp to Tsmax)	6℃ /second max.	6 ℃ /second max.
Time 25 ℃ to peak temperature	6 minutes max.	8 minutes max.
*Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow(e.g.,ive-bug). If

parts are reflowed in other than the normal ive-bug assembly reflow orientation (i.e.,dead-bug), Tp shall be within ±2℃ of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to

achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly

profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 1-4.

For example, if Tc is 260 ℃and time Tp is 30 seconds, this means the following for the supplier and the user.

For a supplier. The peak temperature must be at least 260 ℃.The time above 255 C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 ℃. The time above 255 ℃C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of ,J-STD-020

JESD22-A112 (rescinded), IPC-SM-786(rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

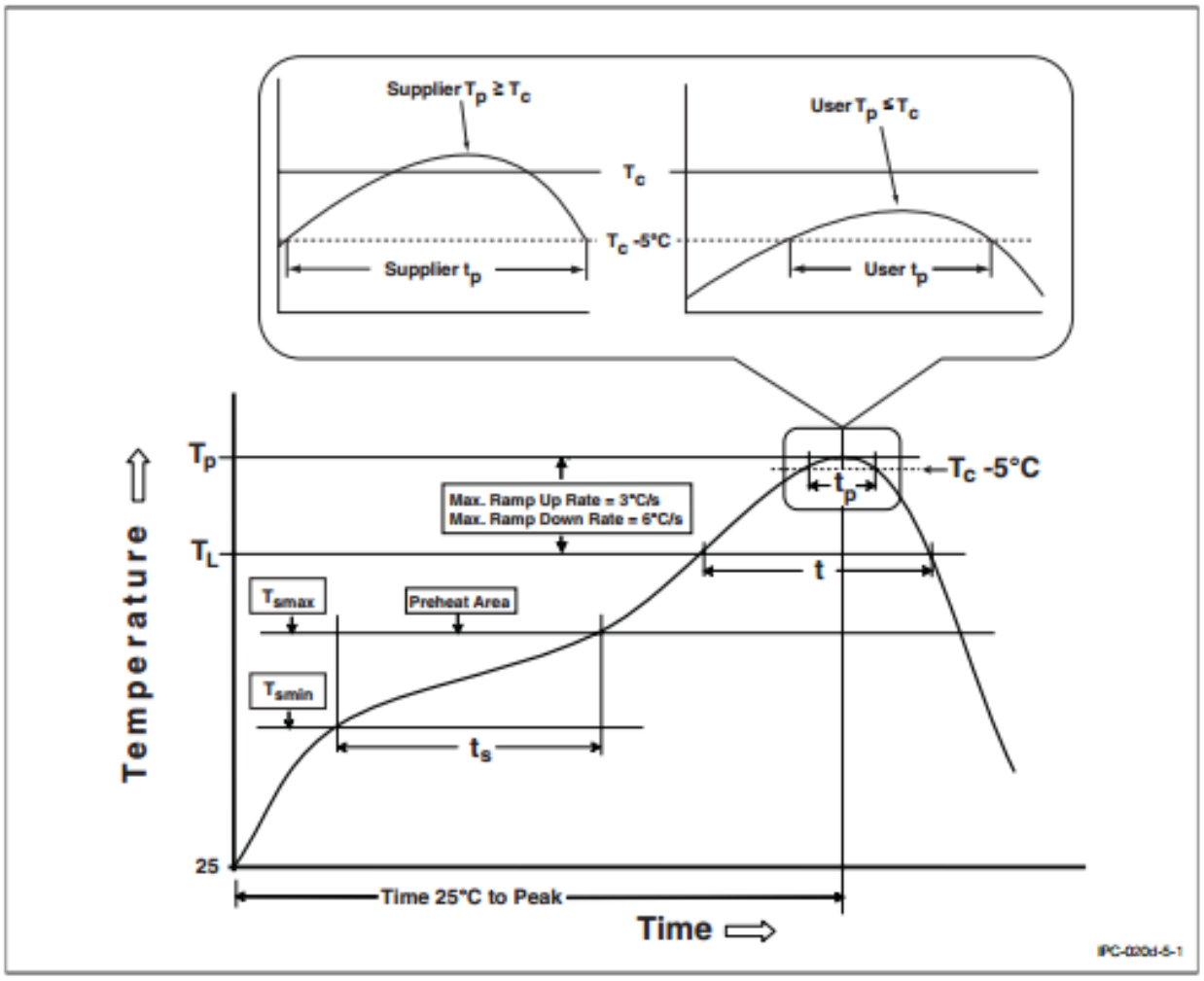


Figure 5-1 Classification Profile