8-Bit Serial-in, Parallel-out Shift Register

1 FEATURES

- **8-Bit Serial Input, Parallel Output Shift**
- **Power-Supply Range: 1.65V to 5.5V**
- **Low Power Consumption: 8μA(Max)**
- **Low Input Current: 1μA(Max)**
- **Gated Serial Data Input**
- **Asynchronous Master Reset**
- **Extended Temperature: -40°C to +125°C**

2 APPLICATIONS

- **IP Routers**
- **Programable Logic Controllers**
- **Enterprise and Communicatios**
- **Industrial**
- **Appliances**
- **LED Displays**
- **Output Expander**

3 DESCRIPTIONS

The RS164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (A and B), eight parallel data outputs (Q0 to Q7).

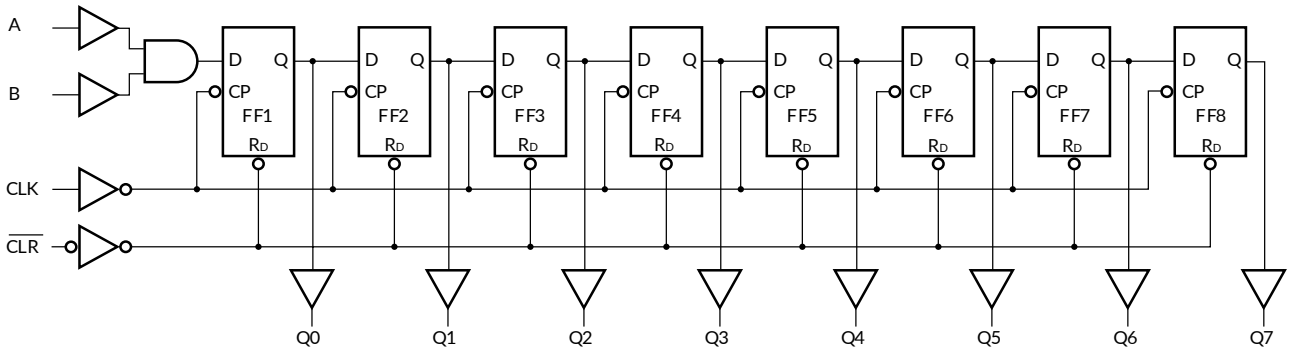
Data is entered serially through A or B and either input can be used as an active High enable for data entry through the other input. Data is shifted on the Low-to-High transitions of the clock (CLK) input. A Low on the master reset input ($\overline{CLR}$) clears the register and forces all outputs Low, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS164	SOIC-14(SOP14)	8.65mm×3.90mm
	TSSOP-14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram



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5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2023/08/28	Preliminary version completed
A.1	2023/09/01	1. Update Recommended Operating Conditions 2. Update ELECTRICAL CHARACTERISTICS 3. Update Switching Characteristics

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS164	RS164XP	-40°C ~+125°C	SOIC-14(SOP14)	RS164	MSL3	Tape and Reel,4000
	RS164XQ	-40°C ~+125°C	TSSOP-14	RS164	MSL3	Tape and Reel,4000

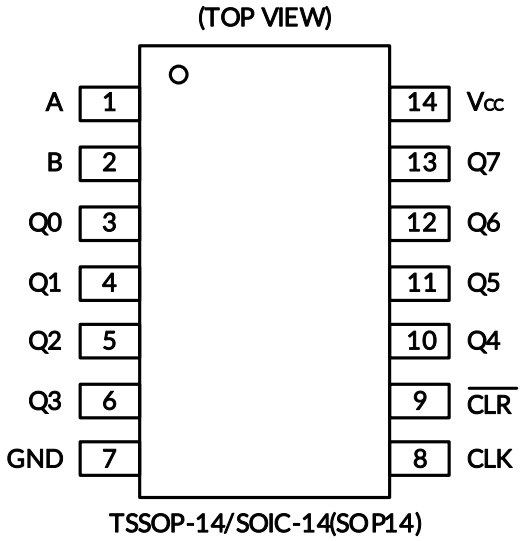
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 PIN CONFIGURATIONS



7.1 PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
TSSOP-14/SOIC-14			
1	A	I	Data input
2	B	I	Data input
3,4,5,6,10,11,12,13	Q0~Q7	O	Parallel data output
7	GND	G	Ground.
8	CLK	I	Clock input (Low-to-High, edge-triggered)
9	$\overline{CLR}$	I	Master reset (active Low)
14	V_{CC}	P	Supply voltage

(1) I=input, O=output, P=power, G=Ground.

7.2 Functional Table

Operating modes	Input				Output	
	$\overline{CLR}$	CLK	A	B	Q0	Q1 to Q7
Reset (Clear)	L	X	X	X	L	L to L
Shift	H	↑	I	I	L	q0 to q6
	H	↑	I	h	L	q0 to q6
	H	↑	h	I	L	q0 to q6
	H	↑	h	h	H	q0 to q6

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
I = Low voltage level one set-up time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced input one set-up time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{CC}	Supply Voltage Range		-0.5	6.5	V
I_{IK}	Input Clamp Current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output Clamp Current	V_O < -0.5V or V_O > V_{CC}+0.5V		±20	mA
I_O	Output Current	-0.5 V < V_O < V_{CC} + 0.5 V		±25	mA
I_{CC}	Supply Current			50	mA
I_{GND}	Ground Current		-50		mA
θ_{JA}	Package thermal impedance (2)	TSSOP-14		90	°C/W
		SOIC-14(SOP14)		105	
T_J	Junction Temperature (3)		-40	150	°C
T_{stg}	Storage Temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	
		Machine Model (MM), JESD22-A115C (2010)	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

Voltages are reference to GND(0V).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}		1.65		5.5	V
Input voltage	V_I		0		V_{CC}	V
Output voltage	V_O		0		V_{CC}	V
Input transition rise or fall rate(Δt/Δv)	Data inputs	V_{CC}=1.65V to 1.95V			20	ns/V
		V_{CC}=2.3V to 2.7V			20	
		V_{CC}=3V to 3.6V			10	
		V_{CC}=4.5V to 5.5V			5	
Operating temperature	T_A		-40		125	°C

8.4 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC}	TEMP	MIN(1)	TYP(2)	MAX(1)	UNIT
High-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V		FULL	0.7xV_{CCI}			V
		V_{CC}=2.3V to 2.7V			1.7			
		V_{CC}=3V to 3.6V			2			
		V_{CC}=4.5V to 5.5V			0.7xV_{CCI}			
Low-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		FULL			0.3xV_{CCI}	V
		V_{CC}=2.3V to 2.7V					0.7	
		V_{CC}=3V to 3.6V					0.8	
		V_{CC}=4.5V to 5.5V					0.3xV_{CCI}	
High-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}						
		I_O = -100 μA	1.65V to 5.5V	FULL	V_{CC}-0.1			V
		I_O = -4 mA	3V	FULL	1.2			
		I_O = -8 mA	3.3V		1.9			
		I_O = -10 mA	5.5V		3.8			
Low-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA	1.65V to 5.5V	FULL			0.1	V
		I_O = 4 mA	3V	FULL			0.45	
		I_O = 8 mA	3.3V				0.4	
		I_O = 10 mA	5.5V				0.55	
Input leakage Current	I_I	V_I=5.5V or GND	0V to 5.5V	FULL			±1	μA
Supply current	I_{CC}	V_I=5.5V or GND; I_O=0	1.65V to 5.5V	FULL			8	
Input capacitance	C_I			25°C		6		pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

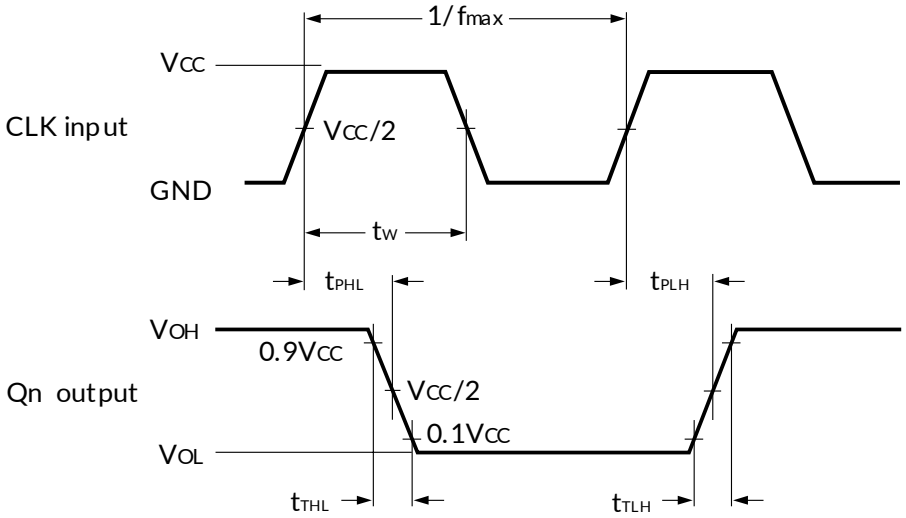
8.5 Switching Characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	25°C (1)			-40°C to +125°C (1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd} (2)	Propagation delay	CLK to Qn							
		V_{CC}=1.8V±0.15V		34				68	ns
		V_{CC}=2.5V±0.2V		24				48	
		V_{CC}=3.3V±0.3V		18				36	
		V_{CC}=5V±0.5V		14				28	
t_{PHL}	High to Low propagation delay	$\overline{CLR}$ to Qn							
		V_{CC}=1.8V±0.15V		24				48	ns
		V_{CC}=2.5V±0.2V		14				28	
		V_{CC}=3.3V±0.3V		10				20	
		V_{CC}=5V±0.5V		8				16	
t_t (3)	transition time	V_{CC}=1.65V		19				60	ns
		V_{CC}=4.5V		7				22	
		V_{CC}=5.5V		6				20	
t_w	Pulse width	CLK High or Low							
		V_{CC}=1.65V	110			110			ns
		V_{CC}=4.5V	22			22			
		V_{CC}=5.5V	19			19			
		CLR LOW							
		V_{CC}=1.65V	110			110			ns
		V_{CC}=4.5V	22			22			
		V_{CC}=5.5V	19			19			
t_{rec}	Recovery time	$\overline{CLR}$ to CLK							
		V_{CC}=1.65V	50			50			ns
		V_{CC}=4.5V	10			10			
		V_{CC}=5.5V	9			9			
t_{su}	Set-up time	A, and B to CLK							
		V_{CC}=1.65V	55			55			ns
		V_{CC}=4.5V	11			11			
		V_{CC}=5.5V	10			10			
t_h	Hold width	A, and B to CLK							
		V_{CC}=1.65V	3			3			ns
		V_{CC}=4.5V	3			3			
		V_{CC}=5.5V	3			3			
f_{max}	Maximum frequency	For CLK							
		V_{CC}=1.65V	4			4			MHz
		V_{CC}=4.5V	20			20			
		V_{CC}=5.5V	24			24			
C_{PD} (4)	Power dissipation capacitance	per package; V_I = GND to V_{CC}		115					pF

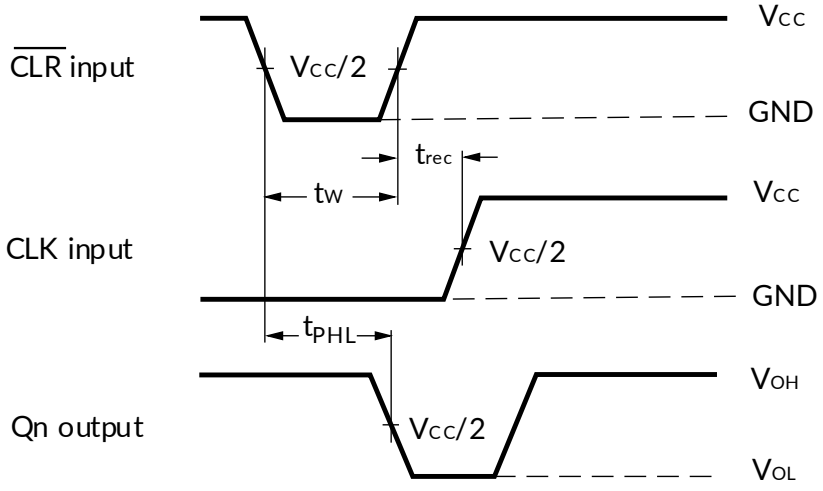
NOTE:
(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) t_{pd} is the same as t_{PHL} and t_{PLH}.
(3) t_t is the same as t_{THL} and t_{TLH}.
(4) C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_O)$ where:
f_i = input frequency in MHz;
f_O = output frequency in MHz;
$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching.

9 Parameter Measurement Information



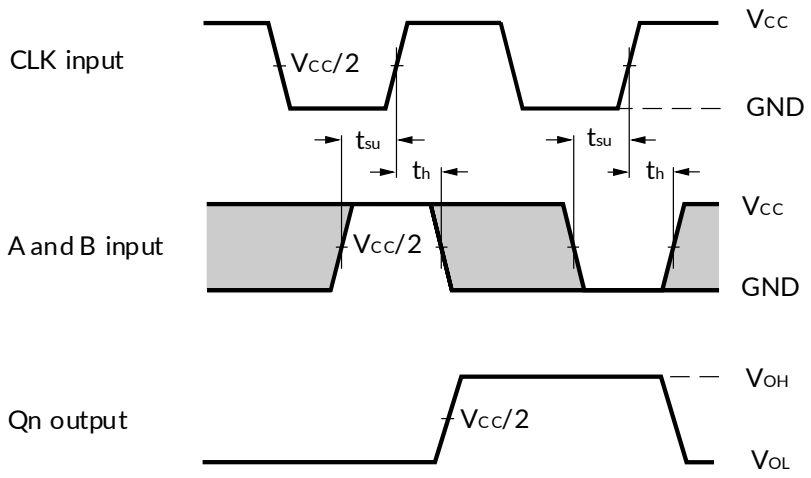
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 1. Waveforms showing the clock (CLK) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



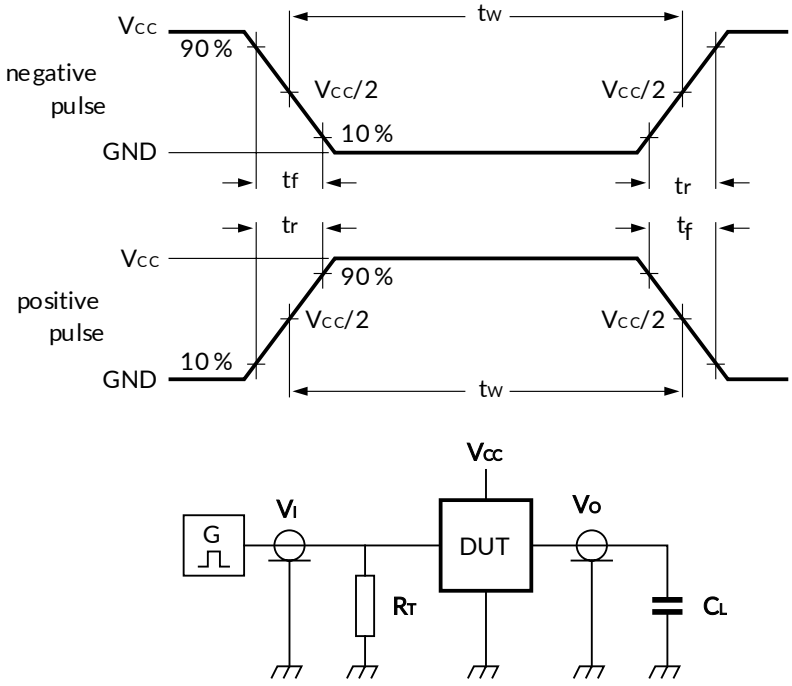
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 2. Waveforms showing the master reset ($\overline{CLR}$) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CLK) removal time



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. Waveforms showing the data set-up and hold times for A and B inputs



Test data is given in Table 1.
Definitions test circuit:
R_T = termination resistance should be equal to output impedance Zo of the pulse generator.
C_L = load capacitance including jig and probe capacitance.

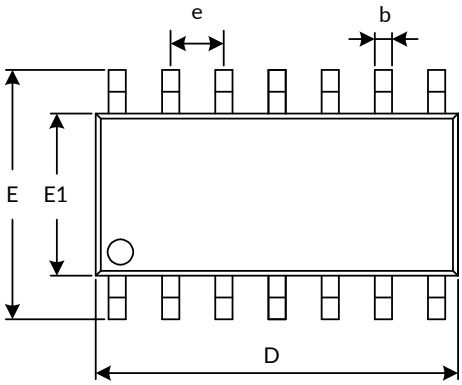
Figure 4. Test circuit for measuring switching times

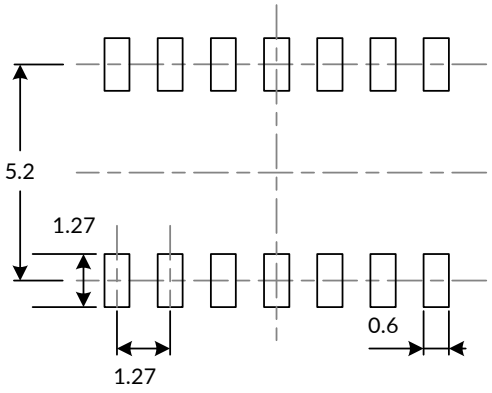
Table 1. Test data

TEST	Input		Load
	V_I	t_r, t_f	C_L
t_{PHL}/t_{PLH}	V_{CC}	6ns	15pF, 50pF

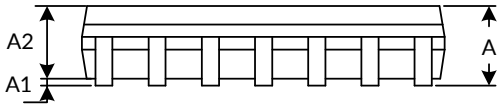
10 PACKAGE OUTLINE DIMENSIONS

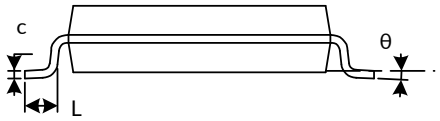
SOIC-14(SOP14) (3)





RECOMMENDED LAND PATTERN (Unit: mm)



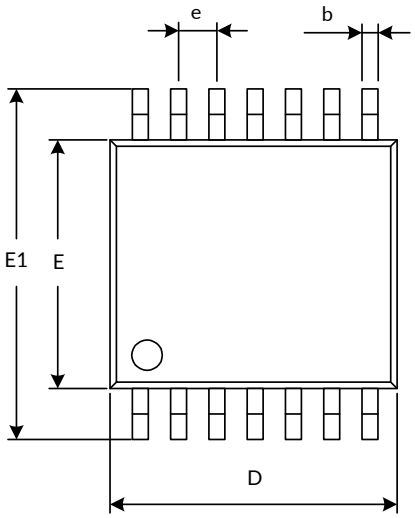


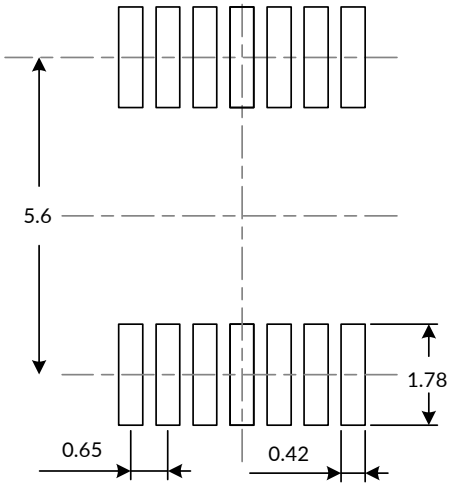
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.750		0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.390	0.470	0.015	0.019
c	0.200	0.240	0.008	0.009
D (1)	8.550	8.750	0.336	0.344
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.500	0.800	0.020	0.031
θ	0°	8°	0°	8°

NOTE:

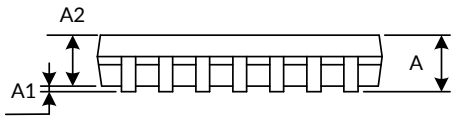
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

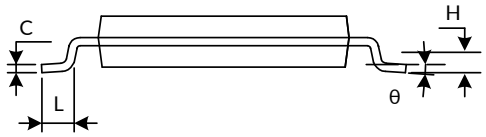
TSSOP-14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
b	0.200	0.300	0.008	0.012
c	0.130	0.170	0.005	0.007
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°

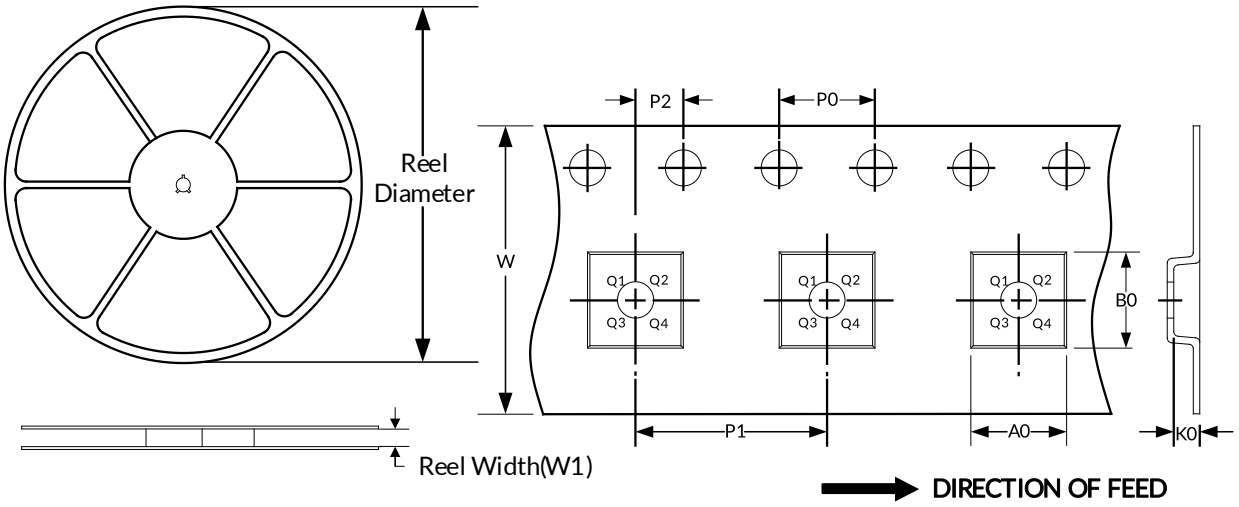
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-14(SOP14)	13”	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13”	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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