

DIO1646

10 Channels (4-Data plus 1-Clock Pairs)

2.5 Gbps Differential MIPI Switch

Features

- Input voltage range: 1.65 to 5 V
- Input signals: 0 to 1.3 V
- DIFF bandwidth: 2.5 GHz (Min)
- Switch type: SPDT (10 channels)
- Signal types: MIPI, D-PHY
- R_{ON} : 5.5 Ω Typical HS MIPI
5.5 Ω Typical LP MIPI
- I_{CCZ} : 1 μ A (Max)
- I_{CC} : 45 μ A (Typ)
- O_{IRR} : -25 dB (Typ)
- X_{talk} : -30 dB (Typ)
- C_{ON} : 1.6 pF (Typ)
- Operating temperature: -40 to 85 °C
- Package: 36-ball WLCSP

Descriptions

The DIO1646 is a 4-Data lane plus 1-Clock pairs MIPI switch. This device is an optimized 10 channels (5 differential) single-pole, double-throw switch for high speed applications.

The DIO1646 is designed to facilitate multiple MIPI compliant devices to connect to a single CSI or DSI module.

The device has excellent bandwidth, low channel to channel skew with little signal degradation.

Applications

- Cellular phones, smart phones
- Displays
- Tablets
- Laptops

Typical Application

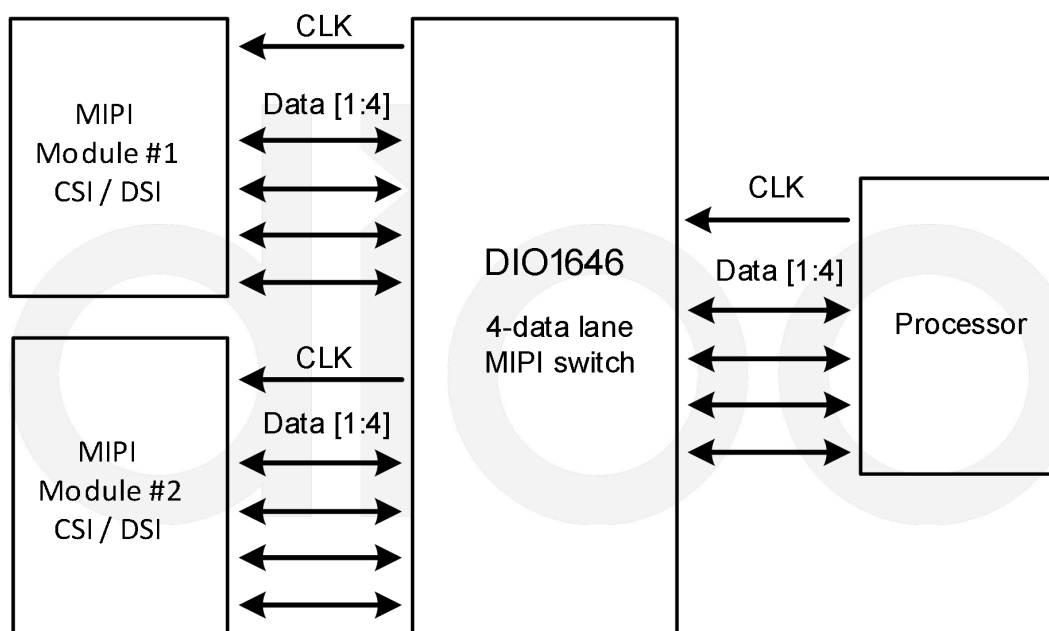


Figure 1. Typical application

Ordering Information

Part No.	Top Marking	RoHS	T _A	Package	
DIO1646WL36	1646	Green	-40 to 85°C	WLCSP-36 0.4mm pitch	Tape & Reel, 3000

Pin Descriptions

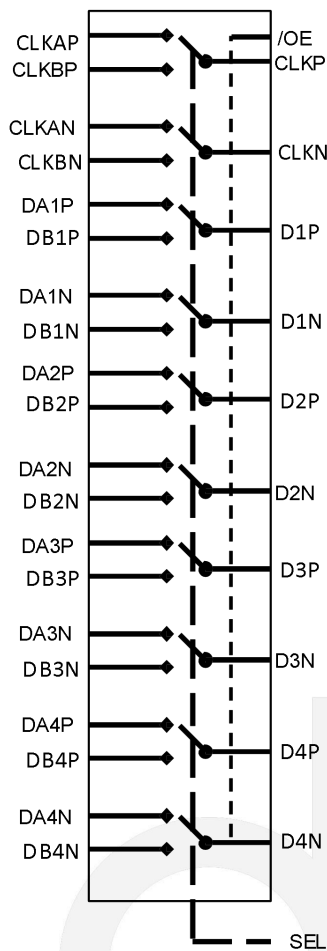


Figure 2. Analog symbol

Pin Name	Description		
CLK _{P/N}	Common clock path		
D1 _{P/N}	Common data path 1		
D2 _{P/N}	Common data path 2		
D3 _{P/N}	Common data path 3		
D4 _{P/N}	Common data path 4		
CLKA _{P/N}	A-side clock path		
DA1 _{P/N}	A-side data path 1		
DA2 _{P/N}	A-side data path 2		
DA3 _{P/N}	A-side data path 3		
DA4 _{P/N}	A-side data path 4		
CLKB _{P/N}	B-side clock path		
DB1 _{P/N}	B-side data path 1		
DB2 _{P/N}	B-side data path 2		
DB3 _{P/N}	B-side data path 3		
DB4 _{P/N}	B-side data path 4		
SEL	Control pin	SEL = 0	CLKP = CLKAP, CLKN = CLKAN Dn(P/N) = DAn(P/N)
		SEL = 1	CLKP = CLKBP, CLKN = CLKBN Dn(P/N) = DBn(P/N)
/OE	Output enable		
V _{CC}	Power		
GND	Ground		
NC	No connect, test pin, do not connect externally.		

Pin Definitions

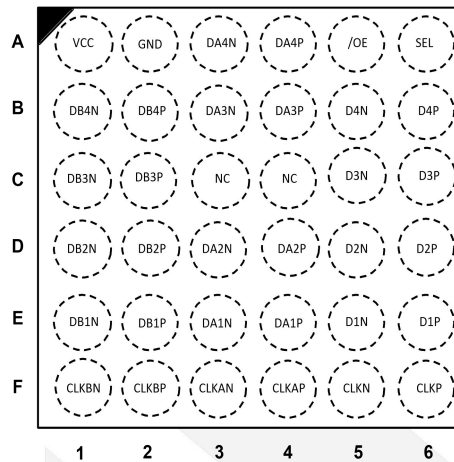


Figure 3. 36-ball WLCSP (Top view)

Ball	Pin Name	Ball	Pin Name
A1	V _{CC}	D1	DB2N
A2	GND	D2	DB2P
A3	DA4N	D3	DA2N
A4	DA4P	D4	DA2P
A5	/OE	D5	D2N
A6	SEL	D6	D2P
B1	DB4N	E1	DB1N
B2	DB4P	E2	DB1P
B3	DA3N	E3	DA1N
B4	DA3P	E4	DA1P
B5	D4N	E5	D1N
B6	D4P	E6	D1P
C1	DB3N	F1	CLKBN
C2	DB3P	F2	CLKBP
C3	NC	F3	CLKAN
C4	NC	F4	CLKAP
C5	D3N	F5	CLKN
C6	D3P	F6	CLKP

Truth Table DB2N

SEL	/OE	Function
LOW	LOW	CLK _P = CLKAP, CLK _N = CLKAN, D _n (P/N) = DAN(P/N)
HIGH	LOW	CLK _P = CLKB _P , CLK _N = CLKB _N , D _n (P/N) = DBN(P/N)
X	HIGH	Clock and data ports high impedance



DIO1646

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply voltage		-0.5	6	V
V _{CNTRL}	DC input voltage (/OE) ⁽¹⁾		-0.5	V _{CC}	V
V _{SW}	DC switch I/O voltage ^(1,2)		-0.5	1.8	V
I _{IK}	DC input diode current		-50		mA
I _{OUT}	DC output current			25	mA
T _{STG}	Storage temperature		-65	150	°C
ESD	HBM	All pins	4.0		kV

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply voltage		1.65	5.0	V
V _{CNTRL}	Control input voltage (SEL, /OE) ⁽³⁾		0	V _{CC}	V
V _{SW}	Switch I/O voltage (CLKN, CLKAN, CLKBN, DN, DAN, DBN)	HS mode	0	0.3	V
		LP mode	0	1.3	
T _A	Operating temperature		-40	85	°C

Note:

3. The control input must be held HIGH or LOW; it must not float.



DIO1646

2:1 MIPI D-PHY (2.5Gbps) 4-Data Lane Switch

DC Electrical Characteristics

Typical values are at $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	V _{CC} (V)	Min	Typ	Max	Unit
V _{IK}	Clamp diode voltage	I _{IN} = -18 mA	1.65		-0.8		V
V _{IH}	Input voltage high	SEL, /OE	1.65 to 5.0	1.20			V
V _{IL}	Input voltage low	SEL, /OE	1.65 to 5.0			0.3	V
I _{IN}	Control input leakage (SEL, /OE)	V _{CNTRL} = 0 to V _{CC}	5.0			1	μA
I _{NO(OFF)} , I _{NC(OFF)}	Off leakage current of port CLKAN, DAN, CLKBN, DBN	V _{SW} =0.0 ≤ DATA ≤ 1.3V	5.0	-0.5		0.5	μA
I _{A(ON)}	On leakage current of common ports (CLKN, DN)	V _{SW} = 0.0 ≤ DATA ≤ 1.3 V	5.0	-0.5		9.5	μA
I _{oz}	Off-state leakage, /OE = High	V _{SW} = 0.0 ≤ DATA ≤ 1.3 V,	5.0	-0.5		14	μA
R _{ON_MIPI_HS}	Switch on resistance for HS MIPI applications ⁽⁴⁾	I _{ON} = -8 mA, /OE = 0 V, SEL=V _{CC} or 0 V, CLKA,B, DBn or DAN = 0.2 V	1.65		5.5	7.3	Ω
			2.5				
			3.3				
			5.0				
R _{ON_MIPI_LP}	Switch on resistance for LP MIPI applications ⁽⁴⁾	I _{ON} = -8 mA, /OE = 0 V, SEL = V _{CC} or 0 V, CLKA,B, DBn or DAN = 1.2 V	1.65		5.5	7.3	Ω
			2.5				
			3.3				
			5.0				
ΔR _{ON_MIPI_HS}	On resistance matching between HS MIPI channels ⁽⁴⁾	I _{ON} = -8 mA, /OE = 0 V, SEL = V _{CC} or 0 V, CLKA,B, DBn or DAN = 0.2 V	1.65		0.3		Ω
			2.5				
			3.3				
			5.0				
ΔR _{ON_MIPI_LP}	On resistance matching between LP MIPI channels ⁽⁴⁾	I _{ON} = -8 mA, /OE = 0 V, SEL = V _{CC} or 0 V, CLKA,B, DBn or DAN = 1.2 V	1.65		0.3		Ω
			2.5				
			3.3				
			5.0				
R _{ON_FLAT_MIPI_HS}	On resistance flatness for HS MIPI signals ⁽⁴⁾	I _{ON} = -8 mA, /OE = 0 V, SEL = V _{CC} or 0 V, CLKA,B, DBn or DAN = 0.1 to 0.3 V	1.65		0.5		Ω
			2.5				
			3.3				
			5.0				

DC Electrical Characteristics

Typical values are at $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	V _{CC} (V)	Min	Typ	Max	Unit
R _{ON_FLAT_MIPLP}	On resistance flatness for LP MIPI signals ⁽⁴⁾	I _{ON} = -8 mA, /OE = 0 V, SEL = V _{CC} or 0 V, CLKA,B, DBn or DAn = 0 to 1.3 V	1.65		0.5		Ω
			2.5				
			3.3				
			5.0				
I _{CCZ}	Quiescent supply current (High impedance)	V _{SEL} = 0 or V _{CC} , I _{OUT} = 0, /OE = V _{CC}	5			1	μA
I _{CC}	Quiescent supply current (Includes charge pump)	V _{SEL} = 0 or V _{CC} , I _{OUT} = 0, /OE = 0	5		45	70	μA
I _{CCCT}	Increase in I _{CC} current per control voltage and V _{CC}	V _{SEL} = 0 or V _{CC} , /OE = 1.65 V	5		1.5		μA

Note:

4. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3 V at $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	V _{CC} (V)	Min	Typ	Max	Unit
t _{INIT}	Initialization time V _{CC} to output ⁽⁵⁾	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.6 V	1.65 to 5		40		μs
t _{EN}	Enable turn-on time, /OE to output	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.6 V	1.65 to 5		50	100	μs
t _{DIS}	Disable turn-off time, /OE to output	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.6 V	1.65 to 5		250		ns
t _{ON}	Turn-on time, SEL to output	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.6 V	1.65 to 5		850		ns
t _{OFF}	Turn-off time, SEL to output	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.6 V	1.65 to 5		250		ns
t _{BBM}	Break-before-make time	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.6 V	1.65 to 5		700		ns
t _{PD}	Propagation delay ⁽⁵⁾	R _L = 50 Ω, C _L = 5 pF	1.65 to 5		0.3		ns
O _{IRR}	Off isolation for MIPI ⁽⁵⁾	R _L = 50 Ω, f = 1250 MHz, /OE = High, V _{SW} = 0.2V _{pp}	1.65 to 5		-25		dB
X _{TALK}	Crosstalk for MIPI ⁽⁵⁾	R _L = 50 Ω, f = 1250 MHz, SEL = High, V _{SW} = 0.2 V _{pp}	1.65 to 5		-30	-20	dB
		R _L = 50 Ω, f = 1250 MHz, SEL = Low, V _{SW} = 0.2 V _{pp}			-30	-20	
DIFF BW	-3dB bandwidth ⁽⁵⁾	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.2 V _{PP}	1.65 to 5	2.5	3		GHz

Note: 5. Guaranteed by characterization.



DIO1646

2:1 MIPI D-PHY (2.5Gbps) 4-Data Lane Switch

High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Typ	Max	Unit
t _{SK(P)}	HS mode skew of opposite transitions of the same output ⁽⁶⁾	R _L = 50 Ω, C _L = 0 pF, V _{SW} = 0.3 V	1.65 to 5		6		ps

Note:

6. Guaranteed by design.

Capacitance

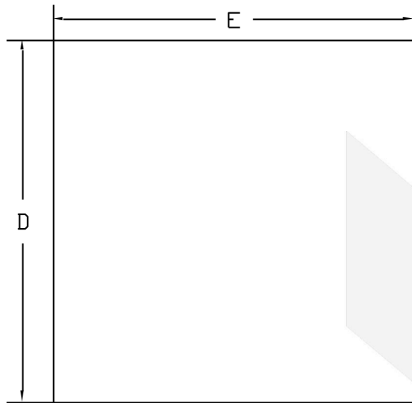
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{IN}	Control pin input capacitance ⁽⁷⁾	V _{CC} = 0 V, f = 1 MHz		2.2		pF
C _{ON}	On capacitance ⁽⁷⁾	V _{CC} = 3.3 V, /OE = 0 V, f = 1250 MHz (In HS common value)		1.6		
C _{OFF}	Off capacitance ⁽⁷⁾	V _{CC} and /OE = 3.3 V, f = 1250 MHz (Both sides in HS common value)		1		

Note:

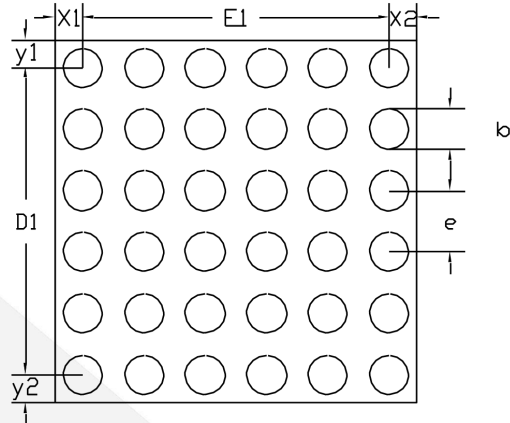
7. Guaranteed by design.



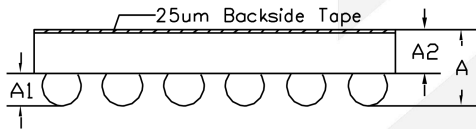
Physical Dimensions: WLCSP-36 0.4mm pitch



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.460	0.500	0.540
A1	0.190	0.210	0.230
A2	0.270	0.290	0.310
D	2.340	2.360	2.380
D1	2.000 BSC		
E	2.340	2.360	2.380
E1	2.000 BSC		
b	0.238	0.258	0.278
e	0.400 BSC		
x1	0.180 REF		
x2	0.180 REF		
y1	0.180 REF		
y2	0.180 REF		



DIO1646

2:1 MIPI D-PHY (2.5Gbps) 4-Data Lane Switch

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as, cell phone, handheld products, laptop, and medical equipment and so on. Dioo's product families include analog signal processing and amplifying, LED drivers and charger IC. Go to <http://www.dioo.com> for a complete list of Dioo product families.

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