

5.0 x 3.2 x 1.2mm
LCC Ceramic Package

Features

- CMOS Output (will interface with TTL devices)
- Enable/Disable Function (optional Standby function)
- 3.3V or 5.0V nominal Supply Voltage
- Size: 5 x 3.2mm
- Factory programmed

Applications

Driving A/Ds, D/As, FPGAs
Digital Video
Ethernet, GbE
Medical
Storage Area Networking
COTS
Broad Band Access
SONET/ SDH/ DWDM
Test & Measurement

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Range	1	-	133	MHz	(3.3V:1-100MHz)
Frequency Stability ²	±25	-	±100	ppm	For all supply voltages, load changes, aging for 1 year at 25°C ± 2°C, shock, vibration and temperatures.
Operating Temperature Range options ²	0 -20 -40	- - -	+70 +70 +85	°C	
Supply Voltage ^{1,2} V _{DD}	2.97	-	5.5	V	See Part Number options on page 2
Supply Current I _{DD} (No Load)	-	-	45 25	mA	V _{DD} = 5.0V V _{DD} = 3.3V
Output Type	CMOS				Cload = 50pF max, V _{DD} = 4.5~5.5V, ≤ 66MHz Cload = 25pF max, V _{DD} = 4.5~5.5V, > 66MHz Cload = 30pF max, V _{DD} = 2.97~3.63V, ≤ 40MHz Cload = 15pF max, V _{DD} = 2.97~3.63V, > 40MHz
	TTL				Cload = 50pF max; V _{DD} = 4.5~5.5V, ≤ 40MHz
Duty Cycle	-	-	-	%	See Page 2
Output V _{OH} (TTL Level) (CMOS Level)	2.4	-	-	V	V _{DD} = 4.5~5.5V
	V _{DD} - 0.4			V	All voltages
Output V _{OL}	-	-	0.4	V	See Load Circuit and waveform page
Output T _{RISE} and T _{FALL}	-	-	-	ns	See page 2
Startup Time	-	-	2	ms	Time for output to reach specified frequency
V _{DISABLE}	-	-	0.8 0.2V _{DD}	V	V _{DD} = 4.5~5.5V V _{DD} = 2.97~3.63V
V _{ENABLE}	2.0 0.7V _{DD}	-			V _{DD} = 4.5~5.5V
Enable Time	-	-	2	ms	
Disable Time - Pin 1 low to Output Hi-Z	-	T/2	T+10	ns	T = Frequency Period
Disable Current	-	-	-	mA	Enable/Disable: Pad 1 low, output disabled; See above Supply Current
	-	0.4	-		Standby option: Pad 1 low, output disabled, oscillator shutdown
RMS Period Jitter	-	8	11	ps	
Period Jitter, Pk-Pk		65	99	ps	>1,000,000 samples
		65	80		≤ 33MHz
					> 33MHz
Storage Temperature Range	-55	-	+125	°C	

Notes: Specifications with Pad 1 E/D open circuit

¹ Place an appropriate power supply bypass capacitor next to device for correct operation

² Specified by part number

Product information is current as of publication date. The product conforms to specifications per the terms of the Cardinal standard warranty. **Apr 25, 2023 Rev. D**
Production processing does not necessarily include testing of all parameters.

Duty Cycle

Parameter	Min	Typ	Max	Unit	
TTL @ 1.4V level; V _{DD} = 4.5~5.5V	45		55	%	Fo ≤ 50 MHz, CL ≤ 50pF 50 MHz < Fo ≤ 66MHz; CL ≤ 15pF 66 MHz < Fo ≤ 125MHz, CL ≤ 25pF 125 MHz < Fo ≤ 133MHz, CL ≤ 15pF
	45		55		
	40		60		
	40		60		
Parameter	Min	Typ	Max	Unit	
CMOS @ 0.5V _{DD} level; V _{DD} = 4.5~5.5V	45		55	%	Fo ≤ 66 MHz, CL ≤ 25pF 66 MHz < Fo ≤ 125MHz; CL ≤ 25pF 125 MHz < Fo ≤ 133MHz, CL ≤ 15pF
	40		60		
	40		60		
Parameter	Min	Typ	Max	Unit	
CMOS @ 0.5V _{DD} level; V _{DD} = 2.97~3.63V	45		55	%	Fo ≤ 40 MHz, CL ≤ 30pF 40 MHz < Fo ≤ 100MHz; CL ≤ 15pF
	40		60		

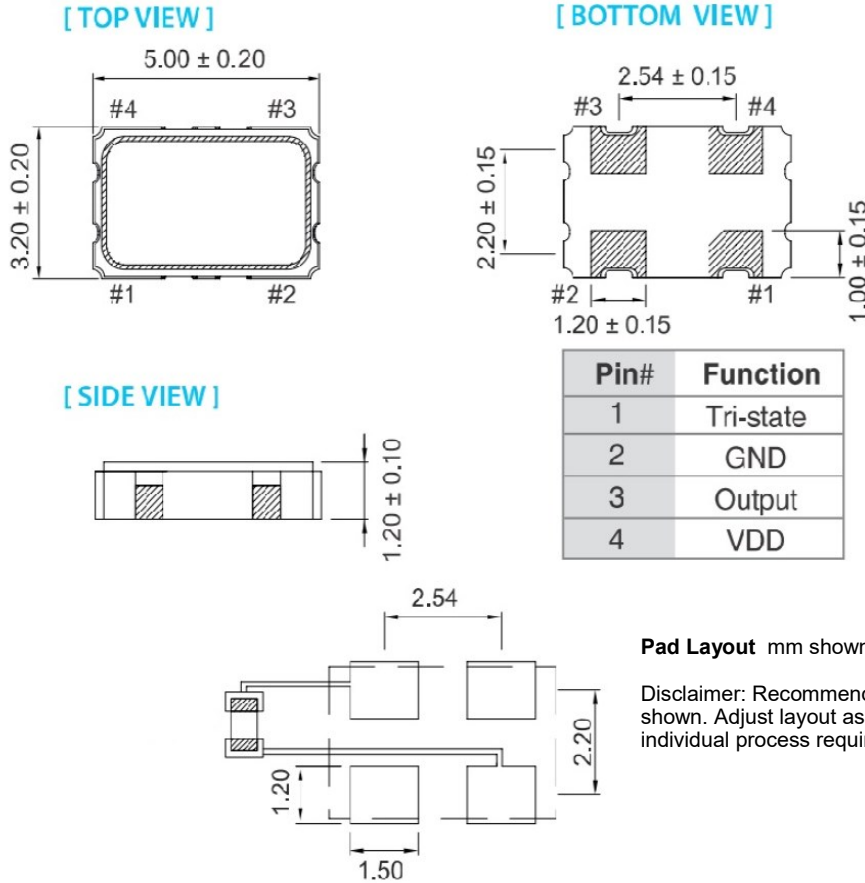
Rise/Fall Time

Parameter	Min	Typ	Max	Unit	
Rise/Fall Time			1.8	ns	0.8V~2.0V, V _{DD} = 4.5~5.5V, CL=50pF 0.8V~2.0V, V _{DD} = 4.5~5.5V, CL=25pF 0.8V~2.0V, V _{DD} = 4.5~5.5V, CL=15pF 0.2V _{DD} ~0.8V _{DD} , V _{DD} = 4.5~5.5V, CL=50pF 0.2V _{DD} ~0.8V _{DD} , V _{DD} = 2.97~3.63V, CL=30pF 0.2V _{DD} ~0.8V _{DD} , V _{DD} = 2.97~3.63V, CL=15pF
			1.2		
			0.9		
			3.4		
			4.0		
			2.4		

Part Number Example: CPPC5LZ-A7BP-50.0TS

Series Model	Logic	Package Size (mm)	Supply Voltage V _{CC}	Packaging	Operating Temperature Range	Frequency Stability (ppm)	Frequency (MHz)	Enable/Disable
CPPL	C	5	L	Z	A7	BP	50.0	TS
	C=CMOS T = TTL	5 = 5 x 3.2	L = 3.3V Blank= 5.0V	Blank = Tape Only Z= Tape/reel	Blank = 0 to +70°C A5 = -20 to +70°C A7 = -40 to +85°C	BR = ±25 BP = ±50 B6 = ±100	5V: 1 - 133 3.3V: 1 - 100	TS = Tristate PD = Powerdown

Mechanical Dimensions (mm)



Pin#	Function
1	Tri-state
2	GND
3	Output
4	VDD

Pin 1	Output
Open	Active
Logic '1'	Active
Ground	Tri-state

Pad Layout mm shown

Disclaimer: Recommended layout shown. Adjust layout as needed for individual process requirements.

To ensure optimal oscillator performance, place a by-pass capacitor of 0.01~0.1µF as close to the part as possible between Vdd and GND pads.

Contacts (pads): Gold (0.3 to 1.0 µm) over Nickel (1.27 to 8.89 µm)

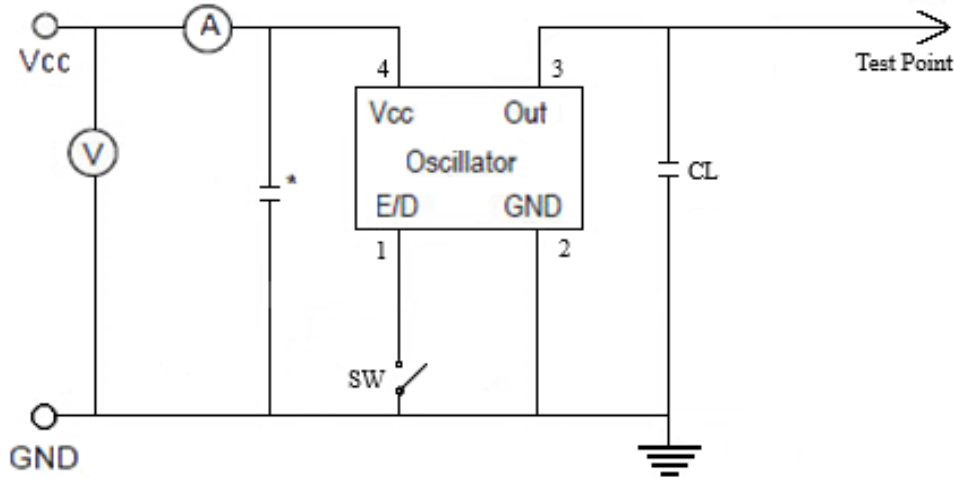
Cardinal Components Inc. certifies this device is in accordance with the RoHS and REACH directives.

Cardinal Components guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
 Weight of the Device: 0.09 grams
 Moisture Sensitivity Level: 1 As defined in J-STD-020D
 Second Level Interconnect code: e4

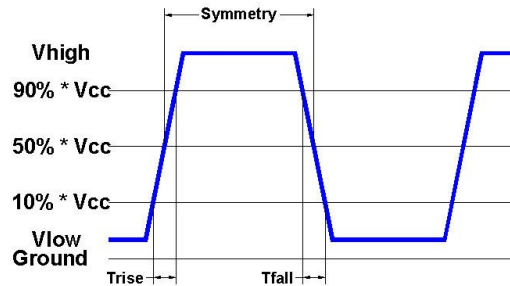
For Optimum Jitter Performance, Cardinal recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Electrical Test / Load Circuit



Notes:
 CL: 15pF Includes the input capacitance of oscilloscope
 * 0.01~0.1 μ F external by-pass filter is recommended



Environmental / ESD Ratings

Reliability: Environmental

Parameter	Condition
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A
Solderability	IPC J-STD-002
Thermal Cycle	MIL-STD-883 Method 1010, Condition B

ESD Rating

Model	Min. Voltage	Condition
Human Body Model	2000V	MIL-STD-883 3015.7
Machine Model	200V	EIAJ ED-4701/304

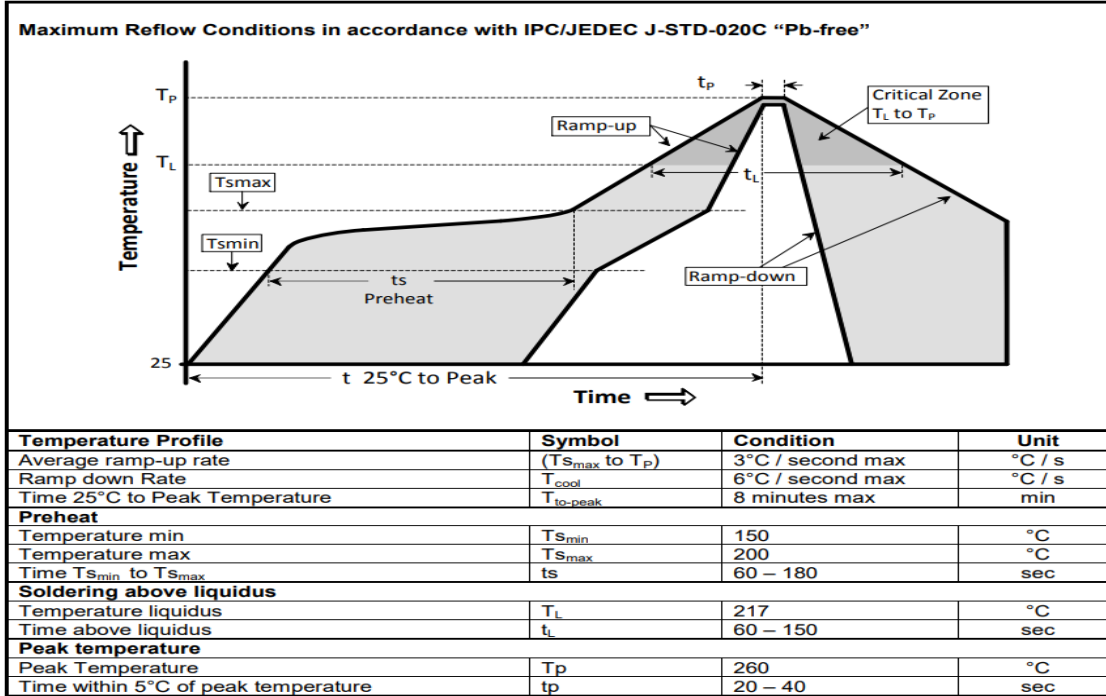
Absolute Maximum Ratings

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +7.0V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics:

The maximum die or junction temperature is 100°C

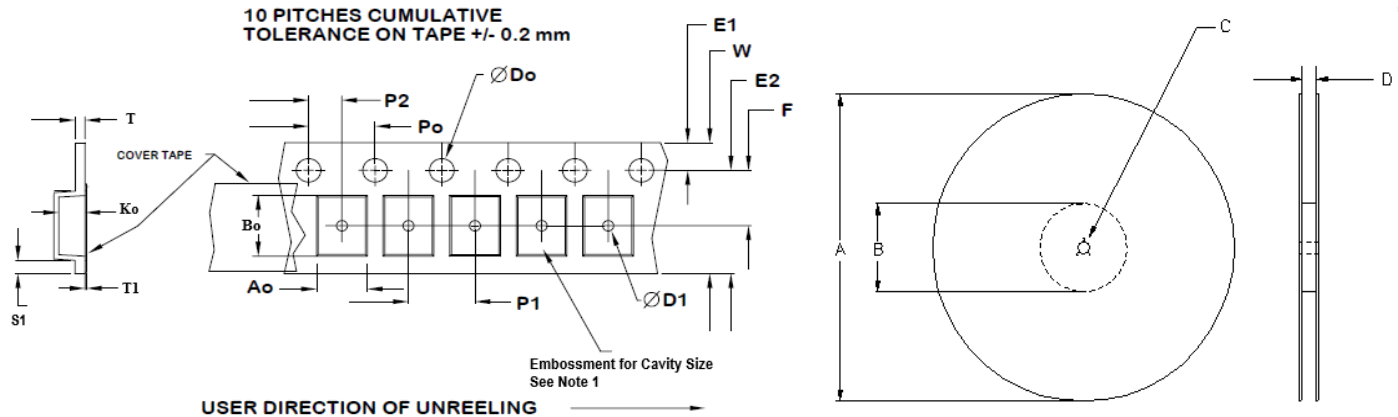
Reflow Cycle



The part may be reflowed 2 times without degradation (typical for lead free processing).

Tape and Reel

Tape and Reel available for quantities of 250 to 1000 per reel, cut tape for < 250. 12mm tape, 8mm pitch.



Tape Size	E2 typ	F	P1	W max	Ao	Bo	Ko
12mm	10.25	5.5 ±0.05	8.0 ±0.1	12.2	3.6±0.1	5.4±0.1	1.4±0.1

Dimensions in mm Drawing Not to scale
Note 1: Embossed cavity to conform to EIA- 481-B

Tape Size	Do	D1 typ	E1	Po	P2	S1 min	T typ	T1 max
12mm	1.5 +0.1 -0.0	1.5	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.3	0.1

Reel Size	A		B		C	D
	Inches	mm	Inches	mm		
7	7.0	177.8	2.50	63.5	13.0 +0.5 -0.2	Tape size +0.4 +2.0 -0.0
10	10.0	254.0	4.00	101.6		
13	13.0	330.2	3.75	95.3		

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