ALLEGRO microsystems

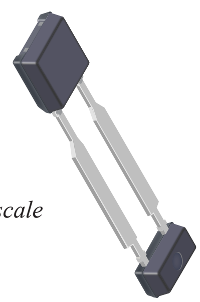
A1698

Two-Wire, True Zero-Speed, High Accuracy Sensor IC with Speed and Direction Output

FEATURES AND BENEFITS

- Integrated capacitor for EMC suppression in a single overmolded miniature package
- Wide leads facilitate ease of assembly
- True zero-speed operation
- Pulse-width output protocol
- Automatic Gain Control (AGC) for air gap independent switch points
- Automatic Offset Adjustment (AOA) for signal processing optimization, providing large operating air gap range
- Single chip sensing IC for high reliability
- Fully synchronous digital logic with Scan and IDDQ testing

Package: 2-pin SIP (suffix UB)



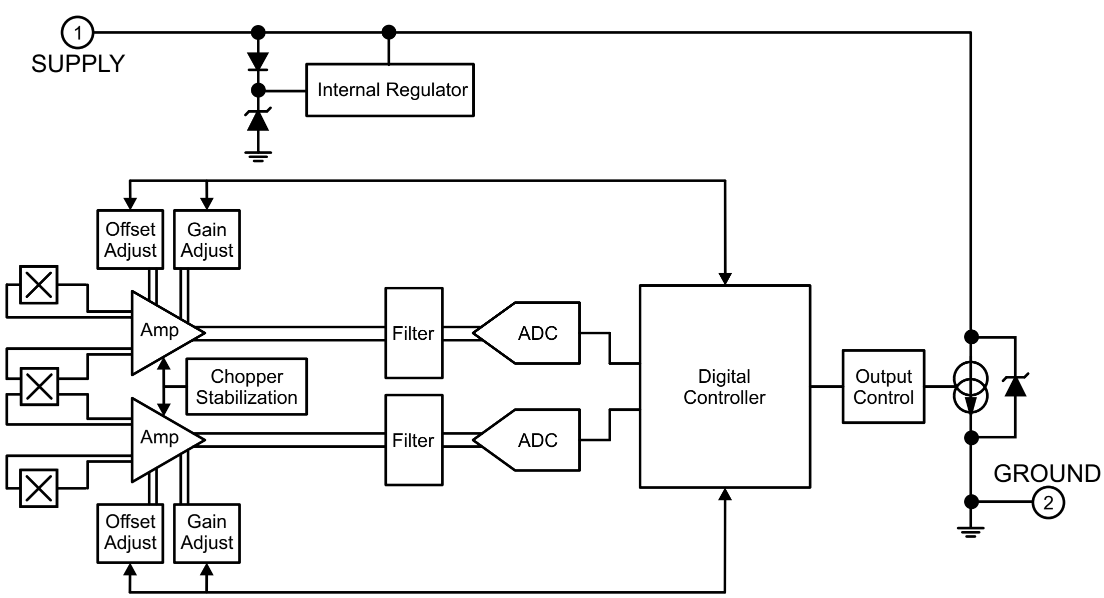
Not to scale

DESCRIPTION

The A1698 is a Hall-effect-based integrated circuit (IC) that provides a user-friendly solution for two-wire speed sensing of ring magnets or ferrous targets (when back-biased by the user) down to zero-speed in applications where speed and direction is required. The A1698 is offered in the UB package, which integrates the IC and a high temperature ceramic capacitor in a single overmolded SIP package. The integrated capacitor provides enhanced EMC performance.

The integrated circuit incorporates Hall-effect circuits and signal processing that switches in response to differential magnetic signals created by magnetic encoders, or, when properly back-biased with a magnet, from ferromagnetic targets. The circuitry contains a sophisticated digital circuit that reduces magnet and system offsets, calibrates the gain for air gap independent switch points, and provides true zero-speed operation.

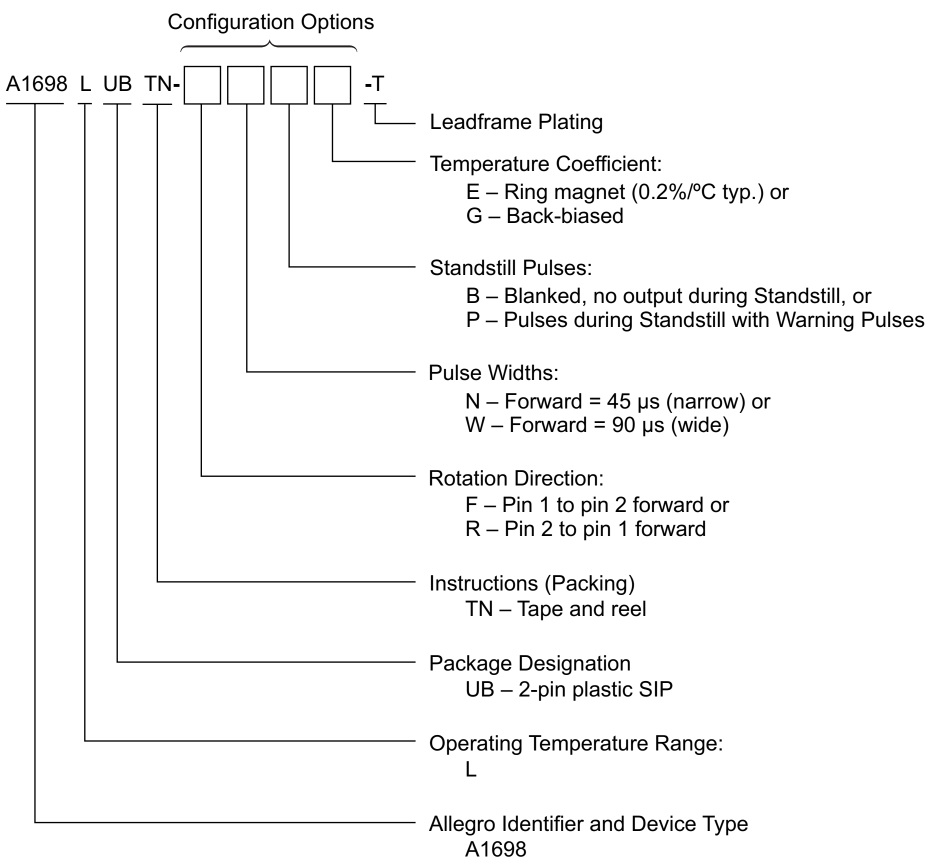
The regulated current output is configured for two-wire interface circuitry and is ideally suited for obtaining speed and direction information in wheel speed applications. The 2-pin SIP package is lead (Pb) free, with tin leadframe plating.



Functional Block Diagram

SELECTION GUIDE

Part Number	Temperature Coefficient	Air Gap Warning and Standstill Function
A1698LUBTN-FWPE-T	Ring Magnet	Yes
A1698LUBTN-FWPG-T	Back-Biased	Yes
A1698LUBTN-FWBE-T	Ring Magnet	No
A1698LUBTN-FWBG-T	Back-Biased	No



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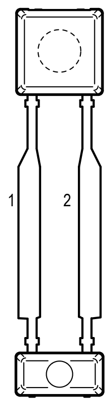
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C



UB Package, 2-Pin SIP Pinout Diagram

Terminal List Table

Name	Number	Function
VCC	1	Supply Voltage
GND	2	Ground

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Test Conditions	Value (Typ.)	Unit
Nominal Capacitance	C_{SUPPLY}	Connected between VCC and GND	2200	pF

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OPERATING CHARACTERISTICS: Valid throughout full operating and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Operating, $T_J < T_{J(max)}$	4	–	24	V
Reverse Supply Current [3]	I_{RCC}	$V_{CC} = V_{RCC(max)}$	–	–	–10	mA
Supply Zener Clamp Voltage	$V_{Zsupply}$	$I_{CC} = I_{CC(max)}$ + 3 mA, T_A = 25°C	28	–	–	V
OUTPUT						
Power-On State				$I_{CC(LOW)}$		–
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	7	8.4	mA
	$I_{CC(HIGH)}$	High-current state	12	14	16	mA
Supply Current Ratio	$I_{CC(HIGH)}$ / $I_{CC(LOW)}$	Measured as ratio of high current to low current (isothermal)	1.9	–	–	–
Supply Current Stabilization Time		Signal stabilization time from V_{CC} > undervoltage lockout level	–	–	1	ms
Output Rise/Fall Time	t_r, t_f	Voltage measured at terminal 2 in Figure 1, R_L = 100 Ω, C_L = 10 pF, measured between 10% and 90% of signal.	0	–	1.5	μs
OPERATING CHARACTERISTICS						
Operate Point	B_{OP}	% of peak-to-peak IC-processed magnetic signal	–	60	–	%
Release Point	B_{RP}	% of peak-to-peak IC-processed magnetic signal	–	40	–	%
Operating Frequency	f		0	–	5	kHz
Input Signal	B_{SIG}	Differential signal, measured peak to peak	20	–	1200	G
Air Gap Warning	B_{WARN}	-P variant	–	2 × $B_{SIG(MIN)}$	–	G
Allowable User-Induced Differential Offset	B_{SIGEXT}	External differential signal bias (DC), operating within specification	–300	–	300	G
Sensitivity Temperature Coefficient [5]	T_C	Valid for full temperature range: *E* variant, Ring Magnet	–	+0.2	–	%/°C
		Valid for full temperature range: *G* variant, Back-Biased	–	TBD	–	%/°C
Total Pitch Deviation		For constant B_{SIG}, sine wave	–	–	+/-2	%
Front-End Chopping Frequency			–	340	–	kHz
OUTPUT PULSE CHARACTERISTICS, PULSE PROTOCOL[4]						
Pulse Width Off Time	$t_{w(Pre)}$		38	45	52	μs
Pulse Width, Air Gap Warning	$t_{w(Warn)}$	-P variant	38	45	52	μs
Pulse Width, Forward Rotation	$t_{w(FWD)}$	-N variant	38	45	52	μs
		-W variant	76	90	104	μs
Pulse Width, Reverse Rotation	$t_{w(REV)}$	-N variant	76	90	104	μs
		-W variant	153	180	207	μs
Pulse Width, Standstill	$t_{w(STOP)}$	-P variant	1232	1440	1656	μs
Standstill Period	T_{STOP}	-P variant	590	737	848	ms

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative discussions in Power Derating section.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Load circuit is R_L = 100 Ω and C_L = 10 pF. Pulse duration measured at threshold of (($I_{CC(HIGH)}$ + $I_{CC(LOW)}$) /2).
[5] Ring magnet decreases strength with rising temperature. Device compensates. Note that B_{SIG} requirement is not influenced by this.

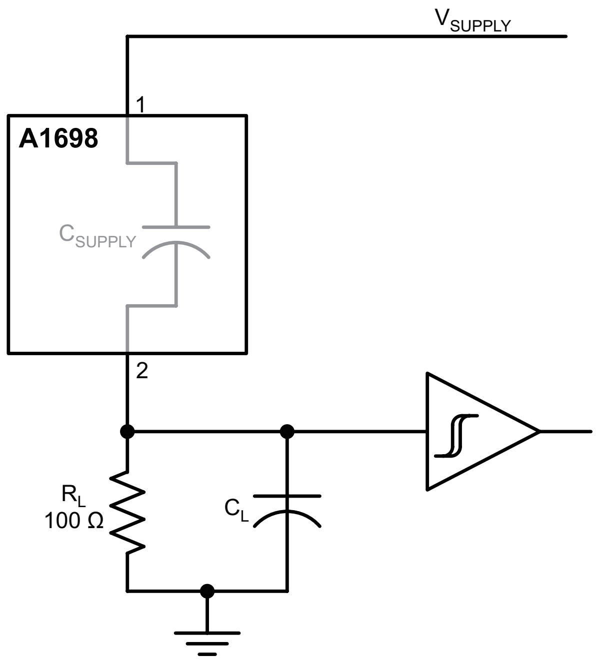


Figure 1: Typical Application Circuit

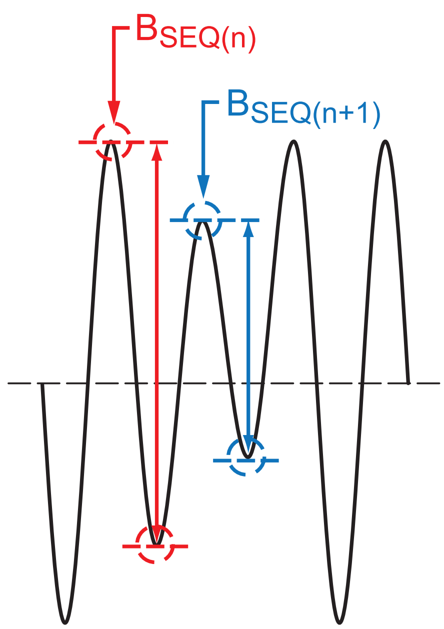
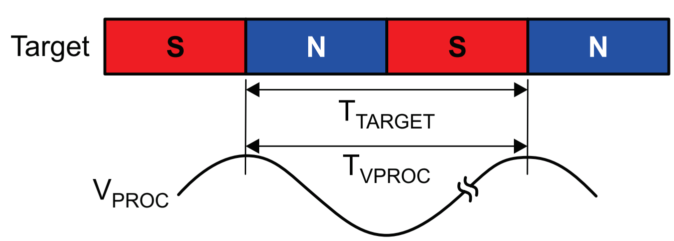


Figure 2: Differential Signal Variation



V_{PROC} = the processed analog signal of the sinusoidal magnetic input (per channel)

T_{TARGET} = the period between successive sensed target magnetic edges of the same polarity (either both north-to-south or both south-to-north)

Figure 3: Definition of T_{TARGET}

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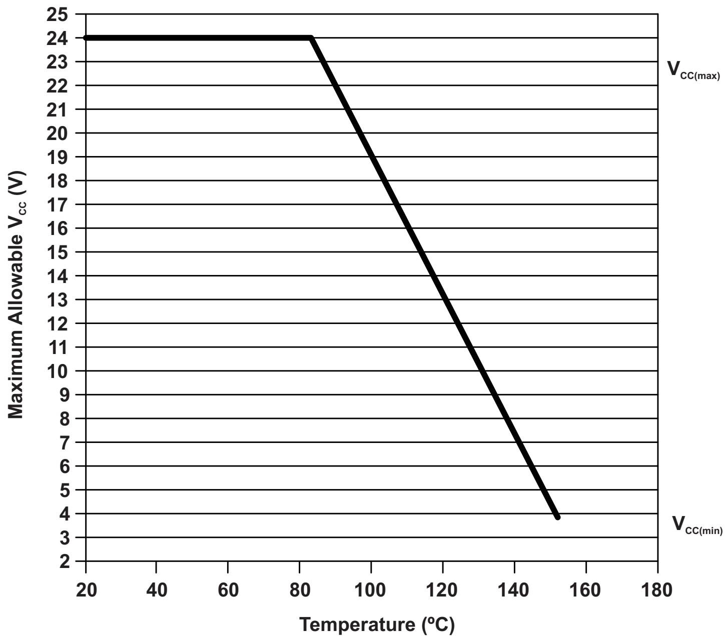
THERMAL CHARACTERISTICS

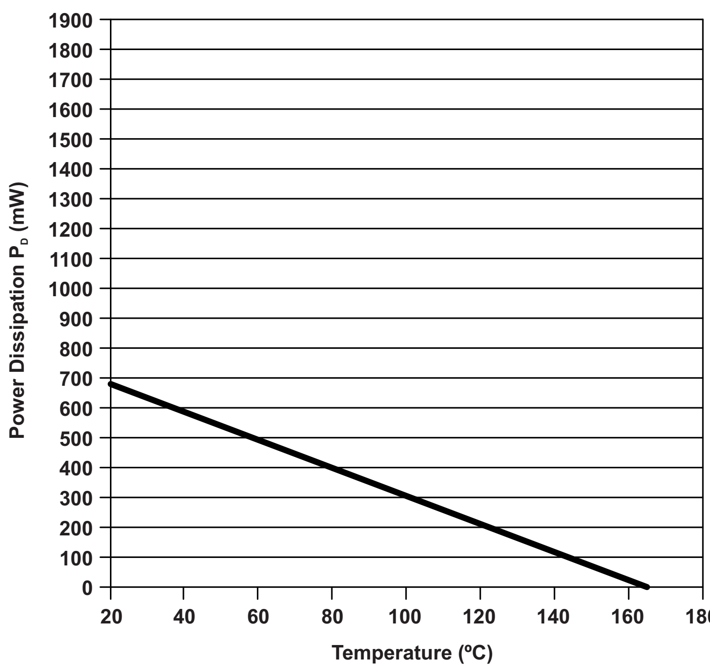
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	213	°C/W

*Additional thermal information is available on the Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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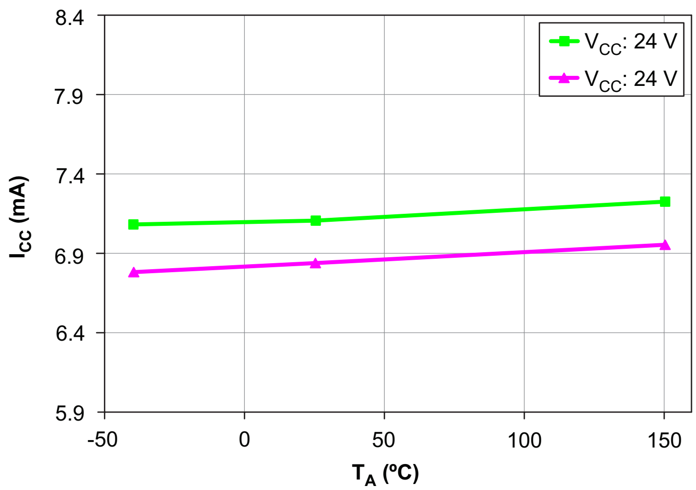
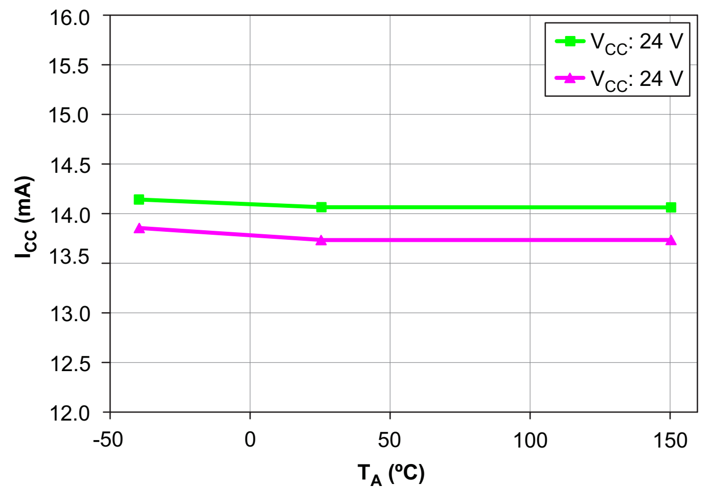
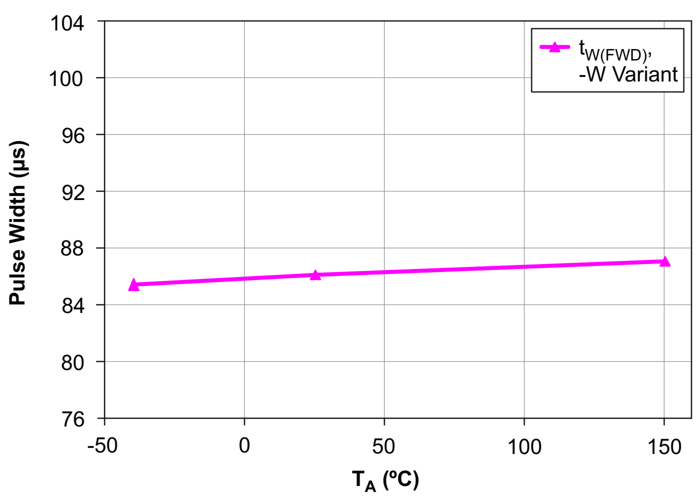
CHARACTERISTIC PLOTS



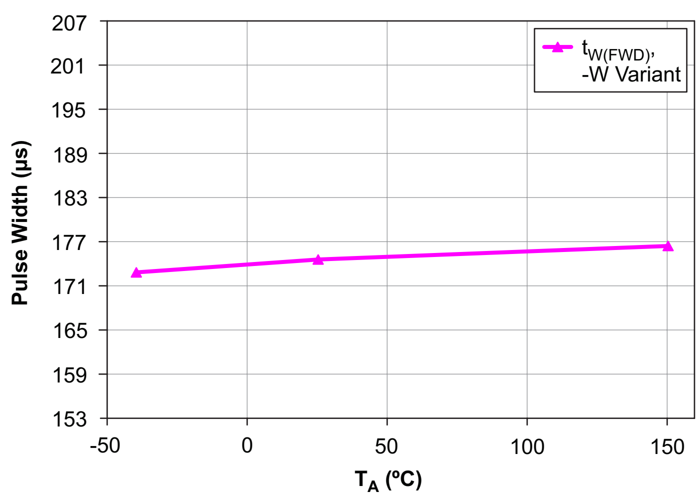
Supply Current versus Ambient Temperature



Supply Current versus Ambient Temperature



Output Pulse Widths versus Ambient Temperature



Output Pulse Widths versus Ambient Temperature

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FUNCTIONAL DESCRIPTION

The sensor IC contains a single-chip Hall-effect circuit that supports a trio of Hall elements. These elements are used in differential pairs to provide electrical signals containing information regarding edge position and direction of target rotation. The A1698 is intended for use with ring magnet targets, or, when back-biased with an appropriate magnet, with ferromagnetic targets (gears). The IC detects the peaks of the magnetic signals and sets dynamic thresholds based on these detected signals.

Data Protocol Description

When a target passes in front of the device (opposite the branded face of the package case), the A1698 generates an output pulse for each magnetic pole, or each tooth and valley, of the target. Speed information is provided by the output pulse rate, while direction of target rotation is provided by the duration of the output pulses. The sensor IC can sense target movement in both the forward and reverse directions. The translation of magnetic input to the output is shown in Figure 6.

FORWARD ROTATION

For the –F variant, when the target is rotating such that a target feature passes from pin 1 to pin 2, this is referred to as forward rotation. This direction of rotation is indicated on the output by a $t_{W(FWD)}$ pulse width. For the –R variant, forward direction is indicated for target rotation from pin 2 to 1 (see Figure 4).

REVERSE ROTATION

For the –F variant, when the target is rotating such that a target feature passes from pin 2 to pin 1, this is referred to as reverse rotation. This direction of rotation is indicated on the output by a $t_{W(REV)}$ pulse width. For the –R variant, reverse direction is indicated for target rotation from pin 1 to 2.

Output edges are triggered by V_{PROC} transitions through the switch points. On a crossing, the output is first set to $I_{CC(LOW)}$ for a duration of $t_{w(PRE)}$, after which the output pulse of $I_{CC(HIGH)}$ is present for $t_{w(FWD)}$ or $t_{w(REV)}$.

The IC is always capable of properly detecting input signals up to the defined operating frequency. However, the end user will note that a sequence of $t_{w(PRE)}$ and $t_{w(REV)}$ does meet this frequency. The $t_{w(PRE)}$ period is dominant, thus always providing rising output edge, but, at high frequencies, potentially truncating the $I_{CC(HIGH)}$ duration.

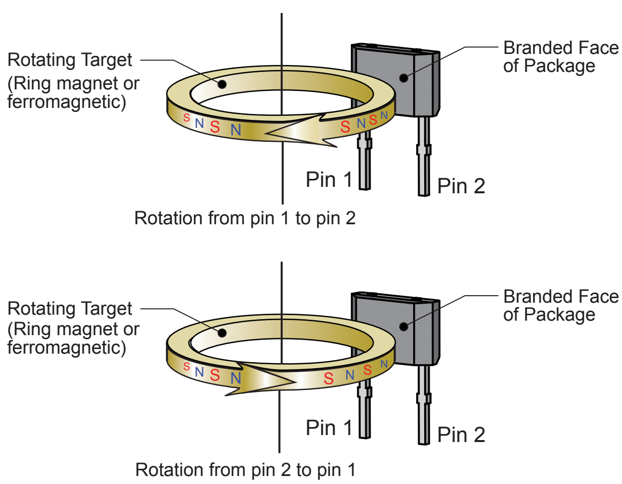

Figure 4: Target Orientation Relative to Device (ring magnet shown).

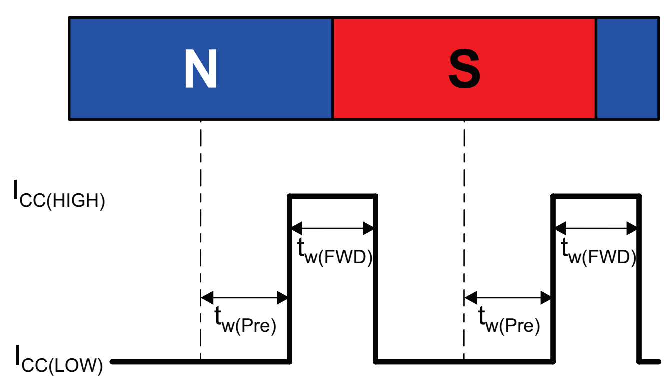

Figure 5: Output Timing Example

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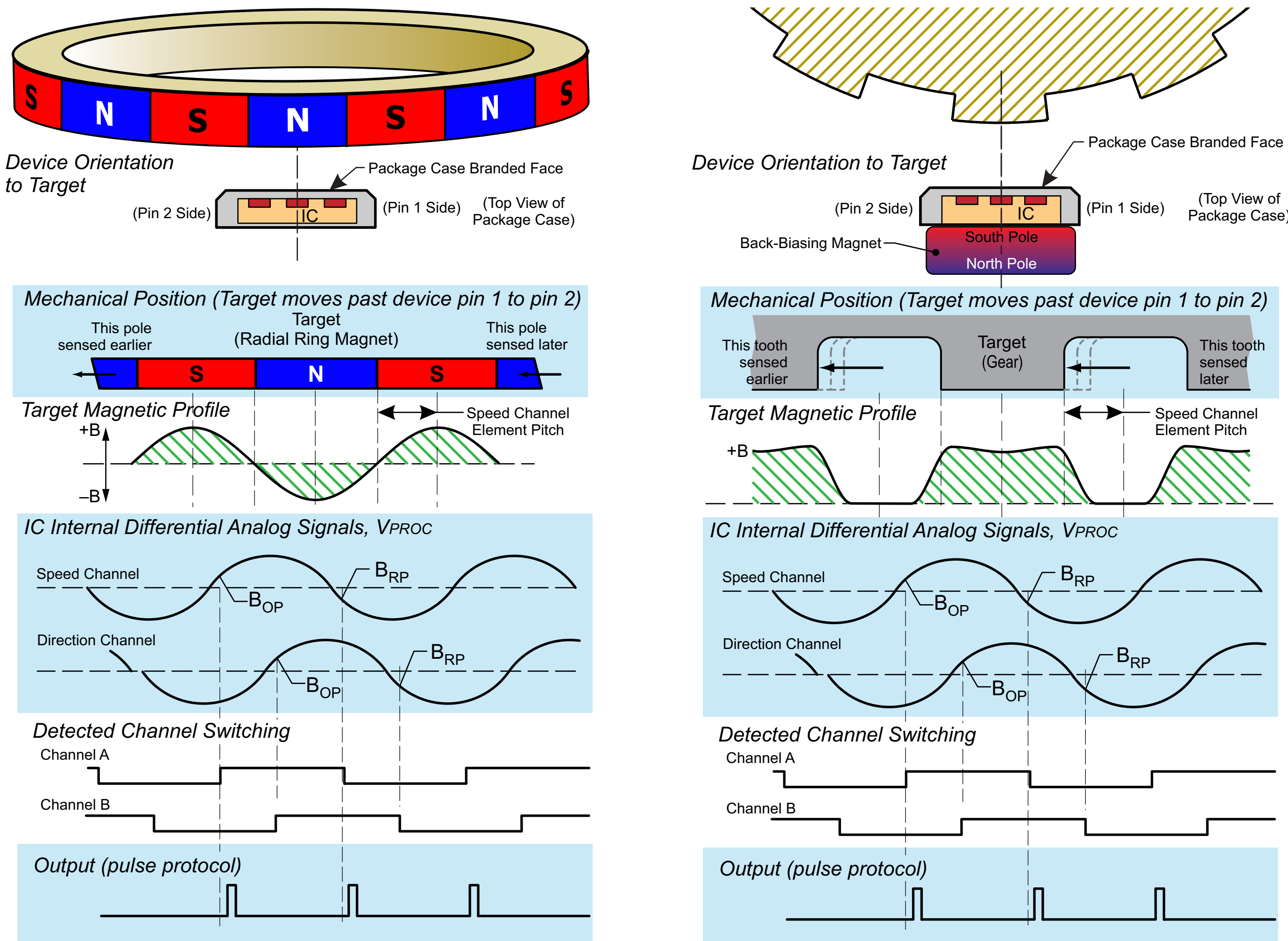

Figure 6: Basic Operation

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Calibration and Direction Validation

When power is applied to the A1698, the sensor IC internally detects the profile of the target. The gain and offset of the detected signals are adjusted during the calibration period, normalizing the internal signal amplitude for the installation air gap of the device.

The Automatic Gain Control (AGC) feature ensures that operational characteristics are isolated from the effects of installation air gap variation.

Automatic Offset Adjustment (AOA) is circuitry that compensates for the effects of chip, magnet, and installation offsets. This circuitry works with the AGC during calibration to adjust V_{PROC} in the internal A-to-D range to allow for acquisition of signal peaks. AOA and AGC function separately on the two differential signal channels.

During calibration, output pulses with direction information are immediately transmitted to the output. Depending on target design, air gap, and the phase of the target, direction may be momentarily incorrect.

Following a direction change in running mode, direction changes are immediately transmitted to the output. Depending on target design and the phase of the target, direction may be fleetingly incorrect.

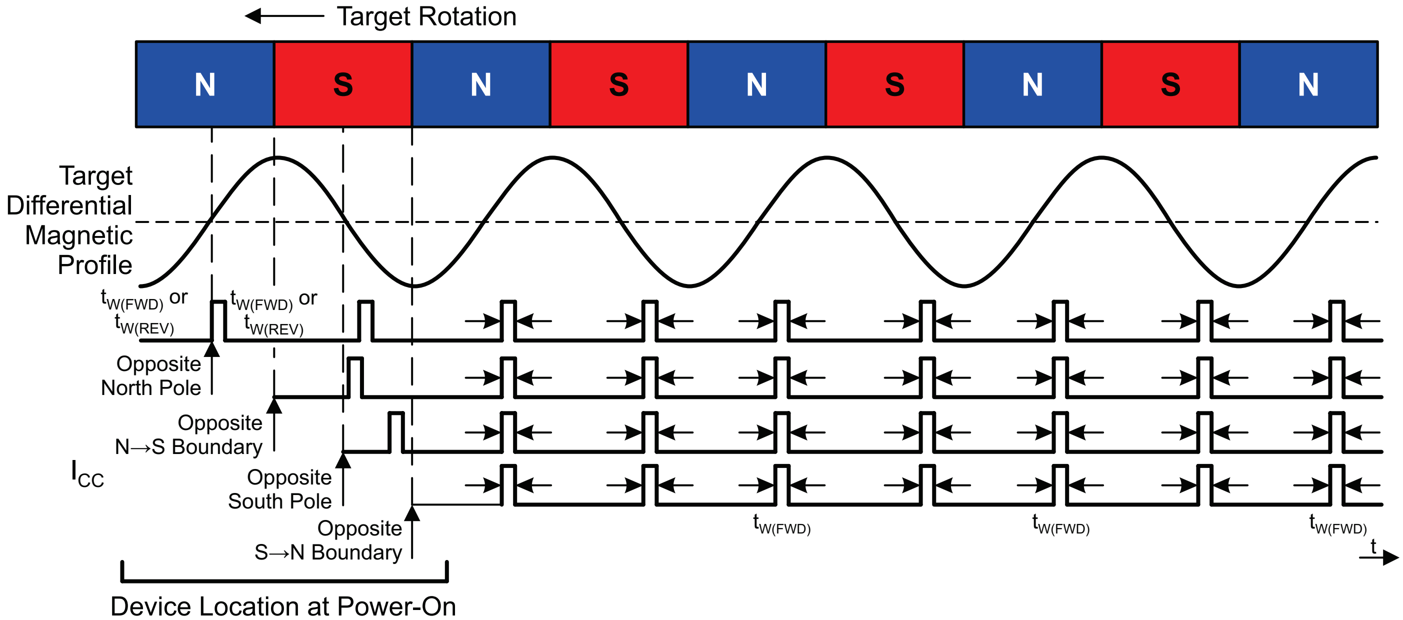

Figure 7: Startup Position Effect on First Device Output Switching

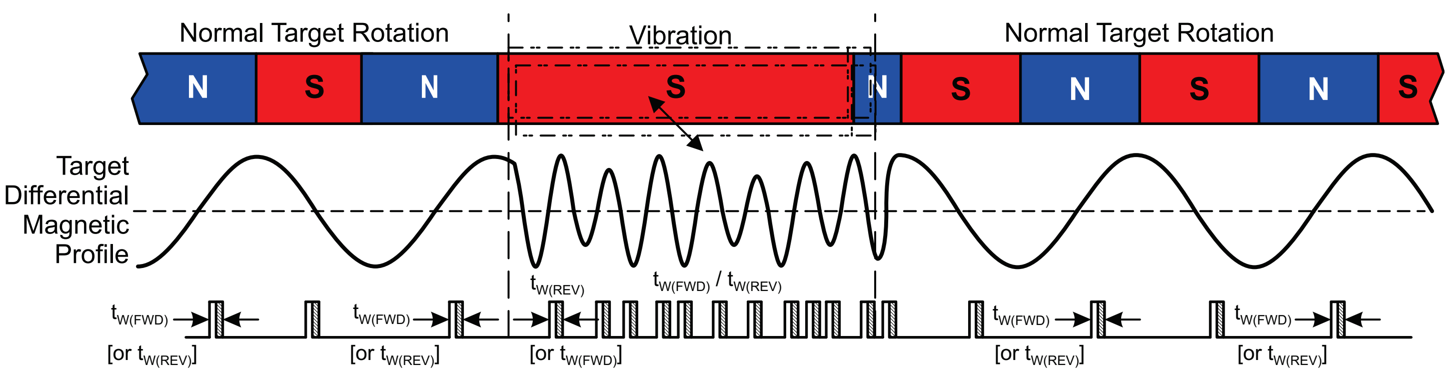

Figure 8: Output Functionality in the Presence of Running Mode Target Vibration

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POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 14 mA, and $R_{\theta JA}$ = 213 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7\ mA = 84\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 84\ mW \times 213\ °C/W = 17.9°C$$

$$T_J = T_A + \Delta T = 25°C + 17.9°C = 42.9°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UB, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=213°C/W, $T_{J(max)}$=165°C, $V_{CC(max)}$= 24 V, and $I_{CC(AVG)}$ = 14.66 mA. $I_{CC(AVG)}$ is computed using $I_{CC(HIGH)(max)}$ and $I_{CC(LOW)(max)}$, with a duty cycle of 73% computed from $t_{w(REV)(max)}$ on-time and $t_{w(FW)(min)}$ off-time (pulse width protocol). This condition happens at a select limiting frequency.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 213\ °C/W = 70.4\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(AVG)} = 70.4\ mW \div 14.6\ mA = 4.8\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000408, Rev. 4)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

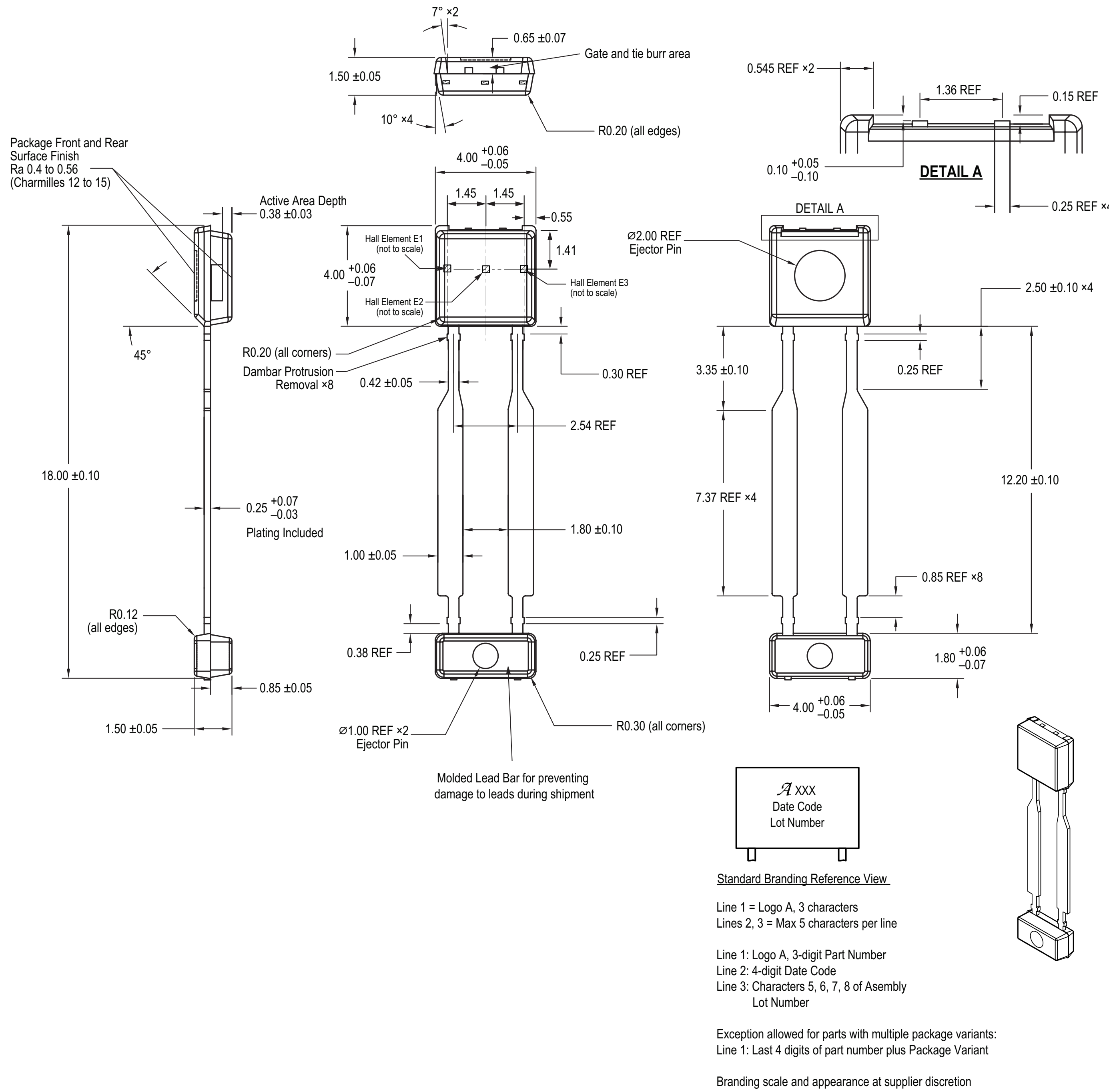

Figure 9: Package UB, 2-Pin SIP

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Revision History

Number	Date	Description
–	March 24, 2015	Initial release.
1	May 6, 2015	Corrected typo in Selection Guide.
2	March 2, 2016	Updated Package Outline Drawing molded lead bar footnote, Internal Discrete Capacitor Ratings table, and miscellaneous editorial changes.
3	September 26, 2016	Corrected Package Outline Drawing.
4	March 29, 2019	Minor editorial updates
5	April 3, 2020	Updated Package Outline Drawing, and minor editorial updates
6	April 4, 2022	Updated package drawing (page 12)

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