Bi-directional ESD Protection Diode

FEATURES

- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Designed for mounting on small surface
- Protects one Bi-directional I/O line
- Moisture sensitivity level 1
- Working Voltage : 5V, 12V, 24V
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

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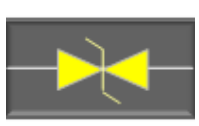


Pb-Free

RoHS COMPLIANT

MECHANICAL DATA

- Case: 1005 small outline plastic package
- Terminal : Gold plated, solder per MIL-STD-705, method 2026 guaranteed
- High temperature soldering guaranteed : 260°C/10s
- Weight: 6 ± 0.5 mg

APPLICATIONS

- Cell Phone Handsets and Accessories
- Notebooks, Desktops, and Servers
- Keypads, Side Keys, USB 2.0, LCD Displays
- Portable Instrumentation
- Touch Panel

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20μs waveform)	TESDL5V0	P_{PP}	75	W
	TESDL12V		25	
	TESDL24V		47	
ESD per IEC 61000-4-2 (Air)		V_{ESD}	± 15	KV
ESD per IEC 61000-4-2 (Contact)			± 8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

PARAMETER			SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage	TESDL5V0		V_{RWM}	-	5	V
	TESDL12V			-	12	
	TESDL24V			-	24	
Reverse Breakdown Voltage	TESDL5V0	I_R = 1 mA	$V_{(BR)}$	5.1	-	V
	TESDL12V			13	-	
	TESDL24V			25	-	
Reverse Leakage Current	TESDL5V0	V_R = 5 V	I_R	-	2	μA
	TESDL12V	V_R = 12 V				
	TESDL24V	V_R = 24 V				
Clamping Voltage	TESDL5V0	I_{PP} = 1 A	V_C	-	9.8	V
		I_{PP} = 5 A		-	15	
Clamping Voltage	TESDL12V	I_{PP} = 1 A	V_C	-	25	V
		I_{PP} = 5 A		-	33	
Clamping Voltage	TESDL24V	I_{PP} = 1 A	V_C	-	47	V
		I_{PP} = 5 A		-	51	
Junction Capacitance	TESDL5V0	V_R = 0 V f = 1.0 MHz	C_J	15		pF
	TESDL12V			12		
	TESDL24V			10		

RATINGS AND CHARACTERISTICS CURVES

(T_A=25°C unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

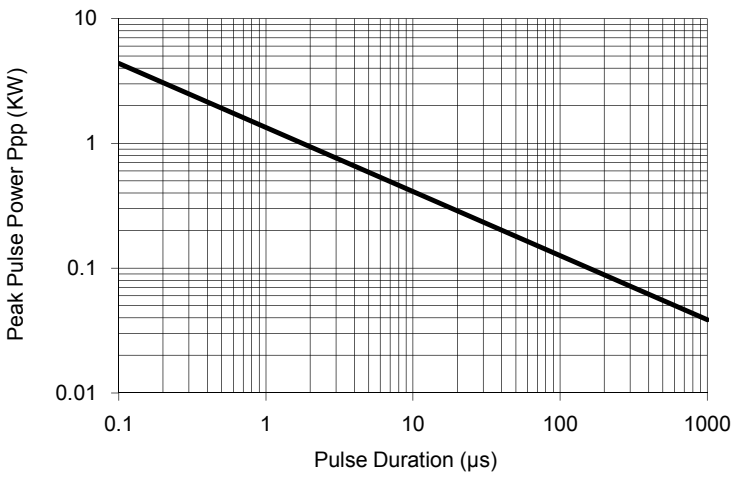


Fig. 2 Pulse Waveform

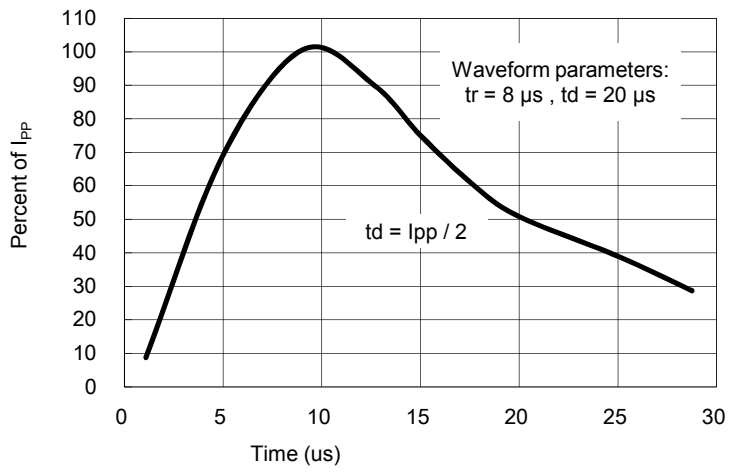


Fig. 3 Admissible Power Dissipation Curve

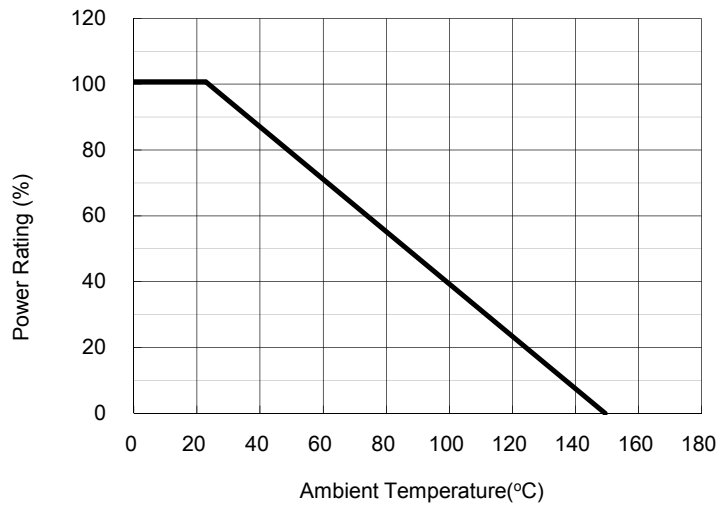


Fig. 4 Typical Junction Capacitance

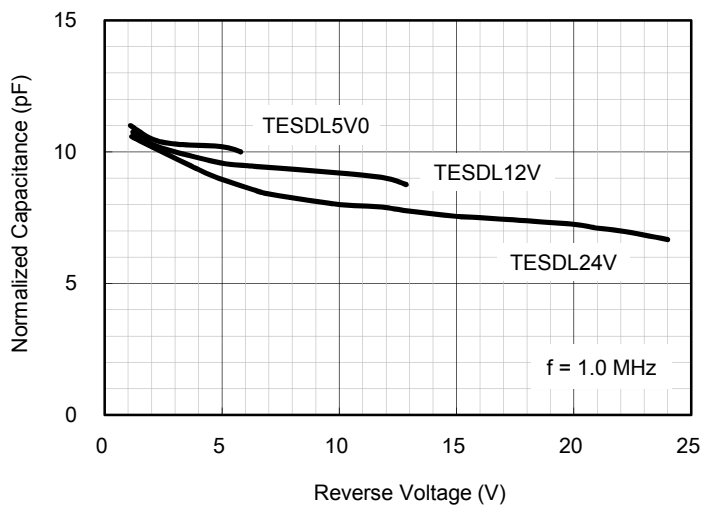
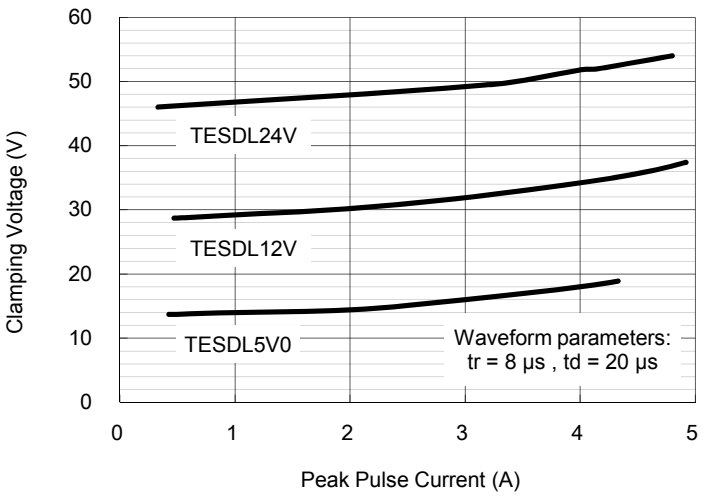
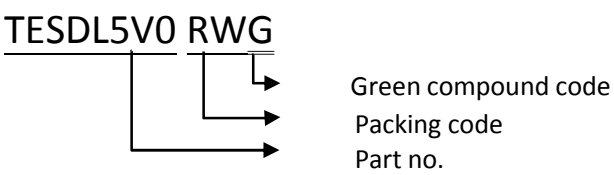


Fig. 5 Clamping Voltage VS. Peak Pulse Current



ORDER INFORMATION (EXAMPLE)



PACKAGE OUTLINE DIMENSIONS

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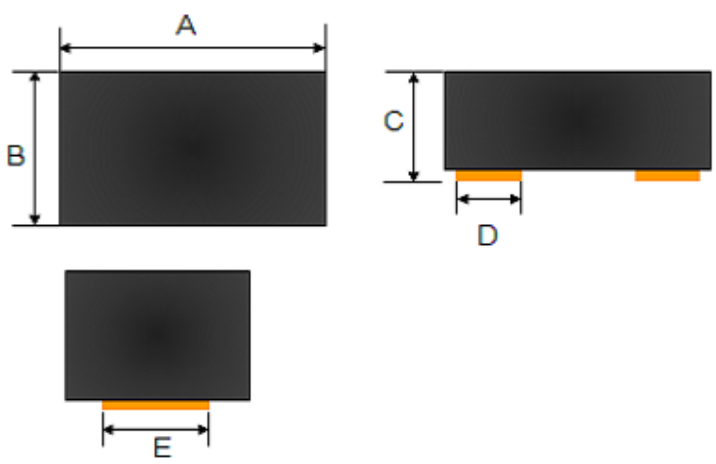
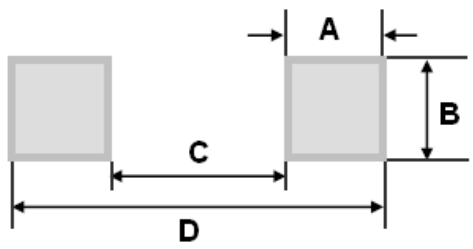


DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.40	2.60	0.094	0.102
B	1.10	1.30	0.043	0.051
C	0.70	0.90	0.028	0.035
D	0.50 (Typ.)		0.020 (Typ.)	
E	1.00 (Typ.)		0.040 (Typ.)	

SUGGEST PAD LAYOUT



DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
A	0.70	0.028
B	1.30	0.051
C	1.30	0.051
D	2.70	0.106

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

MARKING

Part No.	Marking
TESDL5V0	E05
TESDL12V	E12
TESDL24V	E24

APPLICATION INFROMATION

- Designed to protect one data, I/O, or power supply line
- Designed to protect sensitive electronics from damage or latch-up due to ESD
- Designed to replace multilayer varistors (MLVs) in portable applications
- Features large cross-sectional area junctions for conducting high transient currents
- Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- The combination of small size and high ESD surge capability makes them ideal for use in portable applications

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

- Good circuit board layout is critical for the suppression of ESD induced transients
- Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- Minimize the path length between the ESD Protection Diode and the protected line
- Minimize all conductive loops including power and ground loops
- The ESD transient return path to ground should be kept as short as possible
- Never run critical signals near board edges
- Use ground planes whenever possible

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