

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 175 \text{ mA}$  at 10 ns
- Low CMOS standby power
  - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3\text{V}$
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 54-Pin TSOP II and 48-Ball VFBGA packages

## Functional Description

The CY7C1069DV33 is a high performance CMOS Static RAM organized as 2,097,152 words by 8 bits.

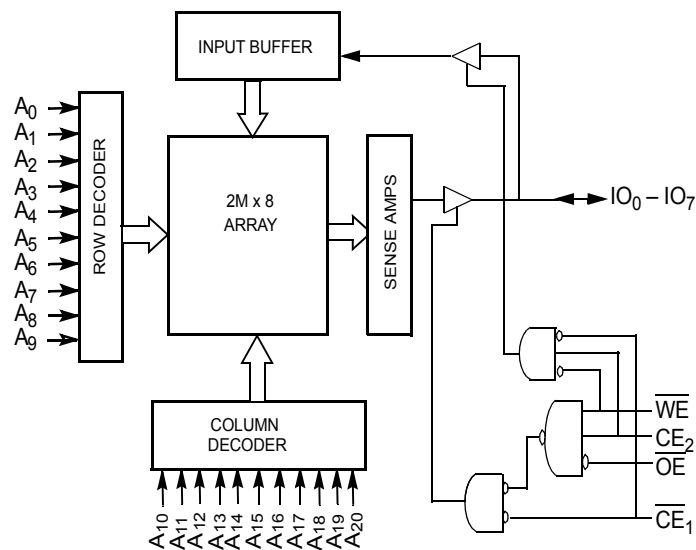
To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) input LOW. Data on the eight IO pins ( $IO_0$  through  $IO_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{20}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the IO pins. See Truth Table on page 8 for a complete description of Read and Write modes.

The input and output pins ( $IO_0$  through  $IO_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and WE LOW).

The CY7C1069DV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-Ball very fine pitch ball grid array (VFBGA) package.

## Logic Block Diagram



### Selection Guide

	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

### Pin Configuration

Figure 1. 54-Pin TSOP II (Top View) [1]

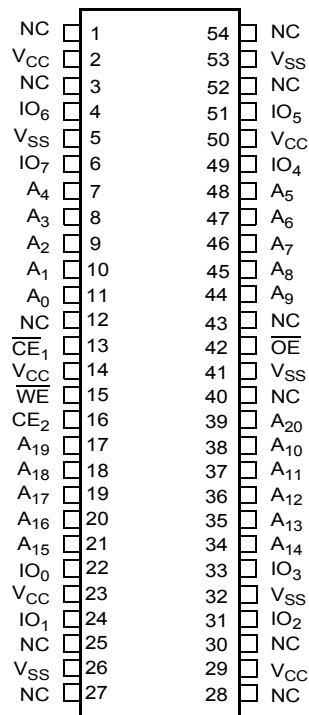
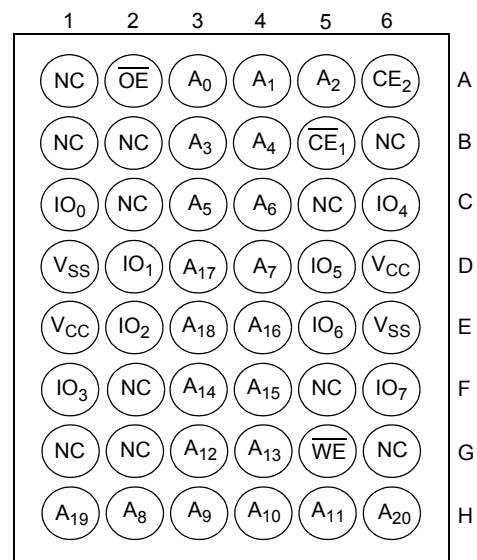


Figure 2. 48-Ball VFBGA (Top View) [1]



**Note**

- 1. NC pins are not connected on the die.

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> Relative to GND <sup>[2]</sup> ..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State <sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage <sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage.....>2001V (MIL-STD-883, Method 3015)
- Latch Up Current..... >200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	3.3V ± 0.3V

### DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , I <sub>OUT</sub> = 0 mA CMOS levels		175	mA
I <sub>SB1</sub>	Automatic CE Power Down Current — TTL Inputs	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30	mA
I <sub>SB2</sub>	Automatic CE Power Down Current — CMOS Inputs	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		25	mA

**Note**

2. V<sub>IL</sub> (min) = -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 2V for pulse durations of less than 20 ns.

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	6	8	pF
C <sub>OUT</sub>	IO Capacitance		8	10	pF

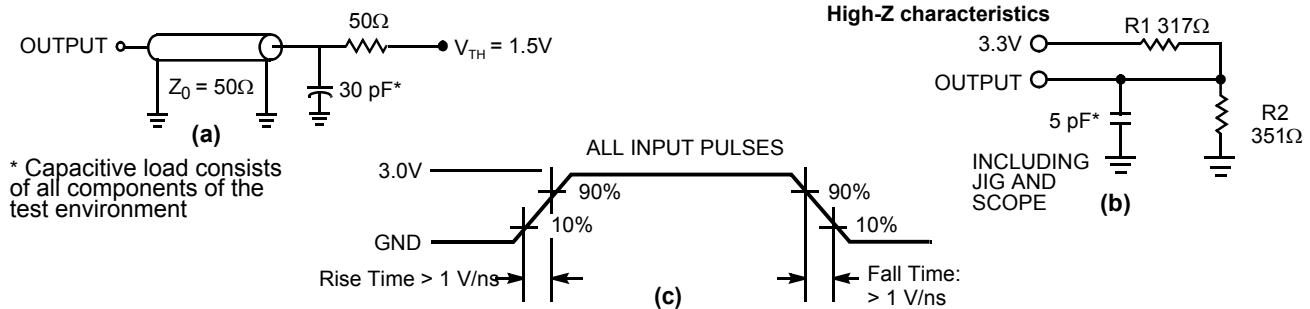
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	28.37	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		5.40	5.79	°C/W

## AC Test Loads and Waveforms

The AC test loads and waveform diagram follows. [3]



### Note

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V<sub>DD</sub> (3.0V). 100 μs (t<sub>power</sub>) after reaching the minimum operating V<sub>DD</sub>, normal SRAM operation begins including reduction in V<sub>DD</sub> to the data retention (V<sub>CDDR</sub>, 2.0V) voltage.

## AC Switching Characteristics

Over the Operating Range <sup>[4]</sup>

Parameter	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}$	$V_{\text{CC}}$ (Typical) to the First Access <sup>[5]</sup>	100		$\mu\text{s}$
$t_{\text{RC}}$	Read Cycle Time	10		ns
$t_{\text{AA}}$	Address to Data Valid		10	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3		ns
$t_{\text{ACE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Data Valid		10	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to Data Valid		5	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low Z	1		ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High Z <sup>[6]</sup>		5	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Low Z <sup>[6]</sup>	3		ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}_1$ HIGH/ $\text{CE}_2$ LOW to High Z <sup>[6]</sup>		5	ns
$t_{\text{PU}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Power Up <sup>[7]</sup>	0		ns
$t_{\text{PD}}$	$\overline{\text{CE}}_1$ HIGH/ $\text{CE}_2$ LOW to Power Down <sup>[7]</sup>		10	ns
<b>Write Cycle <sup>[8, 9]</sup></b>				
$t_{\text{WC}}$	Write Cycle Time	10		ns
$t_{\text{SCE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Write End	7		ns
$t_{\text{AW}}$	Address Setup to Write End	7		ns
$t_{\text{HA}}$	Address Hold from Write End	0		ns
$t_{\text{SA}}$	Address Setup to Write Start	0		ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ Pulse Width	7		ns
$t_{\text{SD}}$	Data Setup to Write End	5.5		ns
$t_{\text{HD}}$	Data Hold from Write End	0		ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>	3		ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High Z <sup>[6]</sup>		5	ns

### Notes

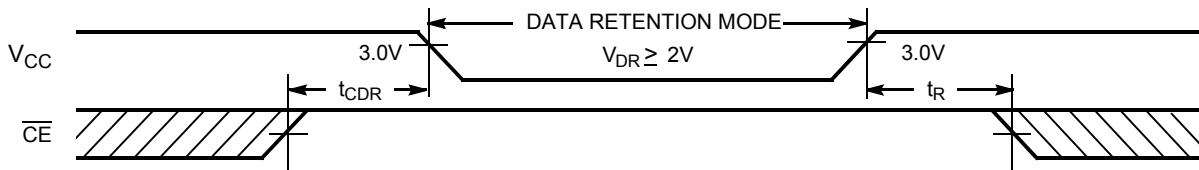
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading shown in part a) of [AC Test Loads and Waveforms](#), unless specified otherwise.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ , and  $t_{\text{LZWE}}$  are specified with a load capacitance of 5 pF as in (b) of [AC Test Loads and Waveforms](#). Transition is measured  $\pm 200$  mV from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ .  $\overline{\text{CE}}_1$  and  $\overline{\text{WE}}$  are LOW along with  $\text{CE}_2$  HIGH to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 2V, \overline{CE}_1 \geq V_{CC} - 0.2V,$ $CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			25	mA
$t_{CDR}^{[10]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[11]}$	Operation Recovery Time		$t_{RC}$			ns

### Data Retention Waveform



### Switching Waveforms

Figure 3. Read Cycle No. 1 [12, 13]

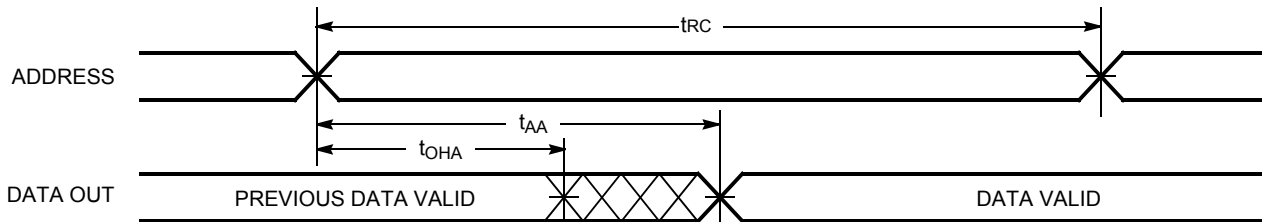
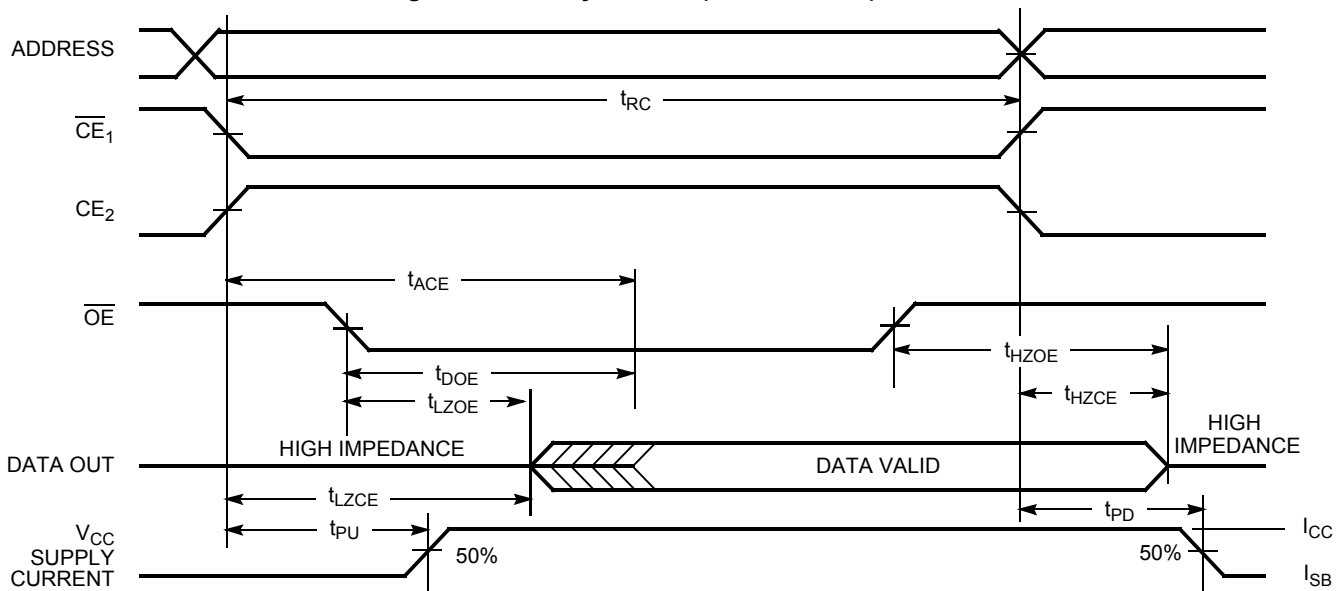


Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [13, 15]



**Notes**

- 10. Tested initially and after any design or process changes that may affect these parameters.
- 11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$ .
- 12. The device is continuously selected.  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 13.  $\overline{WE}$  is HIGH for read cycle.
- 14. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [15, 16, 17]

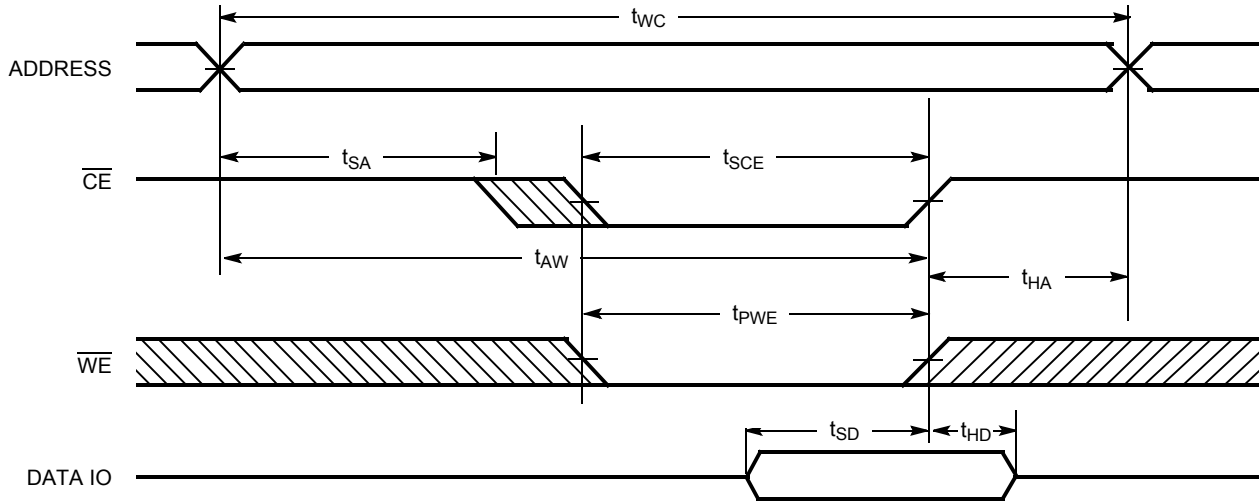
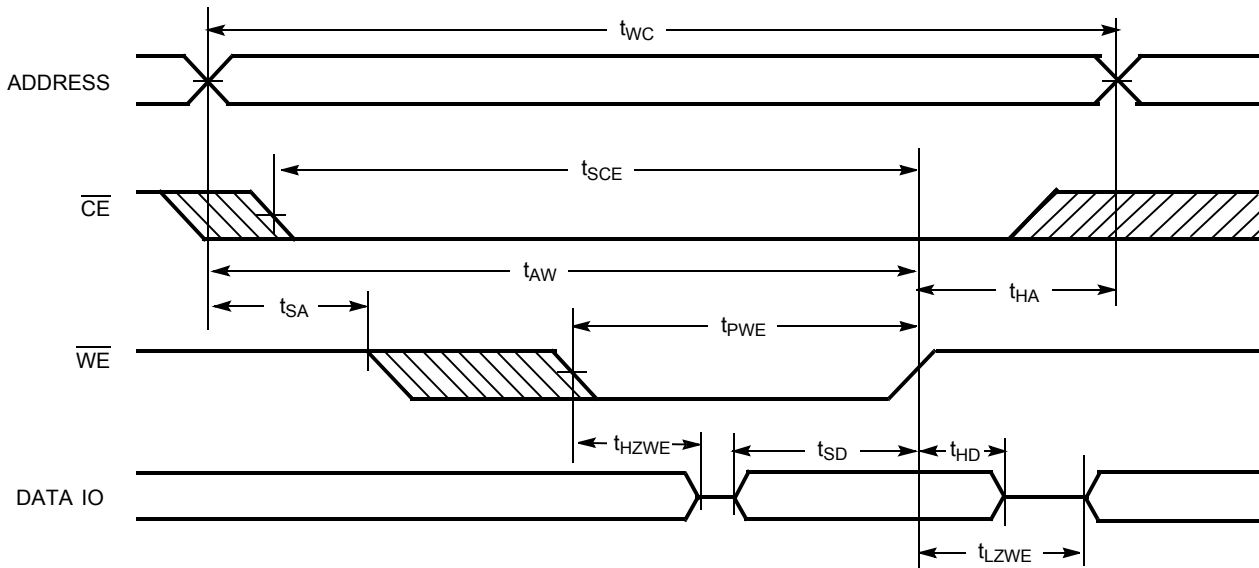


Figure 6. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [15, 16, 17]



Notes

- 15.  $\overline{\text{CE}}$  is a shorthand combination of both  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  combined. It is active LOW.
- 16. Data IO is high impedance if  $\text{OE} = V_{IH}$ .
- 17. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

Truth Table

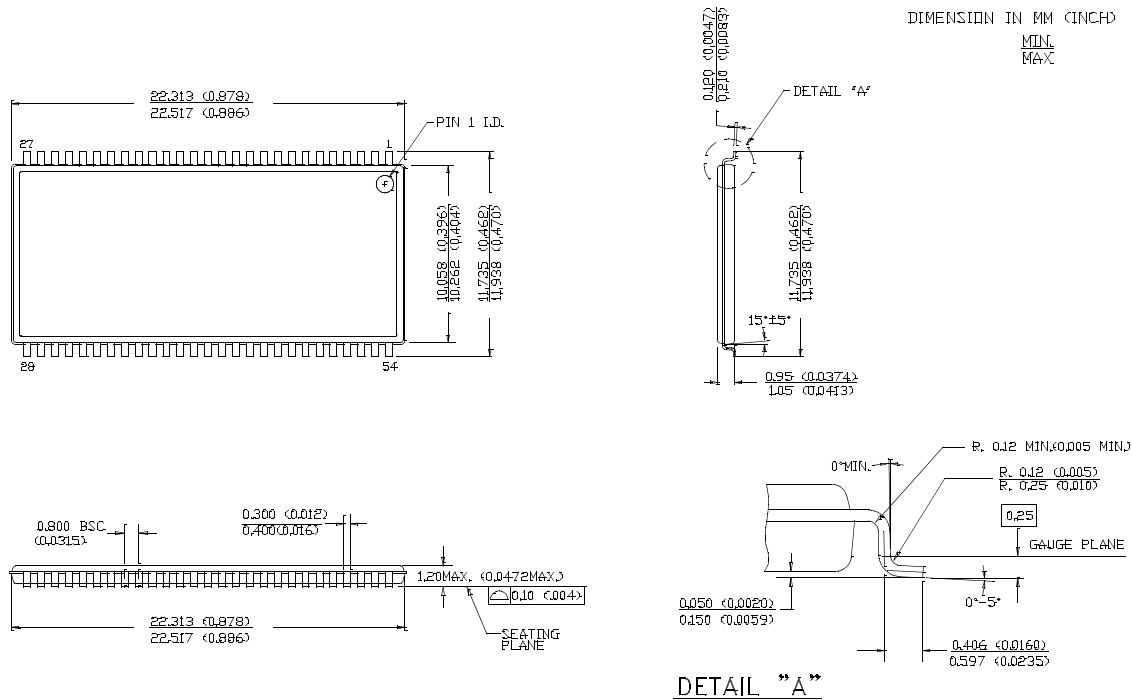
$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	$IO_0 - IO_7$	Mode	Power
H	X	X	X	High Z	Power Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power Down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read All Bits	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write All Bits	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1069DV33-10ZSXI	51-85160	54-Pin TSOP II (Pb-Free)	Industrial
	CY7C1069DV33-10BVXI	51-85178	48-Ball VFBGA (8 × 9.5 × 1 mm) (Pb-Free)	

Package Diagrams

Figure 7. 54-Pin TSOP Type II

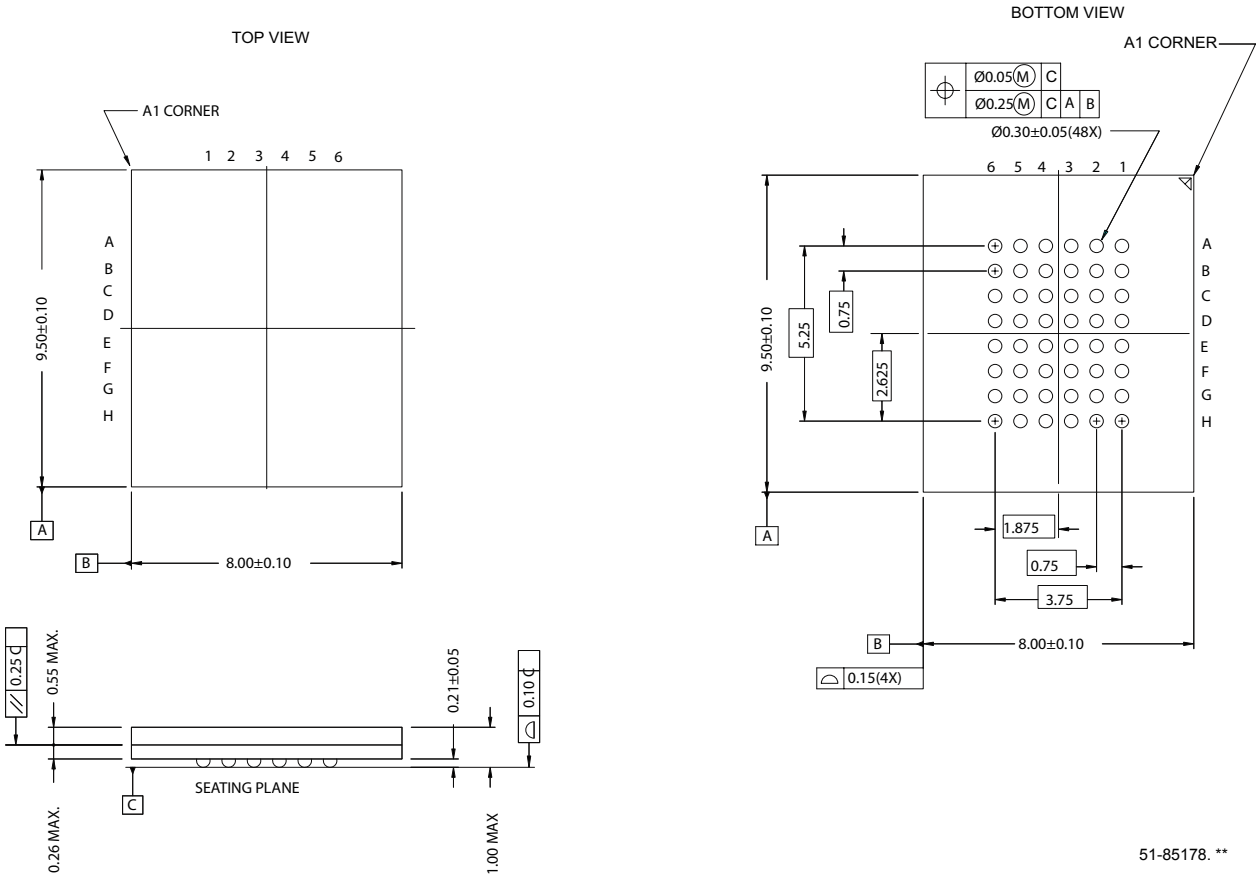


51-85160-\*\*



Package Diagrams (continued)

Figure 8. 48-Ball VFBGA (8 x 9.5 x 1 mm)



51-85178. \*\*

Document History Page

Document Title: CY7C1069DV33 16-Mbit (2M x 8) Static RAM				
Document Number: 38-05478				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance datasheet for C9 IPP
*A	233748	See ECN	RKF	Modified AC, DC parameters as per EROS (Specification 01-2165) Pb-free Offering in the Ordering Information
*B	469420	See ECN	NXR	Converted from Advance Information to Preliminary Removed -8 and -12 speed bins from product offering Removed Commercial Operating Range Changed 2G Ball of FBGA and pin 40 of TSOPII from DNU to NC Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed I <sub>CC(Max)</sub> from 220 mA to 100 mA Changed I <sub>SB1(Max)</sub> from 70 mA to 30 mA Changed I <sub>SB2(Max)</sub> from 40 mA to 25 mA Specified the Overshoot specification in footnote 1 Added Data Retention Characteristics table on page 5 Updated the 48-pin FBGA package Updated the Ordering Information table.
*C	499604	See ECN	NXR	Added note 1 for NC pins Updated Test Condition for I <sub>CC</sub> in DC Electrical Characteristics table Updated the 48-Ball FBGA Package
*D	1462585	See ECN	VKN/AESA	Converted from preliminary to final Changed I <sub>CC</sub> spec from 125 mA to 175 mA Updated thermal specs

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