CYDM064B16
CYDM128B16
CYDM256B16

1.8 V, 4K/8K/16K × 16 MoBL® Dual-Port Static RAM

Features

- True dual ported memory cells that allow simultaneous access of the same memory location
- 4, 8, or 16K × 16 organization
- Ultra Low operating power
  - Active: ICC = 15 mA (typical) at 55 ns
  - Standby: I_{SB3} = 2 μA (typical)
- Small footprint: available in a 6 × 6 mm 100-pin Pb-free vfBGA
- Port independent 1.8 V, 2.5 V, and 3.0 V I/Os
- Full asynchronous operation
- Automatic power down
- Pin select for Master or Slave
- Expandable data bus to 32-bits with Master or Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- Input read registers and output drive registers
- INT flag for port-to-port communication
- Separate upper-byte and lower-byte control
- Industrial temperature ranges

Functional Description

The CYDM256B16, CYDM128B16, and CYDM064B16 are low power CMOS 4K, 8K,16K × 16 dual-port static RAMs. Arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided that permit independent, asynchronous access for reads and writes to any location in memory. The devices can be used as standalone 16-bit dual-port static RAMs or multiple devices can be combined to function as a 32-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 32-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor or multi-processor designs, communications status buffering, and dual-port video or graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ indicates that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems through a mail box. The semaphores are used to pass a flag or token, from one port to the other, to indicate that a shared resource is in use. The semaphore logic consists of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by a Chip Enable ($\overline{CE}$) pin.

The CYDM256B16, CYDM128B16, CYDM064B16 are available in 100-ball 0.5 mm pitch Ball Grid Array (BGA) packages.

Selection Guide for V_{CC} = 1.8V

Parameter	CYDM256B16/CYDM128B16/CYDM064B16	Unit
	(-55)	
Port I/O Voltages (P1–P2)	1.8 V–1.8 V	V
Maximum Access Time	55	ns
Typical Operating Current	15	mA
Typical Standby Current for I_{SB1}	2	µA
Typical Standby Current for I_{SB3}	2	µA

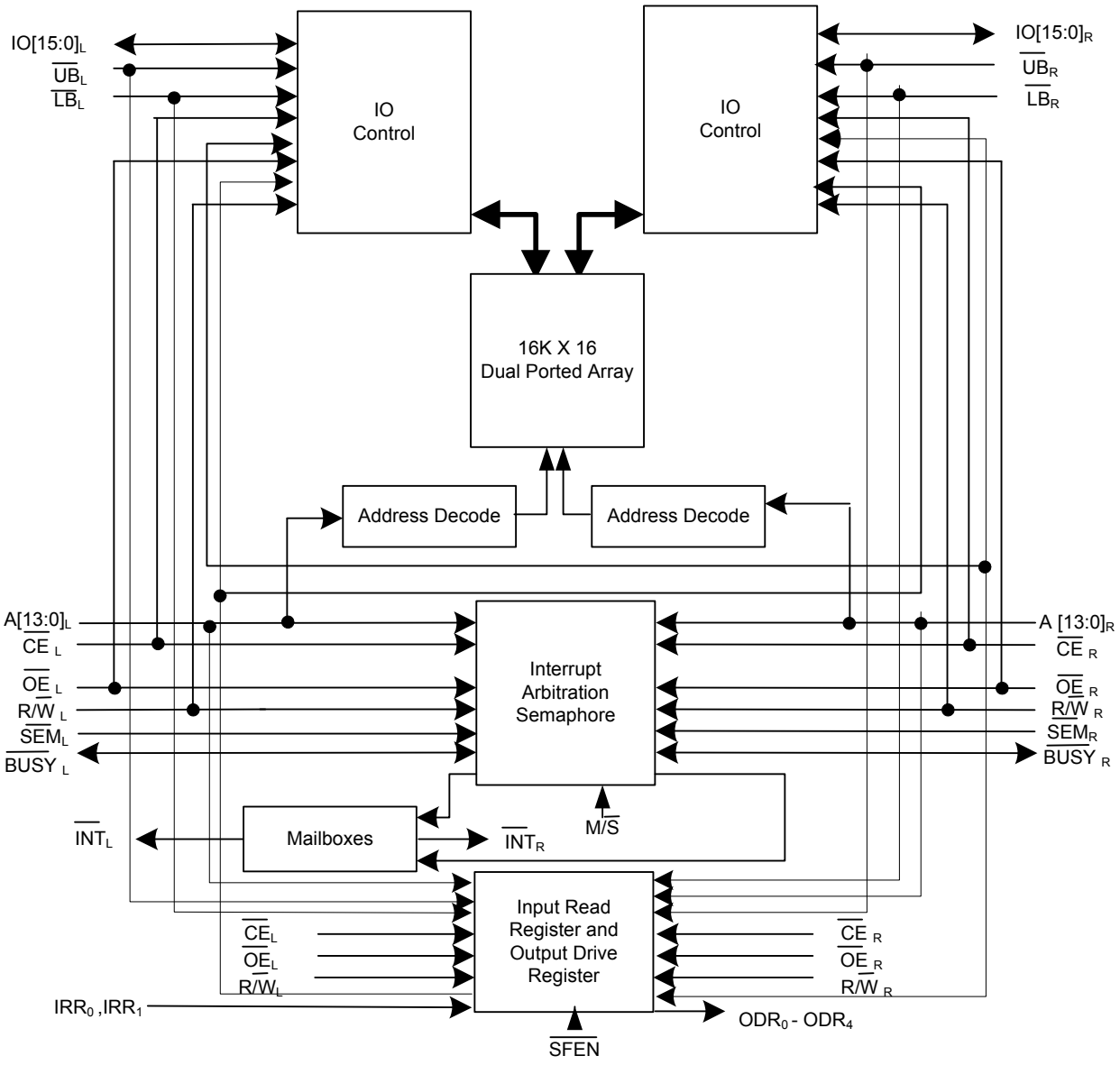
Selection Guide for V_{CC} = 2.5 V

Parameter	CYDM256B16/CYDM128B16/CYDM064B16	Unit
	(-55)	
Port I/O Voltages (P1–P2)	2.5 V–2.5 V	V
Maximum Access Time	55	ns
Typical Operating Current	28	mA
Typical Standby Current for I_{SB1}	6	µA
Typical Standby Current for I_{SB3}	4	µA

Selection Guide for V_{CC} = 3.0 V

Parameter	CYDM256B16/CYDM128B16/CYDM064B16	Unit
	(-55)	
Port I/O Voltages (P1–P2)	3.0 V–3.0 V	V
Maximum Access Time	55	ns
Typical Operating Current	42	mA
Typical Standby Current for I_{SB1}	7	µA
Typical Standby Current for I_{SB3}	6	µA

Logic Block Diagram [1, 2]



Notes
1. A_0–A_{11} for 4K devices; A_0–A_{12} for 8K devices; A_0–A_{13} for 16K devices.
2. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

Contents

Pinouts

Figure 1. Ball Diagram - 100-ball 0.5 mm Pitch BGA (Top View) [3, 4, 5, 6, 7]

CYDM064B16/CYDM128B16/CYDM256B16

	1	2	3	4	5	6	7	8	9	10	
A	A_{5R}	A_{8R}	A_{11R}	UB_R	V_{SS}	SEM_R	IO_{15R}	IO_{12R}	IO_{10R}	V_{SS}	**A**
B	A_{3R}	A_{4R}	A_{7R}	A_{9R}	CE_R	R/W_R	OE_R	V_{DDIOR}	IO_{9R}	IO_{6R}	**B**
C	A_{0R}	A_{1R}	A_{2R}	A_{6R}	LB_R	IRR1[6]	IO_{14R}	IO_{11R}	IO_{7R}	V_{SS}	**C**
D	ODR4	ODR2	$BUSY_R$	INT_R	A_{10R}	A_{12R}[3]	IO_{13R}	IO_{8R}	IO_{5R}	IO_{2R}	**D**
E	V_{SS}	M/S	ODR3	INT_L	V_{SS}	V_{SS}	IO_{4R}	V_{DDIOR}	IO_{1R}	V_{SS}	**E**
F	SFEN	ODR1	$BUSY_L$	A_{1L}	V_{CC}	V_{SS}	IO_{3R}	IO_{0R}	IO_{15L}	V_{DDIOL}	**F**
G	ODR0	A_{2L}	A_{5L}	A_{12L}[3]	OE_L	IO_{3L}	IO_{11L}	IO_{12L}	IO_{14L}	IO_{13L}	**G**
H	A_{0L}	A_{4L}	A_{9L}	LB_L	CE_L	IO_{1L}	V_{DDIOL}	NC[7]	NC[7]	IO_{10L}	**H**
J	A_{3L}	A_{7L}	A_{10L}	IRR0[5]	V_{CC}	V_{SS}	IO_{4L}	IO_{6L}	IO_{8L}	IO_{9L}	**J**
K	A_{6L}	A_{8L}	A_{11L}	UB_L	SEM_L	R/W_L	IO_{0L}	IO_{2L}	IO_{5L}	IO_{7L}	**K**
	1	2	3	4	5	6	7	8	9	10	

Notes
3. A12L and A12R are NC pins for CYDM064B16.
4. IRR functionality is not supported for the CYDM256B16 device.
5. This pin is A13L for CYDM256B16 device.
6. This pin is A13R for CYDM256B16 device.
7. Leave this pin unconnected. No trace or power component can be connected to this pin.

Pin Definitions

100-ball 0.5 mm pitch BGA (CYDM064B16/CYDM128B16/CYDM256B16)

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read or Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L}–A_{13L}	A_{0R}–A_{13R}	Address (A_0–A_{11} for 4K devices; A_0–A_{12} for 8K devices; A_0–A_{13} for 16K devices)
IO_{0L}–IO_{15L}	IO_{0R}–IO_{15R}	Data Bus Input or Output for x16 devices
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select (IO_8–IO_{15})
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select (IO_0–IO_7)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
IRR0, IRR1		Input Read Register for CYDM064B16 and CYDM128B16 A13L and A13R for CYDM256B16.
ODR0-ODR4		Output Drive Register. These outputs are Open Drain.
$\overline{SFEN}$		Special Function Enable
$M/\overline{S}$		Master or Slave Select
V_{CC}		Core Power
GND		Ground
V_{DDIOL}		Left Port I/O Voltage
V_{DDIOR}		Right Port I/O Voltage
NC		No Connect. Leave this pin Unconnected.

Functional Overview

Power Supply

The core voltage (V_{CC}) can be 1.8 V, 2.5 V, or 3.0 V, as long as it is lower than or equal to the I/O voltage.

Each port can operate on independent I/O voltages. This is determined by what is connected to the V_{DDIOL} and V_{DDIOR} pins. The supported I/O standards are 1.8 V or 2.5 V LVCMOS and 3.0V LVTTL.

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W to guarantee a valid write. A write operation is controlled by either the R/W pin (see Figure 6 on page 24) or the $\overline{CE}$ pin (see Figure 7 on page 24). Required inputs for noncontention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output. Otherwise, the data read is not deterministic. Data is valid on the port t_{DDD} after the data is presented on the other port.

Table 1. NonContending Read/Write

Inputs						Outputs		Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	IO_8–IO_{15}	IO_0–IO_7	
H	X	X	X	X	H	High Z	High Z	Deselected: Power down
X	X	X	H	H	H	High Z	High Z	Deselected: Power down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	⎍	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	⎍	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data is available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CYDM064B16, 1FFF for the CYDM128B16, 3FFF for the CYDM256B16) is the mailbox for the right port and the second-highest memory location (FFE for the CYDM064B16, 1FFE for the CYDM128B16, 3FFE for the CYDM256B16) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user-defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin. On power up, an initialization program must be run and the interrupts for both ports must be read to reset them.

The operation of the interrupts and their interaction with Busy are summarized in Table 2.

Table 2. Interrupt Operation Example (Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH) [8]

Function	Left Port					Right Port				
	$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-13L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-13R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	3FFF[11]	X	X	X	X	X	L[10]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	3FFF[11]	H[9]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[9]	L	L	X	3FFE[11]	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	3FFE[11]	H[10]	X	X	X	X	X

Busy

The CYDM256B16, CYDM128B16, and CYDM064B16 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both port $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location. However, which port gets this permission cannot be predicted. $\overline{BUSY}$ is asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

An M/$\overline{S}$ pin is provided to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, as a result, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Input Read Register

The Input Read Register (IRR) captures the status of two external input devices that are connected to the Input Read pins.

The contents of the IRR read from address x0000 from either port. During reads from the IRR, DQ0 and DQ1 are valid bits and DQ<15:2> are don't care. Writes to address x0000 are not allowed from either port.

Address x0000 is not available for standard memory accesses when $\overline{SFEN}$ = V_{IL}. When $\overline{SFEN}$ = V_{IH}, address x0000 is available for memory accesses.

The inputs are 1.8V/2.5V LVCMOS or 3.0V LVTTL, depending on the core voltage supply (V_{CC}). Refer to Table 3 on page 8 for Input Read Register operation.

IRR is not available in the CYDM256B16, because the IRR pins are used as extra address pins A_{13L} and A_{13R}.

Table 3. Input Read Register Operation[12, 13]

$\overline{SFEN}$	$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	ADDR	IO_0–IO_1	IO_2–IO_{15}	Mode
H	L	H	L	L	L	x0000-Max	VALID[14]	VALID[14]	Standard Memory Access
L	L	H	L	X	L	x0000	VALID[15]	X	IRR Read

Notes
8. See Interrupts Functional Description for specific highest memory locations by device.
9. If $\overline{BUSY}_R$ = L, then no change.
10. If $\overline{BUSY}_L$ = L, then no change.
11. See section Functional Description on page 1 for specific addresses by device.
12. $\overline{SFEN}$ = V_{IL} for IRR reads.
13. $\overline{SFEN}$ active when either $\overline{CE}_L$ = V_{IL} or $\overline{CE}_R$ = V_{IL}. It is inactive when $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}.
14. $\overline{UB}$ or $\overline{LB}$ = V_{IL}. If $\overline{LB}$ = V_{IL}, then DQ<7:0> are valid. If $\overline{UB}$ = V_{IL} then DQ<15:8> are valid.
15. $\overline{LB}$ must be active ($\overline{LB}$ = V_{IL}) for these bits to be valid.

Output Drive Register

The Output Drive Register (ODR) determines the state of up to five external binary state devices by providing a path to V_{SS} for the external circuit. These outputs are Open Drain.

The five external devices can operate at different voltages ($1.5\ V \le V_{DDIO} \le 3.5\ V$) but the combined current cannot exceed 40 mA (8 mA max for each external device). The status of the ODR bits are set using standard write accesses from either port to address x0001 with a “1” corresponding to on and “0” corresponding to off.

The status of the ODR bits can be read with a standard read access to address x0001. When $\overline{SFEN} = V_{IL}$, the ODR is active and address x0001 is not available for memory accesses. When $\overline{SFEN} = V_{IH}$, the ODR is inactive and address x0001 can be used for standard accesses.

During reads and writes to ODR DQ<4:0> are valid and DQ<15:5> are don’t care. Refer to Table 4 for Output Drive Register operation.

Table 4. Output Drive Register [16]

$\overline{SFEN}$	$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	ADDR	IO_0–IO_4	IO_5–IO_{15}	Mode
H	L	H	X[17]	L[18]	L[18]	x0000-Max	VALID[18]	VALID[18]	Standard Memory Access
L	L	L	X	X	L	x0001	VALID[19]	X	ODR Write[16, 20]
L	L	H	L	X	L	x0001	VALID[19]	X	ODR Read[16]

Semaphore Operation

The CYDM256B16, CYDM128B16, and CYDM064B16 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port is successful (reads a zero), it assumes control of the shared resource. Otherwise (reads a one), it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only IO_0 is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port requests the semaphore (written a zero) while the left port has control, the right port immediately owns the semaphore as soon as the left port releases it. Table 5 shows sample semaphore operations.

Table 5. Semaphore Operation Example

Function	IO_0–IO_{15} Left	IO_0–IO_{15} Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore.
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore.
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes
16. $\overline{SFEN} = V_{IL}$ for ODR reads and writes.
17. Output enable must be low ($\overline{OE} = V_{IL}$) during reads for valid data to be output.
18. $\overline{UB}$ or $\overline{LB} = V_{IL}$. If $\overline{LB} = V_{IL}$, then DQ<7:0> are valid. If $\overline{UB} = V_{IL}$ then DQ<15:8> are valid.
19. $\overline{LB}$ must be active ($\overline{LB} = V_{IL}$) for these bits to be valid.
20. During ODR writes data are also written to the memory.

When reading a semaphore, all sixteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore. On power up, both ports must write “1” to all eight semaphores.

Architecture

The CYDM256B16, CYDM128B16, and CYDM064B16 consist of an array of 4K, 8K, or 16K words of 16 dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes or reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two Interrupt ($\overline{INT}$) pins can be used for port-to-port communication. Two Semaphore ($\overline{SEM}$) control pins are used to allocate shared resources. With the M/$\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The devices also have an automatic power down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Maximum Ratings

Exceeding maximum ratings[19] may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +3.3V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[20] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 90 mA

Static Discharge Voltage ..... > 2000V

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	1.8 V ± 100 mV 2.5 V ± 100 mV 3.0 V ± 300 mV
Industrial	–40 °C to +85 °C	1.8 V ± 100 mV 2.5 V ± 100 mV 3.0 V ± 300 mV

Notes
19. The voltage on any input or I/O pin can not exceed the power pin during power up.
20. Pulse width < 20 ns.

Electrical Characteristics for V_{CC} = 1.8 V

Over the Operating Range

Parameter	Description	CYDM256B16/CYDM128B16/CYDM064B16					Unit
		-55					
		P1 I/O Voltage	P2 I/O Voltage	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (I_{OH} = –100 µA)	1.8 V (any port)		V_{DDIO} – 0.2	–	–	V
	Output HIGH Voltage (I_{OH} = –2 mA)	2.5 V (any port)		2.0	–	–	V
	Output HIGH Voltage (I_{OH} = –2 mA)	3.0 V (any port)		2.1	–	–	V
V_{OL}	Output LOW Voltage (I_{OL} = 100 µA)	1.8 V (any port)		–	–	0.2	V
	Output HIGH Voltage (I_{OL} = 2 mA)	2.5 V (any port)		–	–	0.4	V
	Output HIGH Voltage (I_{OL} = 2 mA)	3.0 V (any port)		–	–	0.4	V
V_{OL} ODR	ODR Output LOW Voltage (I_{OL} = 8 mA)	1.8 V (any port)		–	–	0.2	V
		2.5 V (any port)		–	–	0.2	V
		3.0 V (any port)		–	–	0.2	V
V_{IH}	Input HIGH Voltage	1.8 V (any port)		1.2	–	V_{DDIO} + 0.2	V
		2.5 V (any port)		1.7	–	V_{DDIO} + 0.3	V
		3.0 V (any port)		2.0	–	V_{DDIO} + 0.2	V
V_{IL}	Input LOW Voltage	1.8 V (any port)		–0.2	–	0.4	V
		2.5 V (any port)		–0.3	–	0.6	V
		3.0 V (any port)		–0.2	–	0.7	V
I_{OZ}	Output Leakage Current	1.8 V	1.8 V	–1	–	1	µA
		2.5 V	2.5 V	–1	–	1	µA
		3.0 V	3.0 V	–1	–	1	µA
I_{CEX} ODR	ODR Output Leakage Current. V_{OUT} = V_{DDIO}	1.8 V	1.8 V	–1	–	1	µA
		2.5 V	2.5 V	–1	–	1	µA
		3.0 V	3.0 V	–1	–	1	µA
I_{IX}	Input Leakage Current	1.8 V	1.8 V	–1	–	1	µA
		2.5 V	2.5 V	–1	–	1	µA
		3.0 V	3.0 V	–1	–	1	µA

Electrical Characteristics for V_{CC} = 1.8 V (continued)

Over the Operating Range

Parameter	Description		CYDM256B16/CYDM128B16/CYDM064B16					Unit
			-55					
			P1 I/O Voltage	P2 I/O Voltage	Min	Typ	Max	
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA), Outputs Disabled	Industrial	1.8 V	1.8 V	–	15	25	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, $SEM_L = SEM_R = V_{CC} - 0.2$, $f = f_{MAX}$	Industrial	1.8 V	1.8 V		2	6	µA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$	Industrial	1.8 V	1.8 V		8.5	14	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, SEM_L and $SEM_R > V_{CC} - 0.2$, $f = 0$	Industrial	1.8 V	1.8 V		2	6	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$[21]	Industrial	1.8 V	1.8 V		8.5	14	mA

Notes
21. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at $f = 1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Electrical Characteristics for V_{CC} = 2.5 V

Over the Operating Range

Parameter	Description		CYDM256B16, CYDM128B16, CYDM064B16					Unit
			-55					
			P1 I/O Voltage	P2 I/O Voltage	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (I_{OH} = –2 mA)		2.5 V (any port)		2.0	–	–	V
			3.0 V (any port)		2.1	–	–	V
V_{OL}	Output LOW Voltage (I_{OL} = 2 mA)		2.5 V (any port)		–	–	0.4	V
			3.0 V (any port)		–	–	0.4	V
V_{OL} ODR	ODR Output LOW Voltage (I_{OL} = 8 mA)		2.5 V (any port)		–	–	0.2	V
			3.0 V (any port)		–	–	0.2	V
V_{IH}	Input HIGH Voltage		2.5 V (any port)		1.7	–	V_{DDIO} + 0.3	V
			3.0 V (any port)		2.0	–	V_{DDIO} + 0.2	V
V_{IL}	Input LOW Voltage		2.5 V (any port)		–0.3	–	0.6	V
			3.0 V (any port)		–0.2	–	0.7	V
I_{OZ}	Output Leakage Current		2.5 V	2.5 V	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	µA
I_{CEX} ODR	ODR Output Leakage Current. V_{OUT} = V_{CC}		2.5 V	2.5 V	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	µA
I_{IX}	Input Leakage Current		2.5 V	2.5 V	–1	–	1	µA
			3.0 V	3.0 V	–1	–	1	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA), Outputs Disabled	Industrial	2.5 V	2.5 V	–	28	40	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, $SEM_L = SEM_R = V_{CC} - 0.2$, f = f_{MAX}	Industrial	2.5 V	2.5 V	–	6	8	µA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Industrial	2.5 V	2.5 V		18	25	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$, SEM_L and $SEM_R > V_{CC} - 0.2$, f = 0	Industrial	2.5 V	2.5 V		4	6	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}[22]	Industrial	2.5 V	2.5 V		18	25	mA

Notes
22. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Electrical Characteristics for V_{CC} = 3.0 V

Over the Operating Range

Parameter	Description		CYDM256B16/CYDM128B16/CYDM064B16					Unit
			-55					
			P1 I/O Voltage	P2 I/O Voltage	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (I_{OH} = –2 mA)		3.0 V (any port)		2.1	–	–	V
V_{OL}	Output LOW Voltage (I_{OL} = 2 mA)		3.0 V (any port)		–	–	0.4	V
V_{OL} ODR	ODR Output LOW Voltage (I_{OL} = 8 mA)		3.0 V (any port)		–	–	0.2	V
V_{IH}	Input HIGH Voltage		3.0 V (any port)		2.0	–	V_{DDIO} + 0.2	V
V_{IL}	Input LOW Voltage		3.0 V (any port)		–0.2	–	0.7	V
I_{OZ}	Output Leakage Current		3.0 V	3.0 V	–1	–	1	µA
I_{CEX} ODR	ODR Output Leakage Current. V_{OUT} = V_{CC}		3.0 V	3.0 V	–1	–	1	µA
I_{IX}	Input Leakage Current		3.0 V	3.0 V	–1	–	1	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA), Outputs Disabled	Industrial	3.0 V	3.0 V	–	42	60	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0.2, SEM_L = SEM_R = V_{CC} – 0.2, f = f_{MAX}	Industrial	3.0 V	3.0 V		7	10	µA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Industrial	3.0 V	3.0 V		25	35	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0.2, SEM_L and $SEM_R > V_{CC}$ – 0.2, f = 0	Industrial	3.0 V	3.0 V		6	8	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[23]	Industrial	3.0 V	3.0 V		25	35	mA

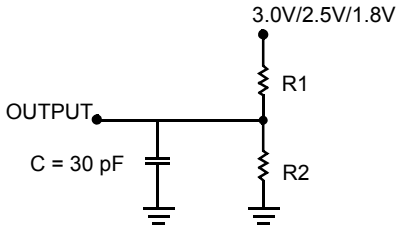
Notes
23. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance

Parameter [24]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.0 V	9	pF
C_{OUT}	Output capacitance		10	pF

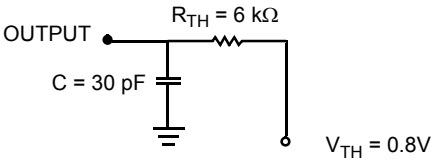
AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



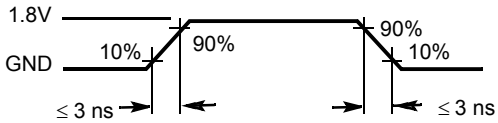
(a) Normal Load

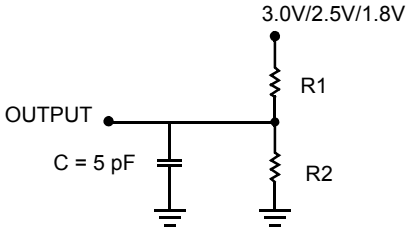
	3.0V/2.5V	1.8V
R1	1022Ω	13500Ω
R2	792Ω	10800Ω



(b) Thévenin Equivalent (Load 1)

ALL INPUT PULSES





(c) Three-State Delay (Load 2)

(Used for t_{LZ}, t_{HZ}, t_{HZWE}, and t_{LZWE} including scope and jig)

Note
24. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics for V_{CC} = 1.8 V

Over the Operating Range

Parameter [23]	Description	CYDM256B16/CYDM128B16/CYDM064B16		Unit
		-55		
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55	–	ns
t_{AA}	Address to Data Valid	–	55	ns
t_{OHA}	Output Hold From Address Change	5	–	ns
t_{ACE}[24]	$\overline{CE}$ LOW to Data Valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	30	ns
t_{LZOE}[25, 26, 27]	$\overline{OE}$ Low to Low Z	5	–	ns
t_{HZOE}[25, 26, 27]	$\overline{OE}$ HIGH to High Z	–	25	ns
t_{LZCE}[25, 26, 27]	$\overline{CE}$ LOW to Low Z	5	–	ns
t_{HZCE}[25, 26, 27]	$\overline{CE}$ HIGH to High Z	–	25	ns
t_{PU}[27]	$\overline{CE}$ LOW to Power up	0	–	ns
t_{PD}[27]	$\overline{CE}$ HIGH to Power down	–	55	ns
t_{ABE}[24]	Byte Enable Access Time	–	55	ns
Write Cycle				
t_{WC}	Write Cycle Time	55	–	ns
t_{SCE}[24]	$\overline{CE}$ LOW to Write End	45	–	ns
t_{AW}	Address Valid to Write End	45	–	ns
t_{HA}	Address Hold From Write End	0	–	ns
t_{SA}[24]	Address Setup to Write Start	0	–	ns
t_{PWE}	Write Pulse Width	40	–	ns
t_{SD}	Data Setup to Write End	30	–	ns
t_{HD}	Data Hold From Write End	0	–	ns
t_{HZWE}[26, 27]	R/$\overline{W}$ LOW to High Z	–	25	ns
t_{LZWE}[26, 27]	R/$\overline{W}$ HIGH to Low Z	0	–	ns
t_{WDD}[28]	Write Pulse to Data Delay	–	80	ns
t_{DDD}[28]	Write Data Valid to Read Data Valid	–	80	ns

Notes
23. Test conditions assume signal transition time of 3 ns or less, timing reference levels of V_{CC}/2, input pulse levels of 0 to V_{CC}, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
24. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
25. At any temperature and voltage condition for any device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
26. Test conditions used are Load 3.
27. This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
28. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

Switching Characteristics for V_{CC} = 1.8 V (continued)

Over the Operating Range

Parameter [23]	Description	CYDM256B16/CYDM128B16/CYDM064B16		Unit
		-55		
		Min	Max	
Busy Timing[29]				
t_{BLA}	$\overline{BUSY}$ LOW from Address Match	–	45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch	–	45	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	45	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	45	ns
t_{PS}[30]	Port Setup for Priority	5	–	ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	35	–	ns
t_{BDD}[31]	$\overline{BUSY}$ HIGH to Data Valid	–	40	ns
Interrupt Timing[29]				
t_{INS}	$\overline{INT}$ Set Time	–	45	ns
t_{INR}	$\overline{INT}$ Reset Time	–	45	ns
Semaphore Timing				
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	ns
t_{SWRD}	SEM Flag Write to Read Time	10	–	ns
t_{SPS}	SEM Flag Contention Window	10	–	ns
t_{SAA}	SEM Address Access Time	–	55	ns

Notes
29. Test conditions used are Load 2.
30. Add 2 ns to this parameter if V_{CC} and V_{DDIOR} are <1.8 V, and V_{DDIOL} is >2.5 V at temperature <0 °C.
31. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Switching Characteristics for V_{CC} = 2.5 V

Over the Operating Range

Parameter	Description	CYDM256B16/CYDM128B16/CYDM064B16		Unit
		-55		
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55	–	ns
t_{AA}	Address to Data Valid	–	55	ns
t_{OHA}	Output Hold From Address Change	5	–	ns
t_{ACE}[32]	$\overline{CE}$ LOW to Data Valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	30	ns
t_{LZOE}[33, 34, 35]	$\overline{OE}$ Low to Low Z	2	–	ns
t_{HZOE}[33, 34, 35]	$\overline{OE}$ HIGH to High Z	–	25	ns
t_{LZCE}[33, 34, 35]	$\overline{CE}$ LOW to Low Z	2	–	ns
t_{HZCE}[33, 34, 35]	$\overline{CE}$ HIGH to High Z	–	25	ns
t_{PU}[35]	$\overline{CE}$ LOW to Power up	0	–	ns
t_{PD}[35]	$\overline{CE}$ HIGH to Power down	–	55	ns
t_{ABE}[32]	Byte Enable Access Time	–	55	ns
Write Cycle				
t_{WC}	Write Cycle Time	55	–	ns
t_{SCE}[32]	$\overline{CE}$ LOW to Write End	45	–	ns
t_{AW}	Address Valid to Write End	45	–	ns
t_{HA}	Address Hold From Write End	0	–	ns
t_{SA}[32]	Address Setup to Write Start	0	–	ns
t_{PWE}	Write Pulse Width	40	–	ns
t_{SD}	Data Setup to Write End	30	–	ns
t_{HD}	Data Hold From Write End	0	–	ns
t_{HZWE}[34, 35]	R/$\overline{W}$ LOW to High Z	–	25	ns
t_{LZWE}[34, 35]	R/$\overline{W}$ HIGH to Low Z	0	–	ns
t_{WDD}[36]	Write Pulse to Data Delay	–	80	ns
t_{DDD}[36]	Write Data Valid to Read Data Valid	–	80	ns

Notes
32. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
33. At any temperature and voltage condition for any device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
34. Test conditions used are Load 3.
35. This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
36. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

Switching Characteristics for V_{CC} = 2.5 V (continued)

Over the Operating Range

Parameter	Description	CYDM256B16/CYDM128B16/CYDM064B16		Unit
		-55		
		Min	Max	
Busy Timing[37]				
t_{BLA}	$\overline{BUSY}$ LOW from Address Match	–	45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch	–	45	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	45	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	45	ns
t_{PS}[38]	Port Setup for Priority	5	–	ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	35	–	ns
t_{BDD}[39]	$\overline{BUSY}$ HIGH to Data Valid	–	40	ns
Interrupt Timing[37]				
t_{INS}	$\overline{INT}$ Set Time	–	45	ns
t_{INR}	$\overline{INT}$ Reset Time	–	45	ns
Semaphore Timing				
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	ns
t_{SWRD}	SEM Flag Write to Read Time	10	–	ns
t_{SPS}	SEM Flag Contention Window	10	–	ns
t_{SAA}	SEM Address Access Time	–	55	ns

Notes
37. Test conditions used are Load 2.
38. Add 2 ns to this parameter if V_{CC} and V_{DDIOR} are <1.8 V, and V_{DDIOL} is >2.5 V at temperature <0 °C.
39. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

Switching Characteristics for V_{CC} = 3.0 V

Over the Operating Range

Parameter	Description	CYDM256B16/CYDM128B16/CYDM064B16		Unit
		-55		
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55	–	ns
t_{AA}	Address to Data Valid	–	55	ns
t_{OHA}	Output Hold From Address Change	5	–	ns
t_{ACE}[40]	$\overline{CE}$ LOW to Data Valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	30	ns
t_{LZOE}[41, 42, 43]	$\overline{OE}$ Low to Low Z	1	–	ns
t_{HZOE}[41, 42, 43]	$\overline{OE}$ HIGH to High Z	–	25	ns
t_{LZCE}[41, 42, 43]	$\overline{CE}$ LOW to Low Z	1	–	ns
t_{HZCE}[41, 42, 43]	$\overline{CE}$ HIGH to High Z	–	25	ns
t_{PU}[43]	$\overline{CE}$ LOW to Power up	0	–	ns
t_{PD}[43]	$\overline{CE}$ HIGH to Power down	–	55	ns
t_{ABE}[40]	Byte Enable Access Time	–	55	ns
Write Cycle				
t_{WC}	Write Cycle Time	55	–	ns
t_{SCE}[40]	$\overline{CE}$ LOW to Write End	45	–	ns
t_{AW}	Address Valid to Write End	45	–	ns
t_{HA}	Address Hold From Write End	0	–	ns
t_{SA}[40]	Address Setup to Write Start	0	–	ns
t_{PWE}	Write Pulse Width	40	–	ns
t_{SD}	Data Setup to Write End	30	–	ns
t_{HD}	Data Hold From Write End	0	–	ns
t_{HZWE}[42, 43]	R/$\overline{W}$ LOW to High Z	–	25	ns
t_{LZWE}[42, 43]	R/$\overline{W}$ HIGH to Low Z	0	–	ns
t_{WDD}[44]	Write Pulse to Data Delay	–	80	ns
t_{DDD}[44]	Write Data Valid to Read Data Valid	–	80	ns

Notes
40. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
41. At any temperature and voltage condition for any device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
42. Test conditions used are Load 3.
43. This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
44. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

Switching Characteristics for V_{CC} = 3.0 V (continued)

Over the Operating Range

Parameter	Description	CYDM256B16/CYDM128B16/CYDM064B16		Unit
		-55		
		Min	Max	
Busy Timing[45]				
t_{BLA}	$\overline{BUSY}$ LOW from Address Match	–	45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch	–	45	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	45	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	45	ns
t_{PS}[46]	Port Setup for Priority	5	–	ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	35	–	ns
t_{BDD}[47]	$\overline{BUSY}$ HIGH to Data Valid	–	40	ns
Interrupt Timing[45]				
t_{INS}	$\overline{INT}$ Set Time	–	45	ns
t_{INR}	$\overline{INT}$ Reset Time	–	45	ns
Semaphore Timing				
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	ns
t_{SWRD}	SEM Flag Write to Read Time	10	–	ns
t_{SPS}	SEM Flag Contention Window	10	–	ns
t_{SAA}	SEM Address Access Time	–	55	ns

Notes
45. Test conditions used are Load 2.
46. Add 2 ns to this parameter if V_{CC} and V_{DDIOR} are <1.8 V, and V_{DDIOL} is >2.5 V at temperature <0 °C.
47. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} – t_{PWE}$ (actual) or $t_{DDD} – t_{SD}$ (actual).

Switching Waveforms

Figure 3. Read Cycle No.1 (Either Port Address Access) [32, 33, 34]

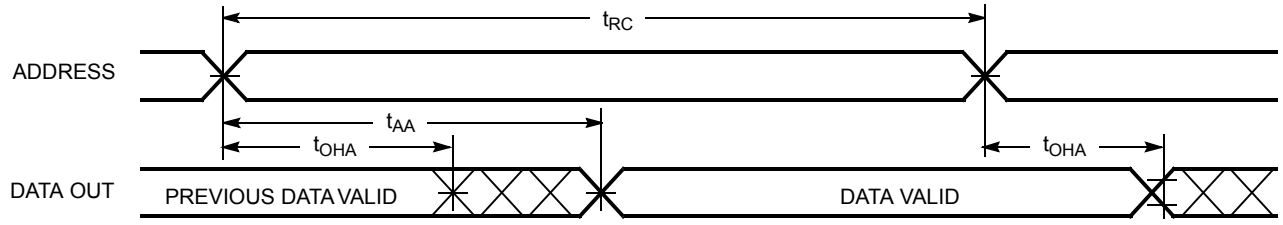


Figure 4. Read Cycle No.2 (Either Port $\overline{CE}$/$\overline{OE}$ Access) [32, 35, 36]

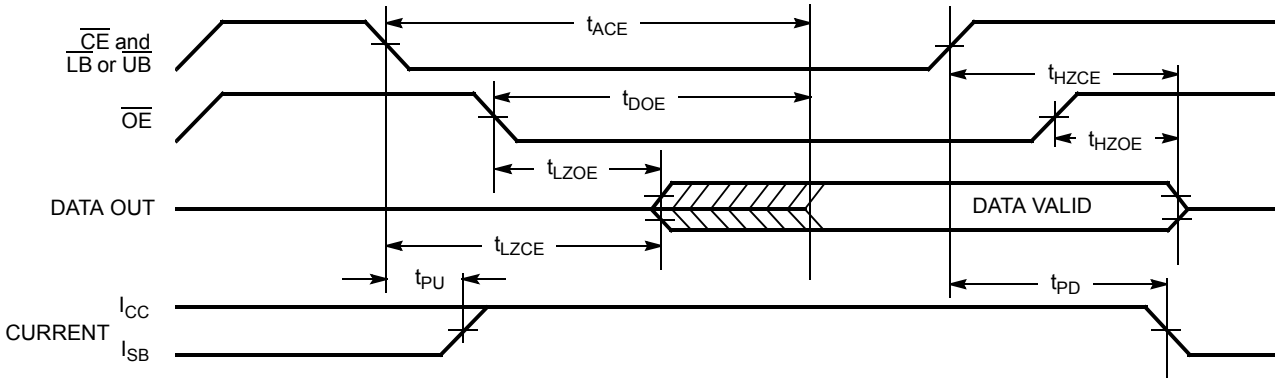
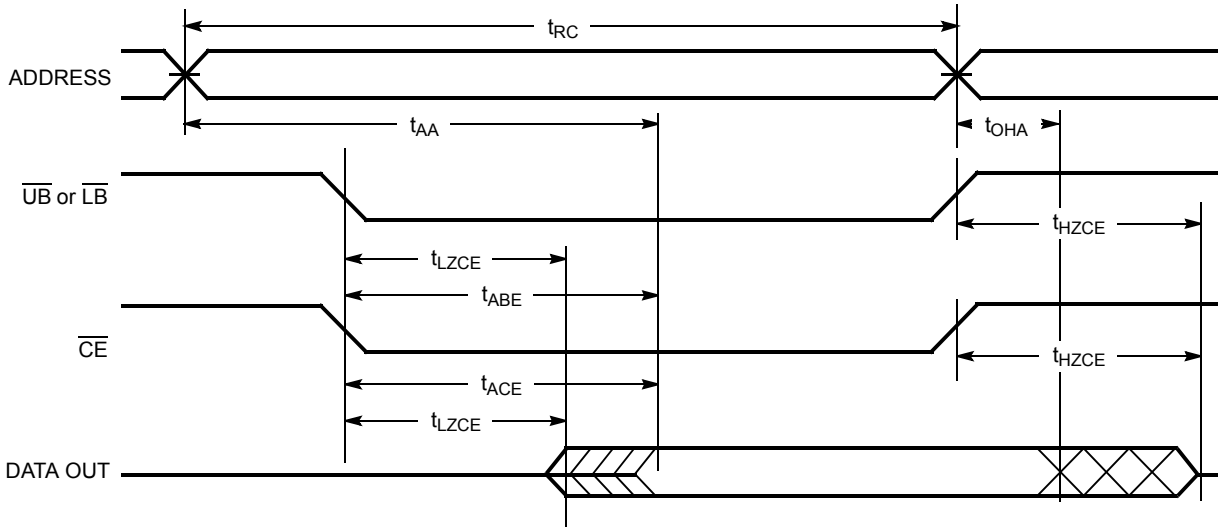


Figure 5. Read Cycle No. 3 (Either Port) [32, 34, 37, 38]



Notes
32. R/$\overline{W}$ is HIGH for read cycles.
33. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
34. $\overline{OE}$ = V_{IL}.
35. Address valid before or coincident with $\overline{CE}$ transition LOW.
36. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.
37. R/$\overline{W}$ must be HIGH during all address transitions.
38. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.

Switching Waveforms (continued)

Figure 6. Write Cycle No.1: R/$\overline{W}$ Controlled Timing [39, 40, 41, 42, 43, 44]

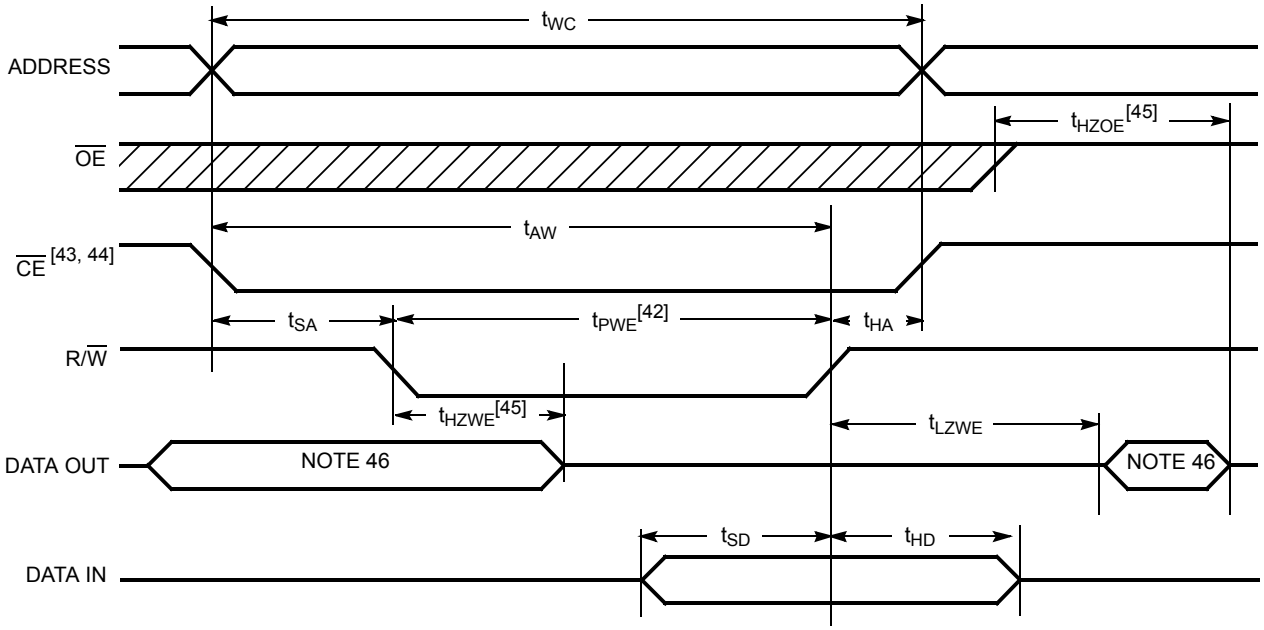
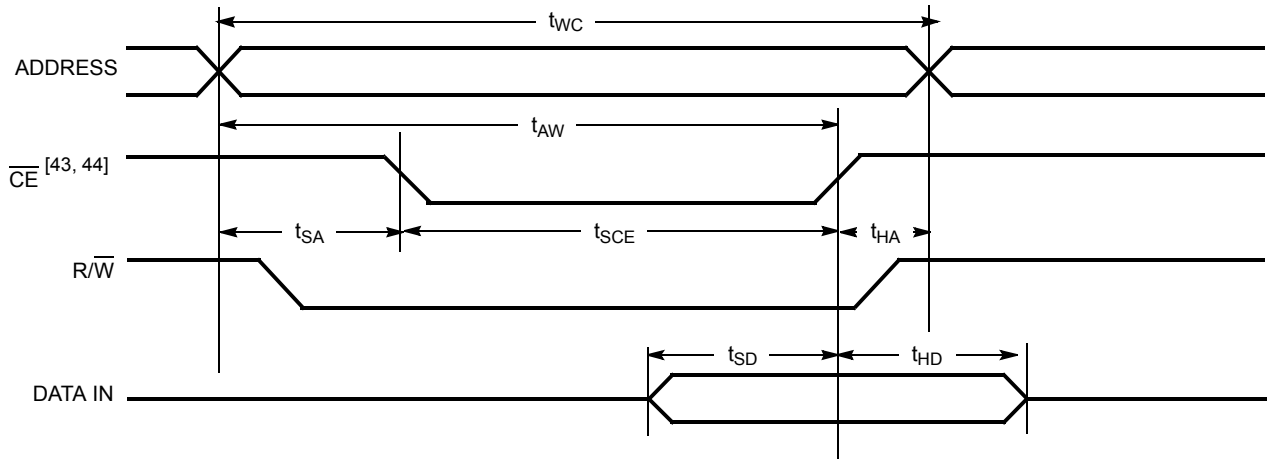


Figure 7. Write Cycle No. 2: $\overline{CE}$ Controlled Timing [39, 40, 41, 46]



Notes

39. R/$\overline{W}$ must be HIGH during all address transitions.
40. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
41. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
42. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
43. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
44. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
    To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
45. Transition is measured ±0 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
46. During this period, the I/O pins are in the output state, and input signals must not be applied.

Switching Waveforms (continued)

Figure 8. Semaphore Read After Write Timing (Either Side) [47, 48]

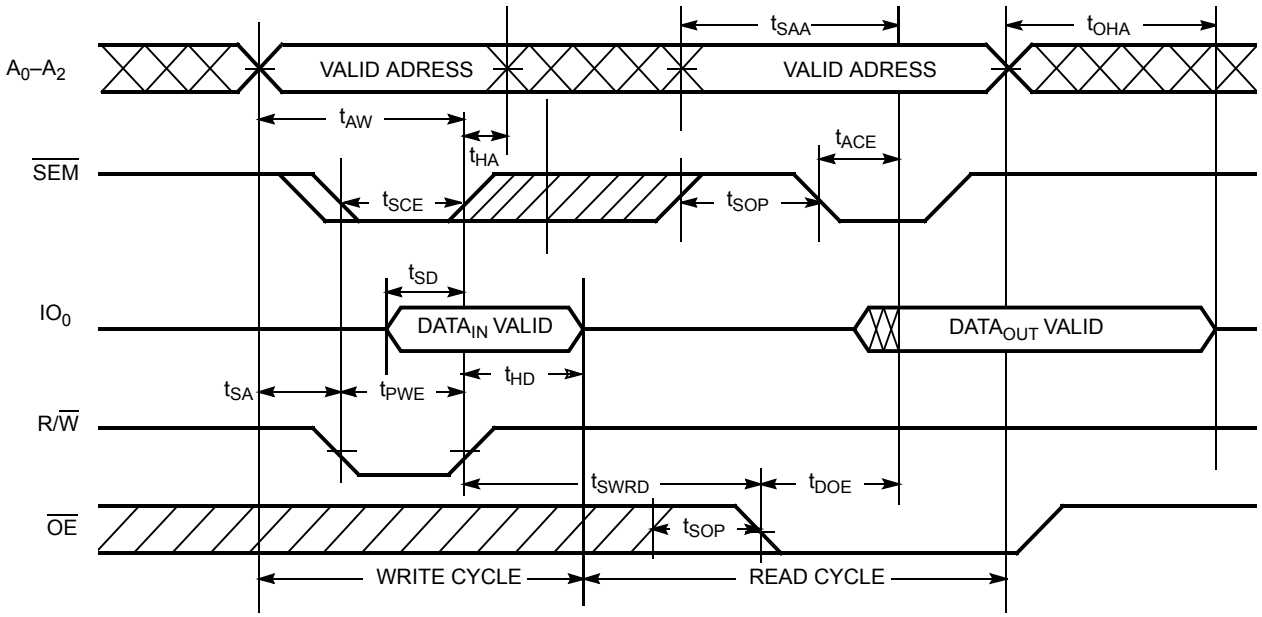
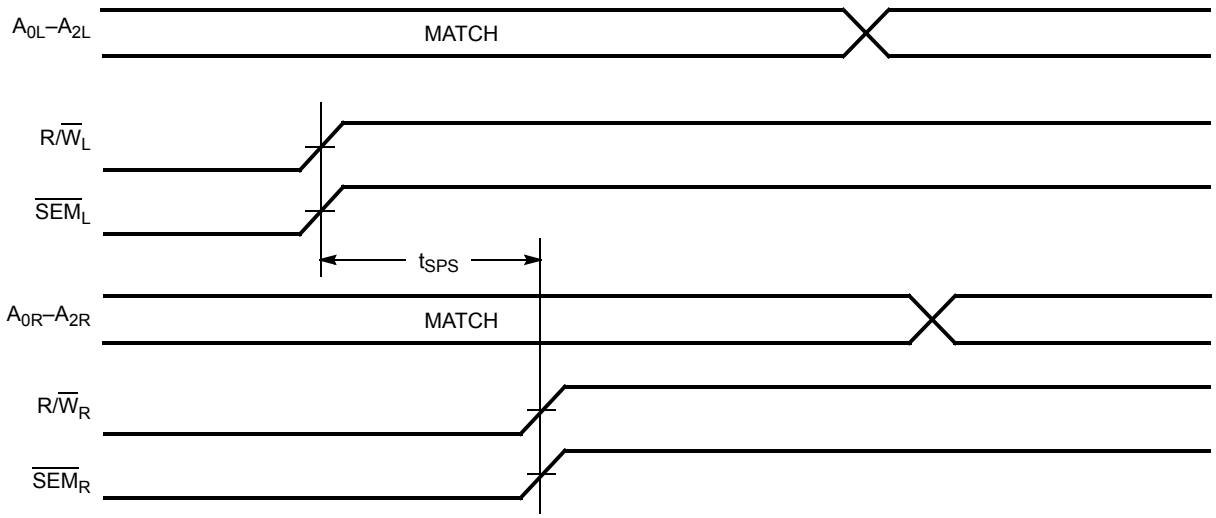


Figure 9. Timing Diagram of Semaphore Contention [49, 50]



Notes
47. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high impedance state.
48. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
49. $IO_{0R} = IO_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
50. If t_{SPS} is violated, the semaphore is definitely obtained by one side or the other, but the side that gets the semaphore cannot be predicted.

Switching Waveforms (continued)

Figure 10. Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$ = HIGH) [51]

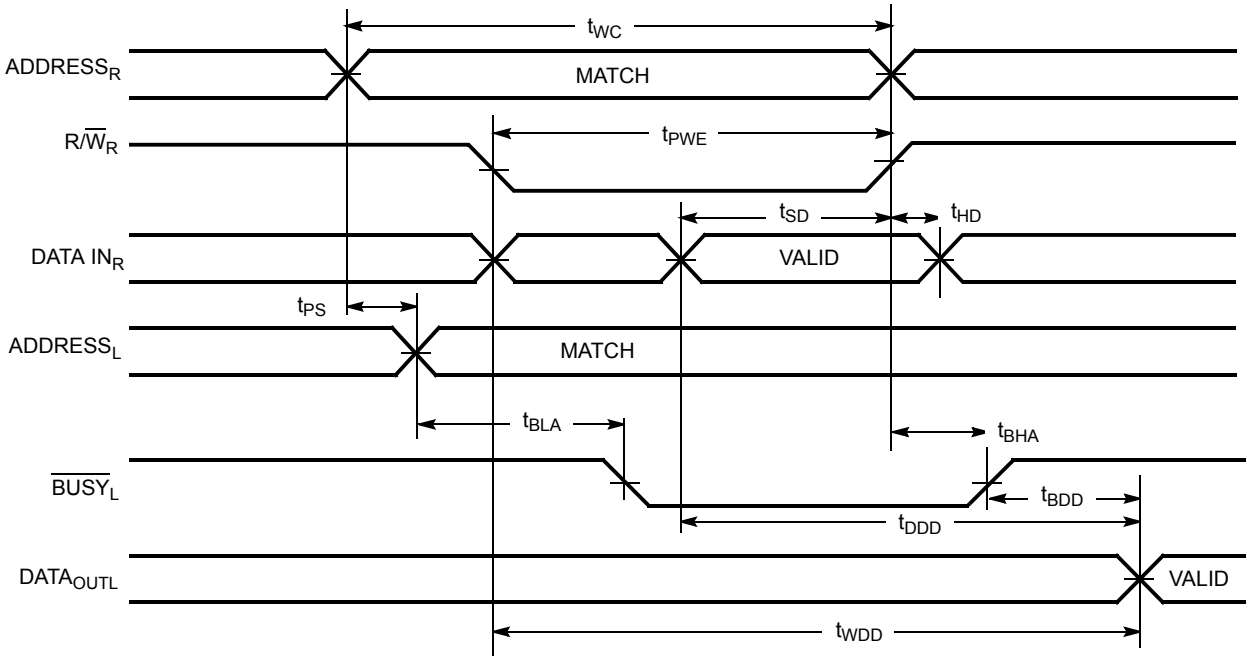
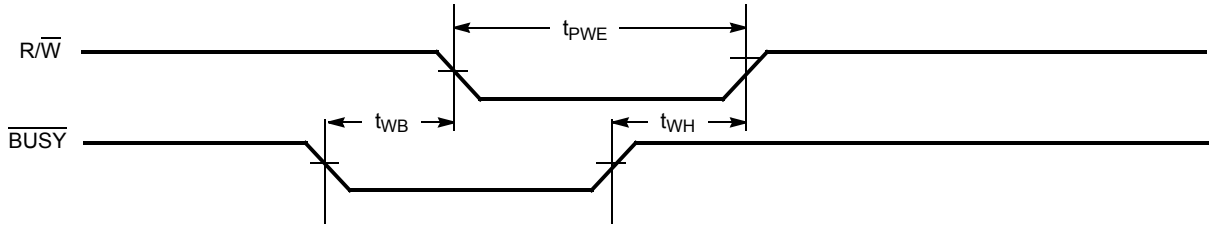


Figure 11. Write Timing with Busy Input (M/$\overline{S}$ = LOW)

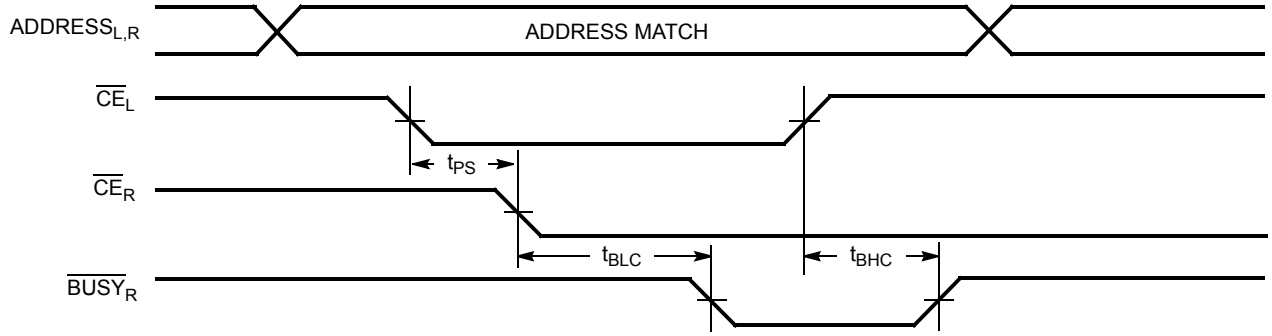


Note
51. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 12. Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)

$\overline{CE_L}$ Valid First [52]



$\overline{CE_R}$ Valid First

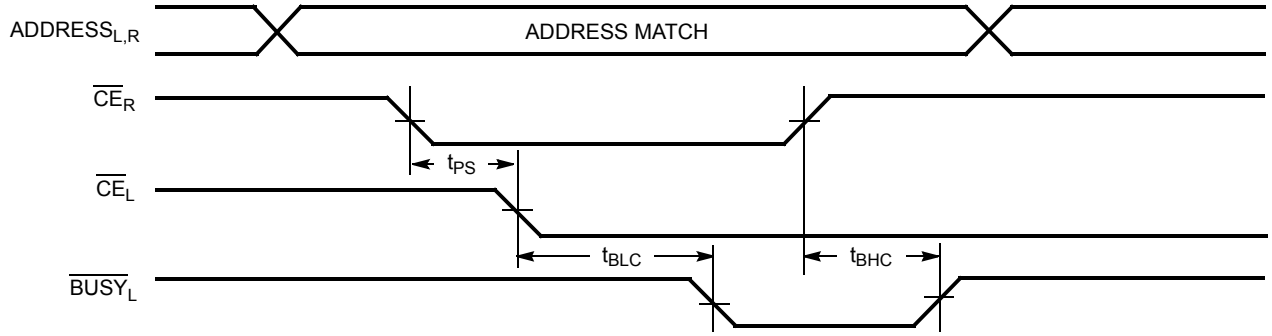
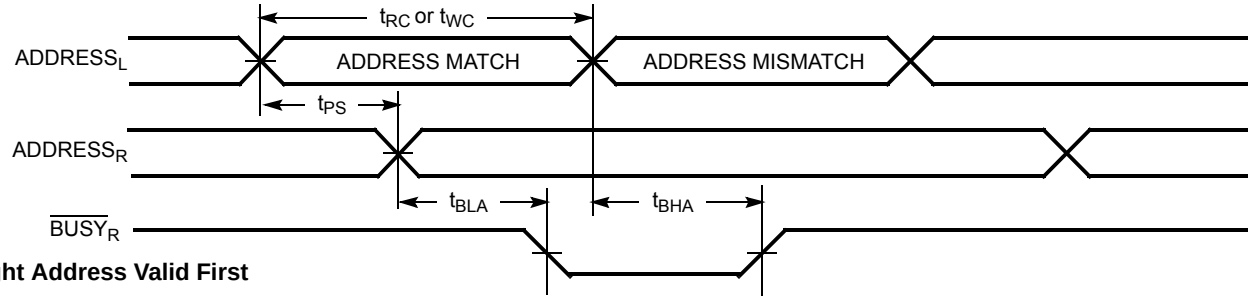
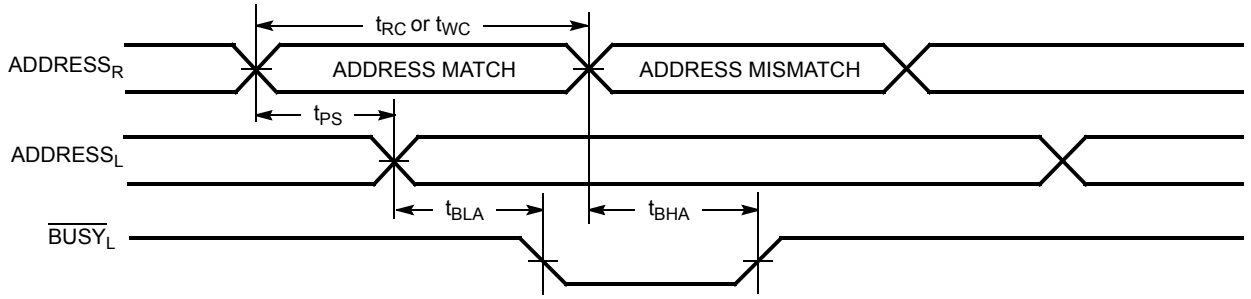


Figure 13. Busy Timing Diagram No.2 (Address Arbitration) [52]

Left Address Valid First



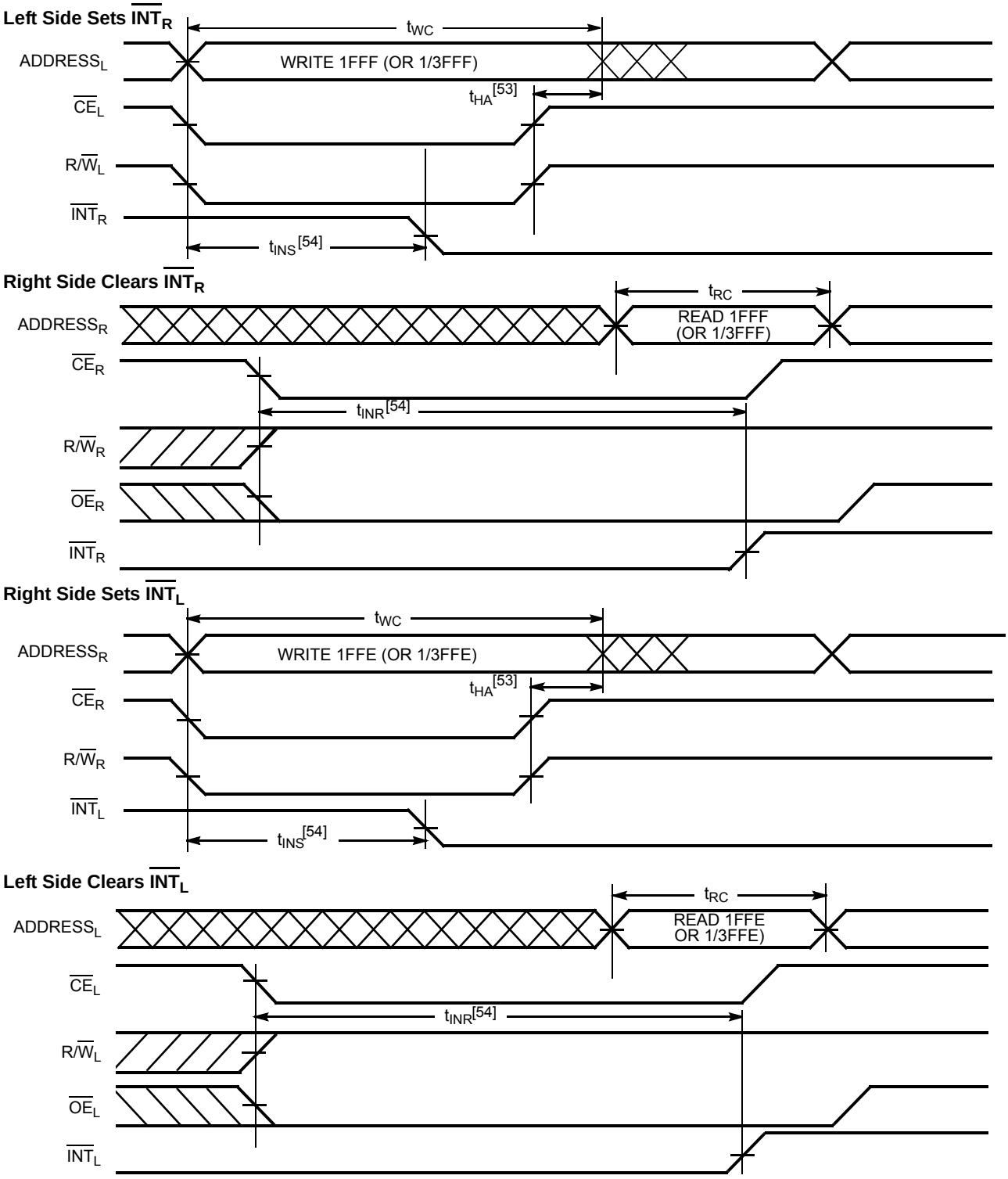
Right Address Valid First



Note
52. If t_{PS} is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ is asserted.

Switching Waveforms (continued)

Figure 14. Interrupt Timing Diagrams



Notes
53. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
54. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Ordering Information

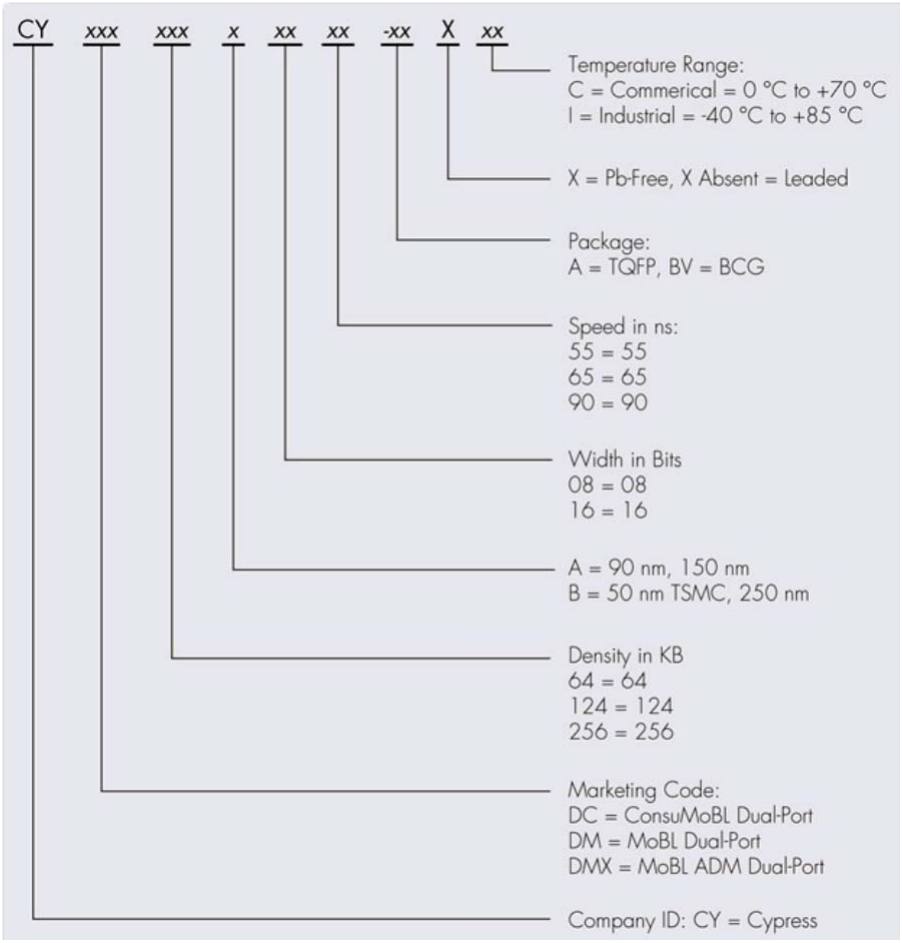
16K × 16 1.8 V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CYDM256B16-55BVXI	BZ100	100-ball 0.5 mm Pitch BGA Pb-free	Industrial

8K × 16 1.8 V Asynchronous Dual-Port SRAM

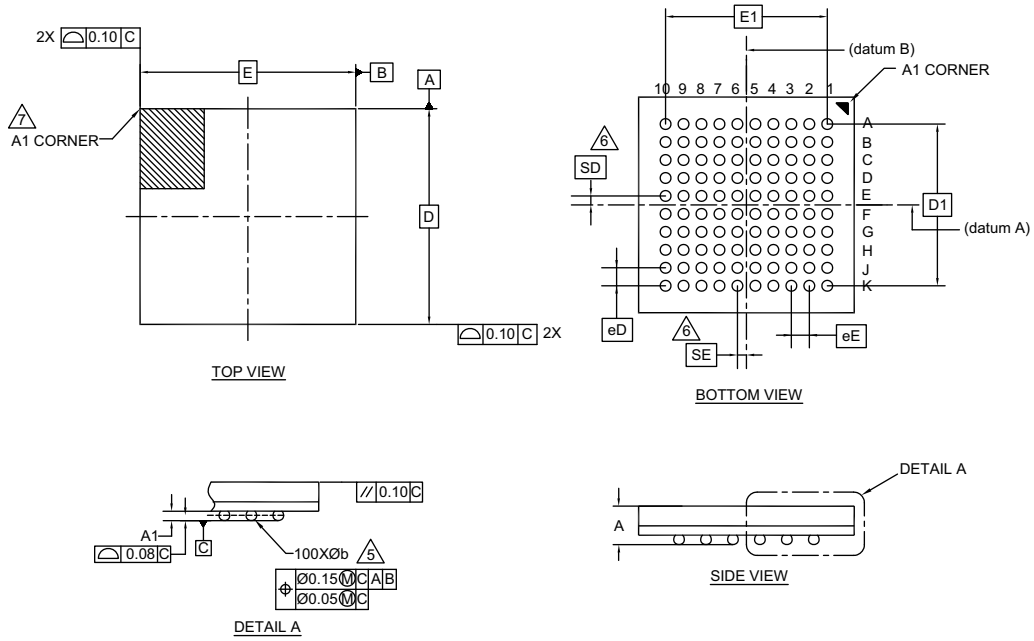
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CYDM128B16-55BVXI	BZ100	100-ball 0.5 mm Pitch BGA Pb-free	Industrial

Ordering Code Definitions



Package Diagram

Figure 15. 100-ball VFBGA (6 × 6 × 1.0 mm) Package Outline, 51-85209



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	4.50 BSC		
E1	4.50 BSC		
MD	10		
ME	10		
N	100		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

Document History Page

Document Title: CYDM064B16/CYDM128B16/CYDM256B16, 1.8 V, 4K/8K/16K × 16 MoBL® Dual-Port Static RAM Document Number: 001-00217				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	369423	YDT	05/23/05	New data sheet.
*A	381721	YDT	See ECN	Updated Selection Guide for VCC = 2.5 V: Updated values of I_{CC}, I_{SB1} parameters. Updated Selection Guide for VCC = 3.0 V: Updated values of I_{CC}, I_{SB1} parameters. Updated Electrical Characteristics for VCC = 1.8 V: Updated values of V_{OL}ODR parameter. Updated Electrical Characteristics for VCC = 2.5 V: Updated values of V_{OL}ODR parameter. Updated values of I_{CC}, I_{SB1}, I_{SB2}, I_{SB4} parameters. Updated Electrical Characteristics for VCC = 3.0 V: Updated values of V_{OL}ODR parameter. Updated values of I_{CC}, I_{SB1}, I_{SB2}, I_{SB4} parameters.
*B	396697	KGH	See ECN	Updated Electrical Characteristics for VCC = 1.8 V: Fixed typo (Replaced µA with mA in “Units” column for ISB2 and ISB4 parameters). Updated Electrical Characteristics for VCC = 2.5 V: Fixed typo (Replaced µA with mA in “Units” column for ISB2 and ISB4 parameters). Updated Electrical Characteristics for VCC = 3.0 V: Fixed typo (Replaced µA with mA in “Units” column for ISB2 and ISB4 parameters). Updated Switching Characteristics for VCC = 1.8 V: Changed value of t_{INS} and t_{INR} parameters corresponding to 55 ns speed bin from 28 ns to 31 ns.
*C	404777	KGH	See ECN	Removed 35 ns speed bin related information in all instances across the document. Added 40 ns speed bin related information in all instances across the document. Updated Electrical Characteristics for VCC = 1.8 V: Updated details in “Description” column of V_{OH} and V_{OL} parameters (Updated I_{OH} and I_{OL} values). Updated Electrical Characteristics for VCC = 2.5 V: Updated details in “Description” column of V_{OH} and V_{OL} parameters (Updated I_{OH} and I_{OL} values). Updated Electrical Characteristics for VCC = 3.0 V: Updated details in “Description” column of V_{OH} and V_{OL} parameters (Updated I_{OH} and I_{OL} values). Updated Switching Characteristics for VCC = 1.8 V: Added Note 30 and referred the same note in t_{PS} parameter. Updated Switching Characteristics for VCC = 2.5 V: Replaced TBD with values. Added Note 38 and referred the same note in t_{PS} parameter. Updated Switching Characteristics for VCC = 3.0 V: Replaced TBD with values. Added Note 46 and referred the same note in t_{PS} parameter. Updated Ordering Information: Updated part numbers.
*D	426637	KGH	See ECN	Updated Ordering Information: Updated part numbers.

Document History Page (continued)

Document Title: CYDM064B16/CYDM128B16/CYDM256B16, 1.8 V, 4K/8K/16K × 16 MoBL® Dual-Port Static RAM Document Number: 001-00217				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	733676	HKH	See ECN	Updated Functional Overview: Updated Power Supply: Fixed typo (Replaced 3.3 V with 3.0 V). Updated Switching Characteristics for VCC = 1.8 V: Updated maximum value of t_{DDD} parameter (to be consistent with value of t_{WDD} parameter). Updated Switching Characteristics for VCC = 2.5 V: Updated maximum value of t_{DDD} parameter (to be consistent with value of t_{WDD} parameter). Updated Switching Characteristics for VCC = 3.0 V: Updated maximum value of t_{DDD} parameter (to be consistent with value of t_{WDD} parameter).
*F	2545957	OGC / AESA	07/31/2008	Removed 40 ns speed bin related information in all instances across the document. Updated to new template.
*G	2920132	OGC	04/26/10	Updated Document Title to read as “CYDM064B16, CYDM128B16, CYDM256B16 1.8V 4K/8K/16K × 16 MoBL® Dual-Port Static RAM”. Removed references of × 8 part in all instances across the document.
*H	3183900	ESH	02/28/11	Added Ordering Code Definitions under Ordering Information.
*I	4303480	HBM	03/10/2014	Updated to new template. Completing Sunset Review.
*J	5677663	HBM	03/30/2017	Updated Package Diagram: spec 51-85209 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*K	6134239	HBM	04/12/2018	Removed obsolete parts CYDM256B16-55BVXC, CYDM128B16-55BVXC, CYDM064B16-55BVXC, and CYDM064B16-55BVXI from Ordering Information.

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