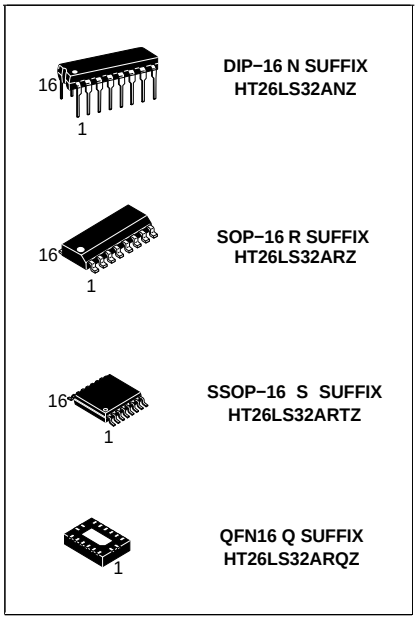
QUAD RS-422, RS-423 CMOS Differential Line Receiver

GENERAL DESCRIPTION

The HT26LS32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The HT26LS32 has an input sensitivity of 200mv over the common mode input voltage range of ±7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the HT26LS32 circuit.The HT26LS32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. HT26LS32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. HT26LS32 is suitable for low power 5V operation.

FEATURES

- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed



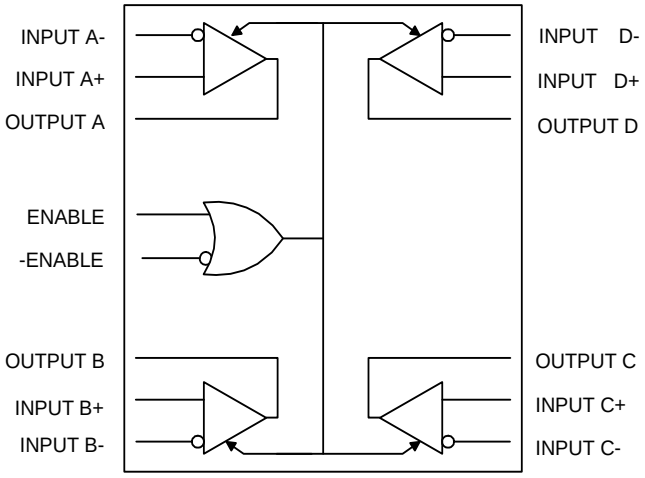
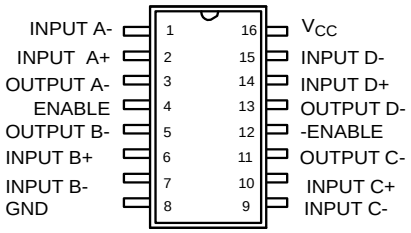


Figure 1. Block Diagram

PIN CONFIGURATION



SOPP16/TSSOP16/DIP16

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	INPUT A-	I	Receiver A differential inverting input pin.
2	INPUT A+	I	Receiver A differential non-inverting input pin.
3	OUTPUT A	O	Receiver A output pin.
4	ENABLE	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four receivers.
5	OUTPUT B	O	Receiver B output pin.
6	INPUT B+	I	Receiver B differential non-inverting input pin.
7	INPUT B-	I	Receiver B differential inverting input pin.
8	GND	O	Signal and power ground.
9	INPUT C-	I	Receiver C differential inverting input pin.
10	INPUT C+	I	Receiver C differential non-inverting input pin.
11	OUTPUT C	O	Receiver C output pin.
12	-ENABLE	I	Gate control (active low). See ENABLE description
13	OUTPUT D	O	Receiver D output pin.
14	INPUT D+	I	Receiver D differential non-inverting input pin.
15	INPUT D-	I	Receiver D differential inverting input pin.
16	V_{CC}	I	Power supply pin.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = -40°C - +85°C, V_{CC} = 5.0V ± 10% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_1	Propagation Delay, Input to Output		8	10	ns	S1=V_{CC}
T_2	Propagation Delay, Input to Output		18	20	ns	S1=GND
T_3	Output Enable Time		18	20	ns	V_{DIF}=2.5V
T_4	Output Disable Time		18	20	ns	V_{DIF}=2.5V

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = -40°C - +85°C, V_{CC} = 5.0V ± 10% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Enable High Level	2.0			V	
V_{IL}	Enable Low Level			0.8	V	
V_{OH}	Output High Level	3.8	4.2		V	I_{OH}= -6mA
V_{OL}	Output Low Level			0.4	V	I_{OH}= 6mA
V_{ID}	Differential Input Level	-0.2		0.2	V	-7V < V_{CM} < +7V
V_H	Input Hysteresis		50		mV	
I_{IN}	Input Current			±1.0	µA	
I_{CC}	Operating Current		12		mA	V_{DIF}=+1V
I_{OZ}	Three-State Output Leakage		±1.0	±5.0	µA	V_{OUT}=V_{CC} or GND
I_{EN}	Enable Input Current		±1.0		µA	V_{IN}=V_{CC} or GND
V_R	Input Resistance	5		15	KQ	-7V < V_{CM} < +7V

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range 7V
Voltage at Any Pin ..... GND-0.3V to V_{CC} + 0.3V
Operating Temperature ..... –40°C to +85°C
Storage Temperature ..... -60°C to +160°C
Package Dissipation 500mW

Enable	-Enable	Input	Differential Non-Inverting Output	Differential Inverting Output
L	H	Z	X	X
H	L	L	L	H
H	L	H	H	L

Notes
X = Don't care
Z = Three-State (high impedance)

Table 1. Functional Table

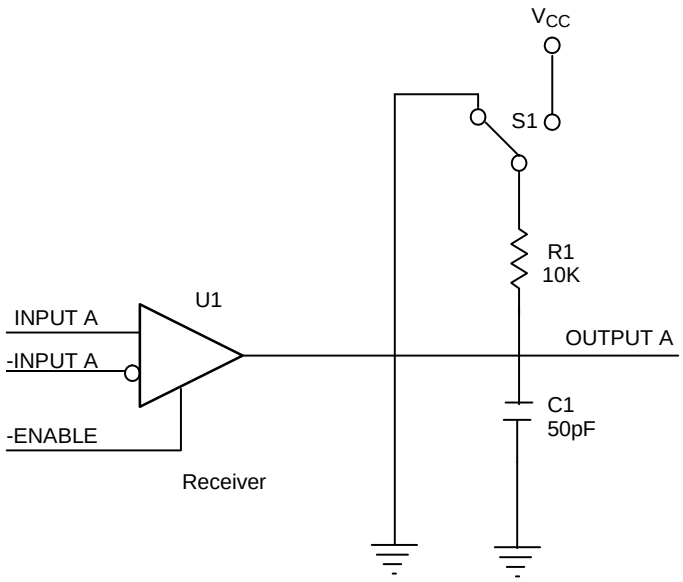


Figure 2. Test Condition

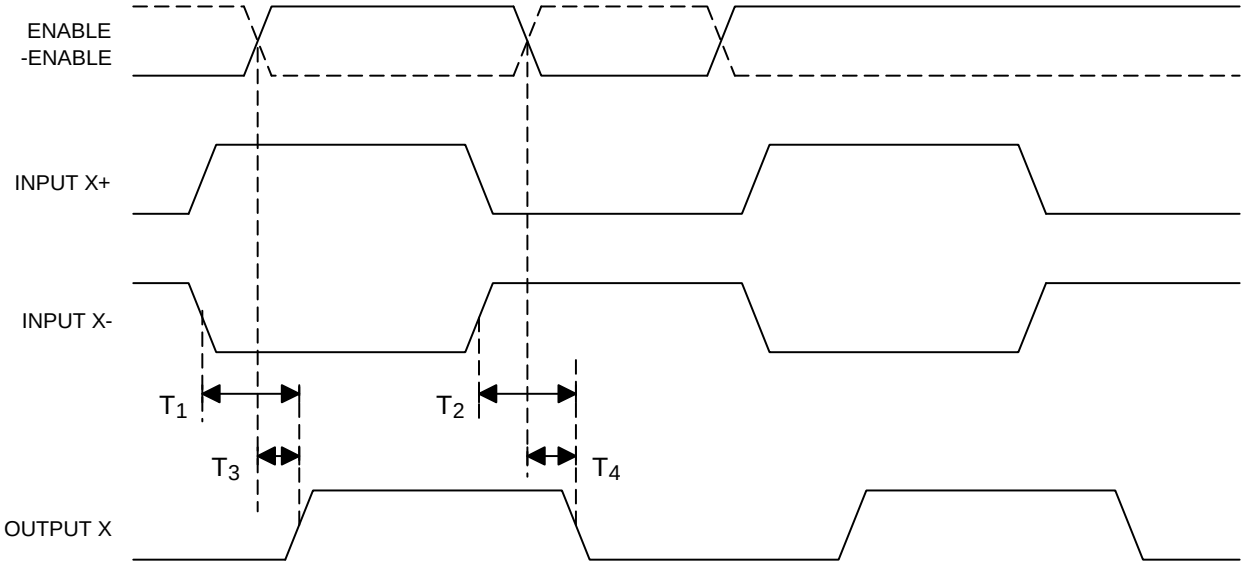
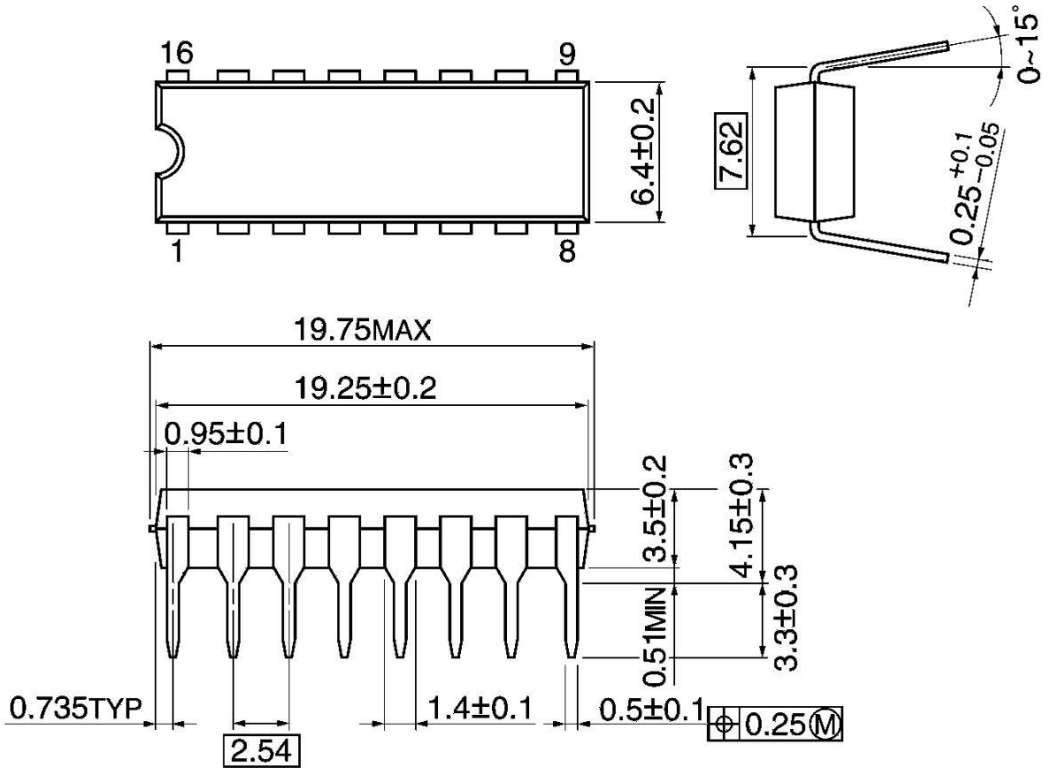


Figure 3. Differential Line Receiver Timing

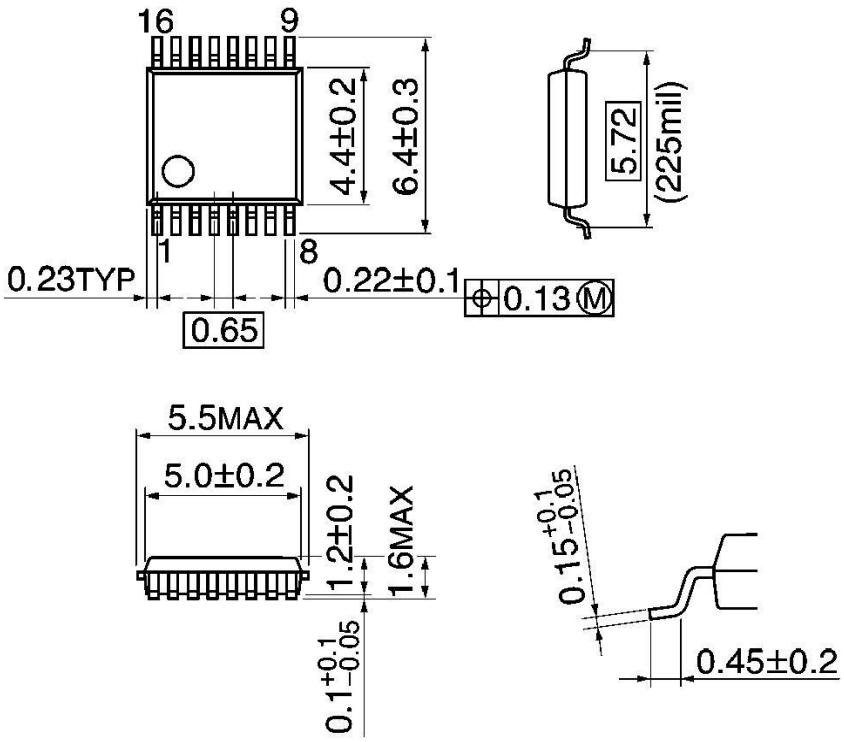
Package Dimensions

DIP16-P-300-2.54A Unit: mm



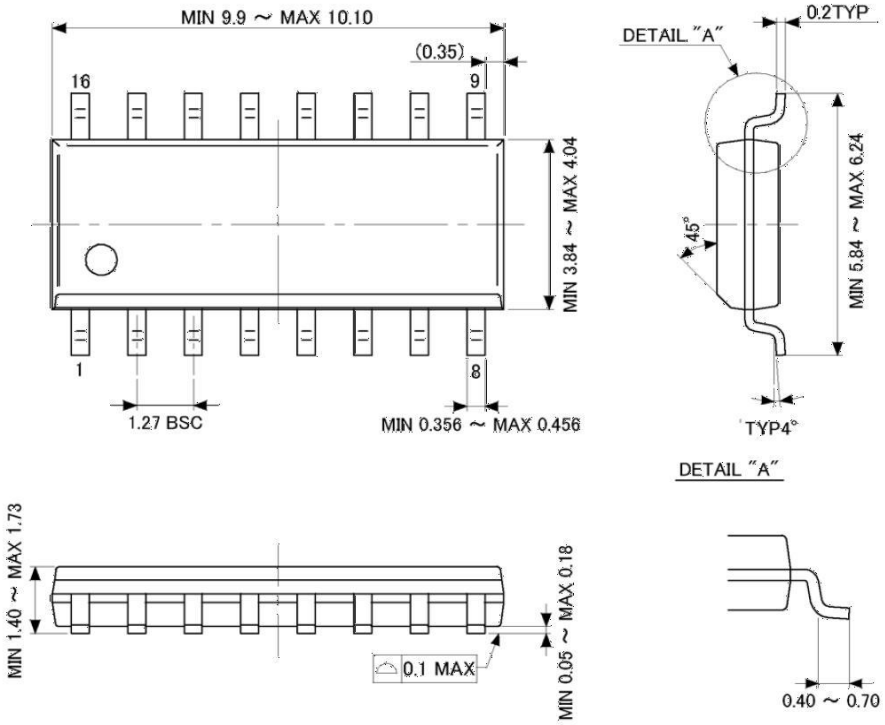
Weight: 1.11 g (Typ.)

TSSOP16-P-225-0.65B Unit: mm



Weight: 0.07 g (Typ.)

P-SOP16-0410-1.27-002 Unit: mm



Weight: 0.15 g (Typ.)