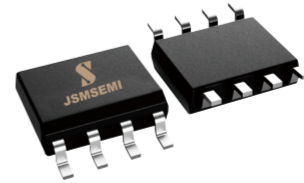


The JSM9435 uses advanced trench technology to provide excellent RDS(ON), shoot-through immunity, body diode characteristics and ultra-low gate resistance.

This device is ideally suited for use as a low side switch in Notebook CPU core power conversion.

JSM9435采用先进的沟道技术，提供出色的无线电数据系统（ON）、穿透抗扰性、体二极管特性和超低栅极电阻。该设备非常适合作为笔记本电脑CPU核心功率转换的低端开关。



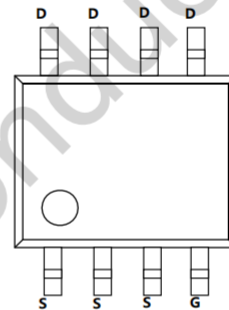
### 主要特性/Features

- 先进的沟槽工艺技术  
Advanced trench process technology
- 高密度单元设计，超低导通电阻  
High density cell design for ultra low on-resistance
- 高功率和电流处理能力  
High power and current handling capability

### 应用/Application

- 蓄电池开关 Battery Switch
- 负荷开关 Load Switch

### 引脚定义/pin definition

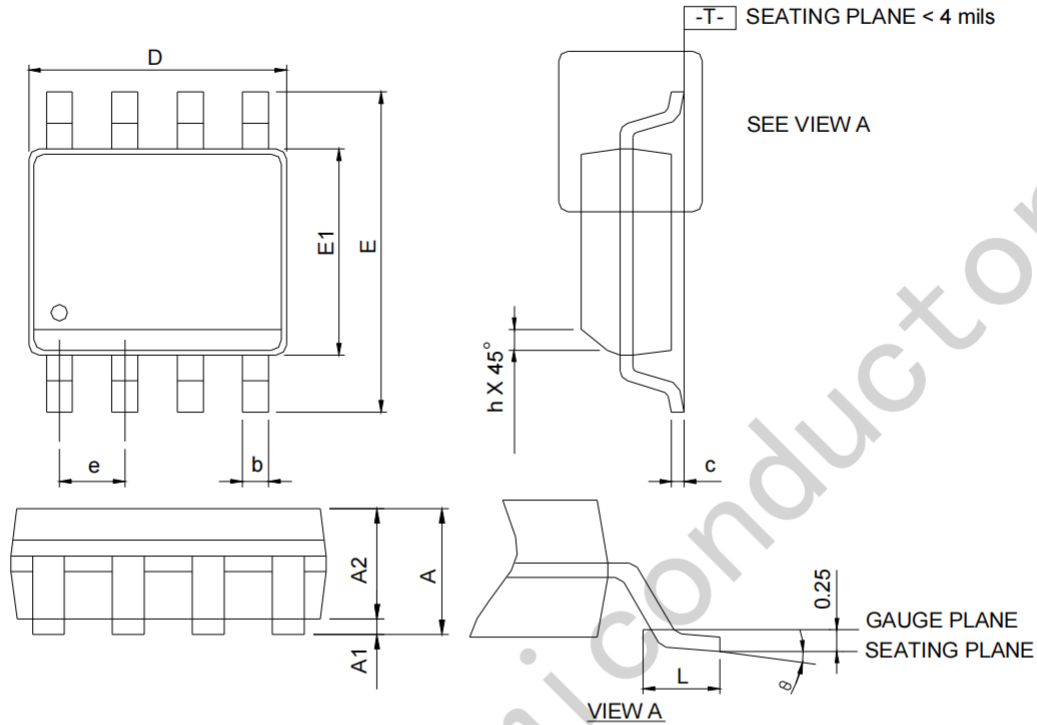


### 电性能参数/Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Description	Min.	Typ.	Max.	Test Conditions
V(BR)DSS	Drain-to-Source Breakdown Voltage	-30V			V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ID(Device Ref.)	Continuous Drain Current			-5.1A	T <sub>J</sub> = 25°C
RDS(on)	Static Drain-to-Source On-Resistance		43mΩ	55mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -5.1A
RDS(on)	Static Drain-to-Source On-Resistance		62mΩ	90mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.2A
VGS(th)	Gate Threshold Voltage	-1.0V	-1.5V	-3.0V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
IDSS	Drain-to-Source Leakage Current			1μA	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C
IGSS	Gate-to-Source Leakage Current			±100nA	V <sub>GS</sub> = ±20V
T <sub>J</sub>	Operating Junction and Storage Temperature Range	-55°C to 150°C Max.			
TSTG					

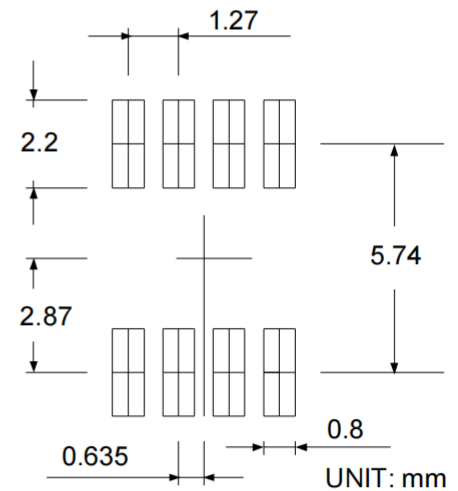
## Package Information

SOP-8



SYMBOLS	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

### RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.