

FEATURES

- +3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20 years at temperature
- RoHS-compliant small footprint BGA and TSOP2 package
- All products meet MSL-3 moisture sensitivity level



BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in systems for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM



INTRODUCTION

The **MR3A16A** is a 8,388,608-bit magnetoresistive random access memory (MRAM) device organized as 524,288 words of 16 bits. The MR3A16A offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR3A16A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.



The **MR3A16A** is available in a small footprint 48-pin ball grid array (BGA) package and a 54-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR3A16A** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), and industrial temperature (-40 to +85 °C) operating temperature options.

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1. DEVICE PIN ASSIGNMENT

Figure 1.0 Block Diagram

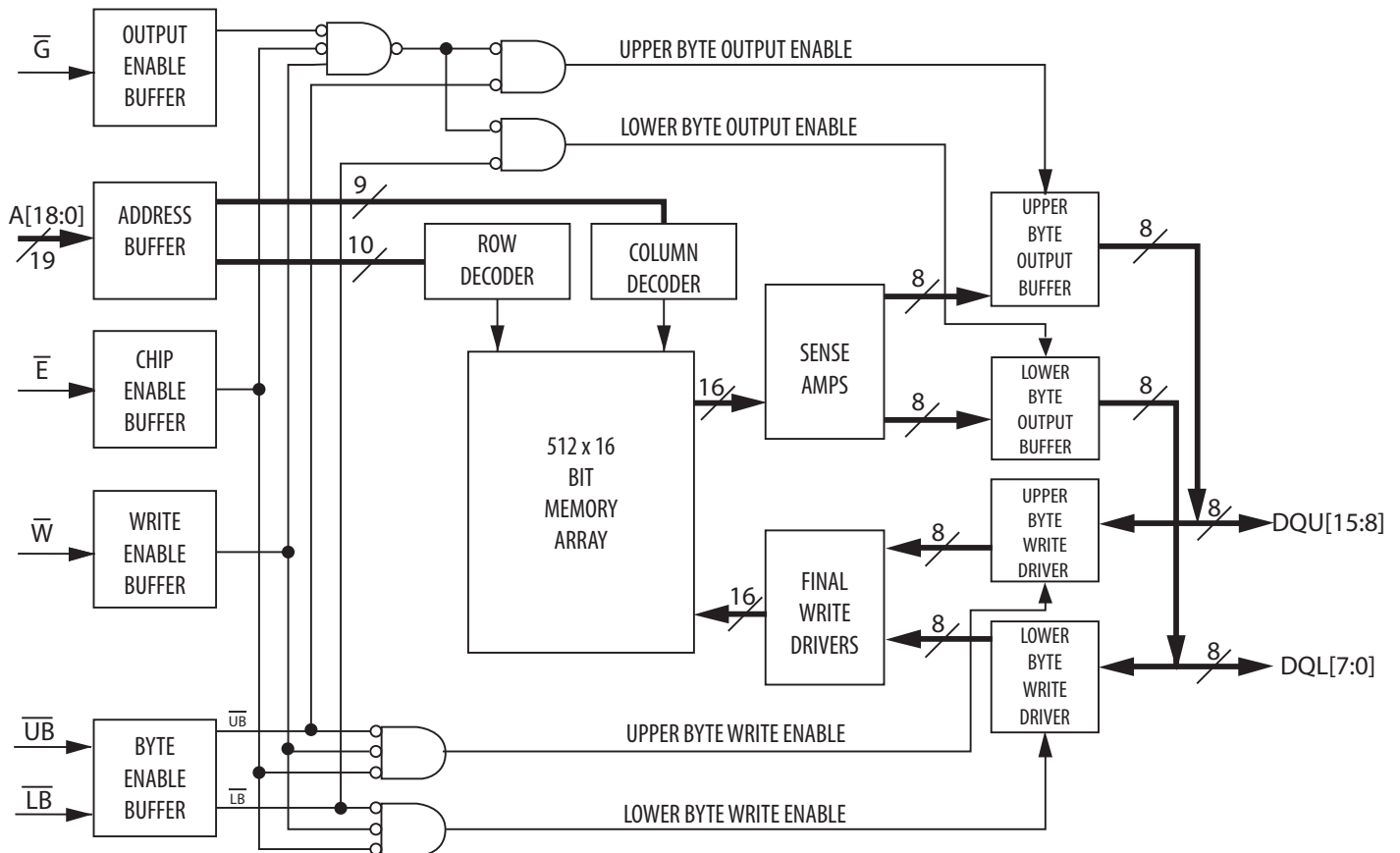
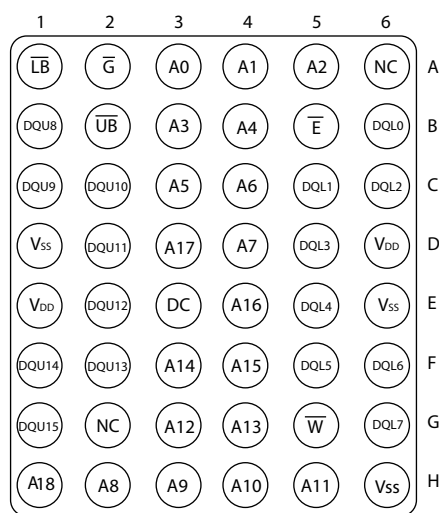


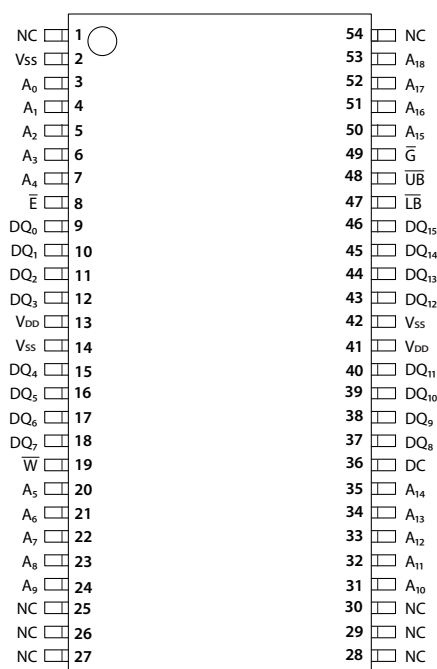
Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
\bar{E}	Chip Enable
\bar{W}	Write Enable
\bar{G}	Output Enable
\bar{UB}	Upper Byte Enable
\bar{LB}	Lower Byte Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection

Figure 1.1 Pin Diagrams for Available Packages (Top View)



48-Pin BGA



54-Pin TSOP2

Table 1.2 Operating Modes

\bar{E}^1	\bar{G}^1	\bar{W}^1	\bar{LB}^1	\bar{UB}^1	Mode	V_{DD} Current	DQL[7:0] ²	DQU[15:8] ²
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower Byte Read	I_{DDR}	D _{Out}	Hi-Z
L	L	H	H	L	Upper Byte Read	I_{DDR}	Hi-Z	D _{Out}
L	L	H	L	L	Word Read	I_{DDR}	D _{Out}	D _{Out}
L	X	L	L	H	Lower Byte Write	I_{DDW}	D _{in}	Hi-Z
L	X	L	H	L	Upper Byte Write	I_{DDW}	Hi-Z	D _{in}
L	X	L	L	L	Word Write	I_{DDW}	D _{in}	D _{in}

¹ H = high, L = low, X = don't care

² Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field greater than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings¹

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Supply voltage ²		-0.5 to 4.0	V
V_{IN}	Voltage on an pin ²		-0.5 to $V_{DD} + 0.5$	V
I_{OUT}	Output current per pin		±20	mA
P_D	Package power dissipation ³		0.600	W
T_{BIAS}	Temperature under bias	Commercial	-10 to 85	°C
		Industrial	-45 to 95	°C
T_{stg}	Storage Temperature		-55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)		260	°C
H_{max_write}	Maximum magnetic field	During Write	8000	A/m
H_{max_read}	Maximum magnetic field	During Read or Standby		

¹ Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

² All voltages are referenced to V_{SS} . The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.

³ Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Symbol	Parameter	Temp Range	Min	Typical	Max	Unit
V_{DD}	Power supply voltage		3.0 ¹	3.3	3.6	V
V_{WI}	Write inhibit voltage		2.5	2.7	3.0 ¹	V
V_{IH}	Input high voltage		2.2	-	$V_{DD} + 0.3$ ²	V
V_{IL}	Input low voltage		-0.5 ³	-	0.8	V
T_A	Temperature under bias	Commercial	0	-	70	°C
		Industrial	-40	-	85	°C

¹ There is a 2 ms startup time once V_{DD} exceeds $V_{DD}(\min)$. See **Power Up and Power Down Sequencing** below.

² $V_{IH}(\max) = V_{DD} + 0.3 V_{DC}$; $V_{IH}(\max) = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

³ $V_{IL}(\min) = -0.5 V_{DC}$; $V_{IL}(\min) = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(\min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2$ V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \bar{E} and \bar{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(\min)$.

Figure 2.1 Power Up and Power Down Diagram

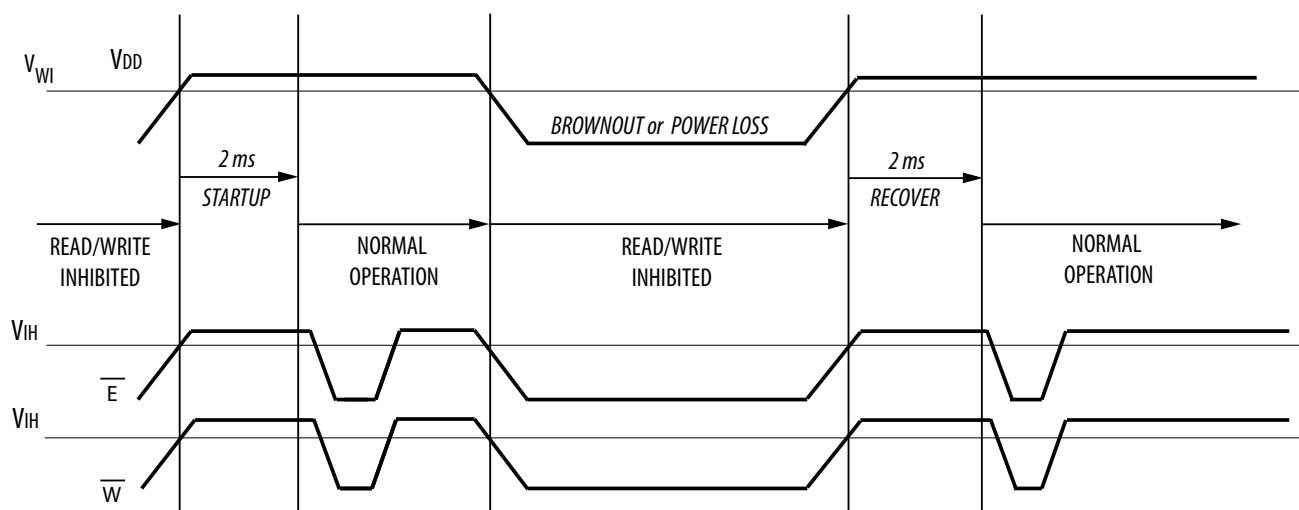


Table 2.3 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{lkg(I)}$	Input leakage current	All	-	± 1	μA
$I_{lkg(O)}$	Output leakage current	All	-	± 1	μA
V_{OL}	Output low voltage	$I_{OL} = +4 \text{ mA}$	-	0.4	V
		$I_{OL} = +100 \mu\text{A}$		$V_{SS} + 0.2$	V
V_{OH}	Output high voltage	$I_{OH} = -4 \text{ mA}$	2.4	-	V
		$I_{OH} = -100 \mu\text{A}$	$V_{DD} - 0.2$	-	V

Table 2.4 Power Supply Characteristics

Symbol	Parameter	Typical	Max	Unit
I_{DDR}	AC active supply current - read modes ¹ ($I_{OUT} = 0 \text{ mA}$, $V_{DD} = \text{max}$)	60	68	mA
I_{DDW}	AC active supply current - write modes ¹ ($V_{DD} = \text{max}$)	152	180	mA
I_{SB1}	AC standby current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$) <i>no other restrictions on other inputs</i>	9	14	mA
I_{SB2}	CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$)	5	9	mA

¹ All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance ¹

Symbol	Parameter	Typical	Max	Unit
C_{In}	Address input capacitance	-	6	pF
C_{In}	Control input capacitance	-	6	pF
$C_{I/O}$	Input/Output capacitance	-	8	pF

¹f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3.1	
Output load for all other timing parameters	See Figure 3.2	

Figure 3.1 Output Load Test Low and High



Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing ¹

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Read cycle time	35	-	ns
t_{AVQV}	Address access time	-	35	ns
t_{ELQV}	Enable access time ²	-	35	ns
t_{GLQV}	Output enable access time	-	15	ns
t_{BLQV}	Byte enable access time	-	15	ns
t_{AXQX}	Output hold from address change	3	-	ns
t_{ELQX}	Enable low to output active ³	3	-	ns
t_{GLQX}	Output enable low to output active ³	0	-	ns
t_{BLQX}	Byte enable low to output active ³	0	-	ns
t_{EHQZ}	Enable high to output Hi-Z ³	0	15	ns
t_{GHQZ}	Output enable high to output Hi-Z ³	0	10	ns
t_{BHQZ}	Byte high to output Hi-Z ³	0	10	ns

¹ \bar{W} is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

² Addresses valid before or at the same time \bar{E} goes low.

³ This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

Figure 3.3B Read Cycle 2

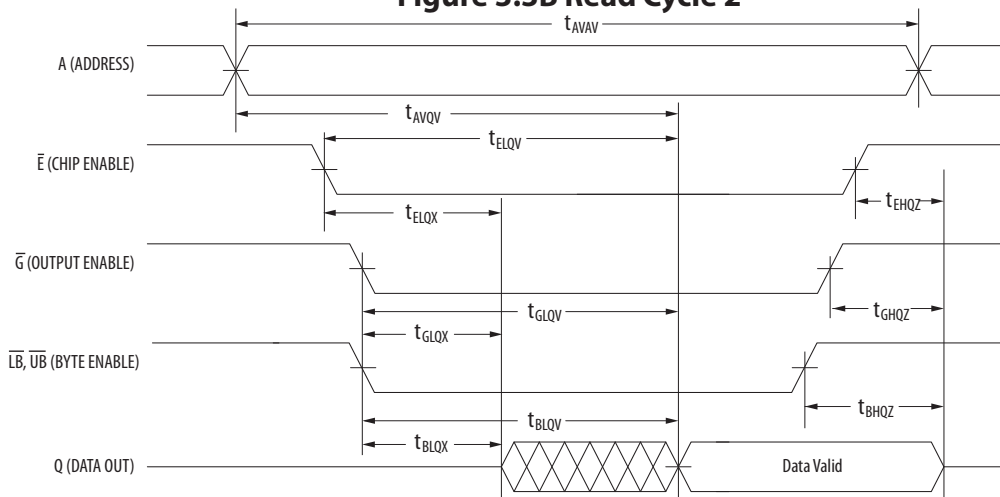


Table 3.4 Write Cycle Timing 1 (\overline{W} Controlled) ¹

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time ²	35	-	ns
t_{AVWL}	Address set-up time	0	-	ns
t_{AVWH}	Address valid to end of write (\overline{G} high)	20	-	ns
t_{AVWH}	Address valid to end of write (\overline{G} low)	20	-	ns
t_{WLWH} t_{WLEH}	Write pulse width (\overline{G} high)	15	-	ns
t_{WLWH} t_{WLEH}	Write pulse width (\overline{G} low)	15	-	ns
t_{DVWH}	Data valid to end of write	10	-	ns
t_{WHDX}	Data hold time	0	-	ns
t_{WLQZ}	Write low to data Hi-Z ³	0	15	ns
t_{WHQX}	Write high to output active ³	3	-	ns
t_{WHAX}	Write recovery time	12	-	ns

¹ All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} , \overline{E} or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.

³ This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(\text{max}) < t_{WHQX}(\text{min})$.

Figure 3.4 Write Cycle Timing 1 (\overline{W} Controlled)

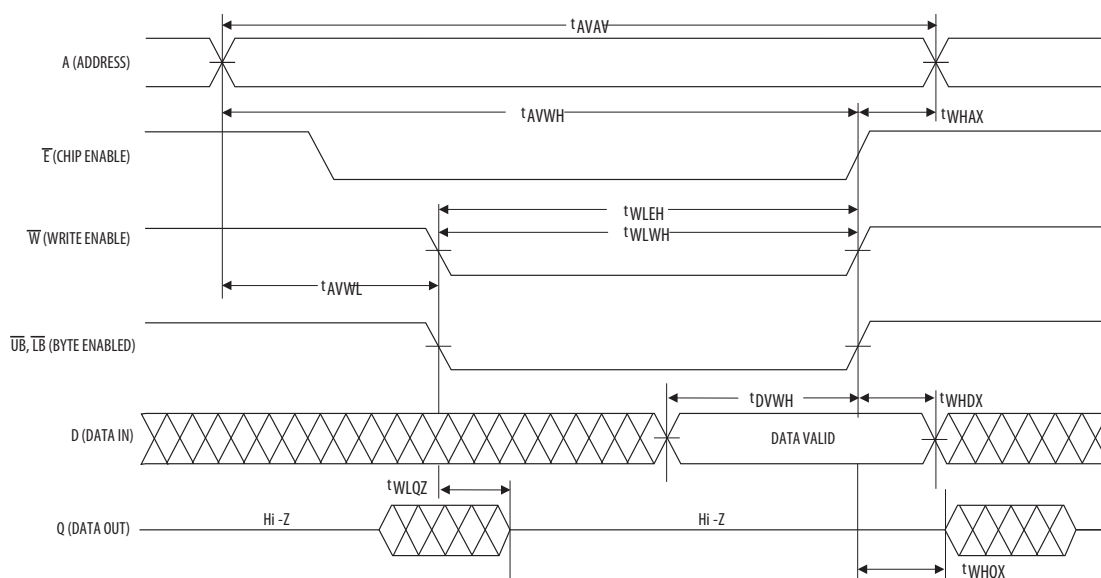


Table 3.5 Write Cycle Timing 2 (\bar{E} Controlled) ¹

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time ²	35	-	ns
t_{AVEL}	Address set-up time	0	-	ns
t_{AVEH}	Address valid to end of write (\bar{G} high)	20	-	ns
t_{AVEH}	Address valid to end of write (\bar{G} low)	20	-	ns
t_{ELEH} t_{ELWH}	Enable to end of write (\bar{G} high)	15	-	ns
t_{ELEH} t_{ELWH}	Enable to end of write (\bar{G} low) ³	15	-	ns
t_{DVEH}	Data valid to end of write	10	-	ns
t_{EHDX}	Data hold time	0	-	ns
t_{EHAX}	Write recovery time	12	-	ns

¹ All write occurs during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} , \bar{E} or \bar{UB}/\bar{LB} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.

³ If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

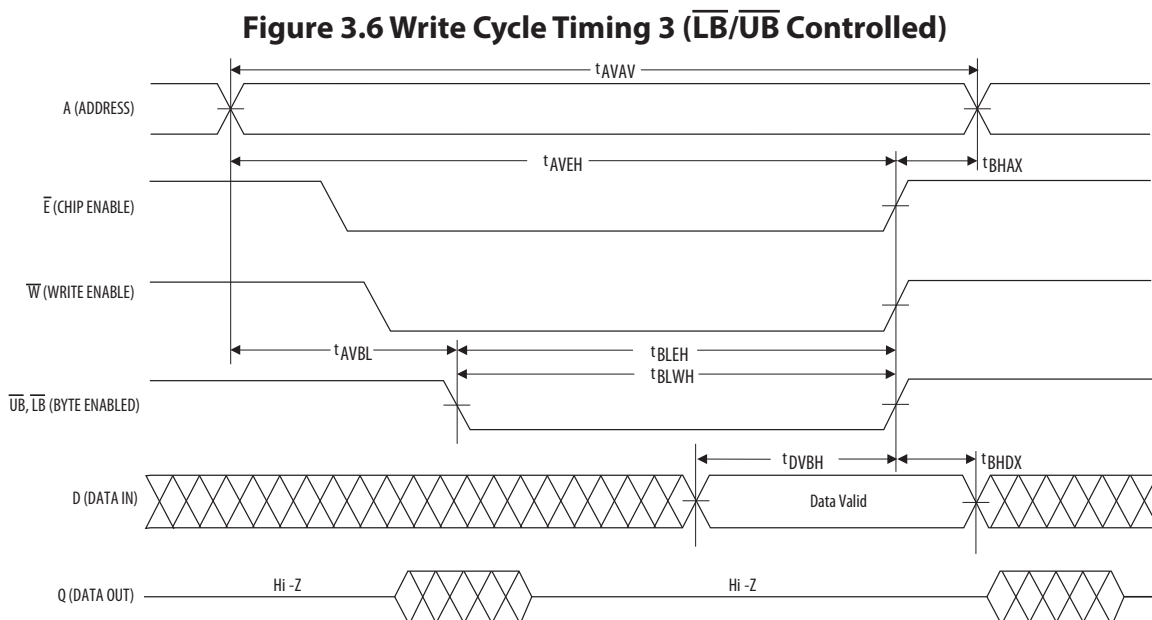
Figure 3.5 Write Cycle Timing 2 (\bar{E} Controlled)

Table 3.6 Write Cycle Timing 3 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled) ¹

Symbol	Parameter	Min	Max	Unit
t_{AVAV}	Write cycle time ²	35	-	ns
t_{AVBL}	Address set-up time	0	-	ns
t_{AVBH}	Address valid to end of write ($\overline{\text{G}}$ high)	20	-	ns
t_{AVBH}	Address valid to end of write ($\overline{\text{G}}$ low)	20	-	ns
t_{BLEH} t_{BLWH}	Write pulse width ($\overline{\text{G}}$ high)	15	-	ns
t_{BLEH} t_{BLWH}	Write pulse width ($\overline{\text{G}}$ low)	15	-	ns
t_{DVBH}	Data valid to end of write	10	-	ns
t_{BHDX}	Data hold time	0	-	ns
t_{BHAX}	Write recovery time	12	-	ns

¹ All write occurs during the overlap of $\overline{\text{E}}$ low and $\overline{\text{W}}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{\text{G}}$ goes low at the same time or after $\overline{\text{W}}$ goes low, the output will remain in a high impedance state. After $\overline{\text{W}}$, $\overline{\text{E}}$ or $\overline{\text{UB}}/\overline{\text{LB}}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between $\overline{\text{E}}$ being asserted low in one cycle to $\overline{\text{E}}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

Toggle MRAM (Parallel I/O)

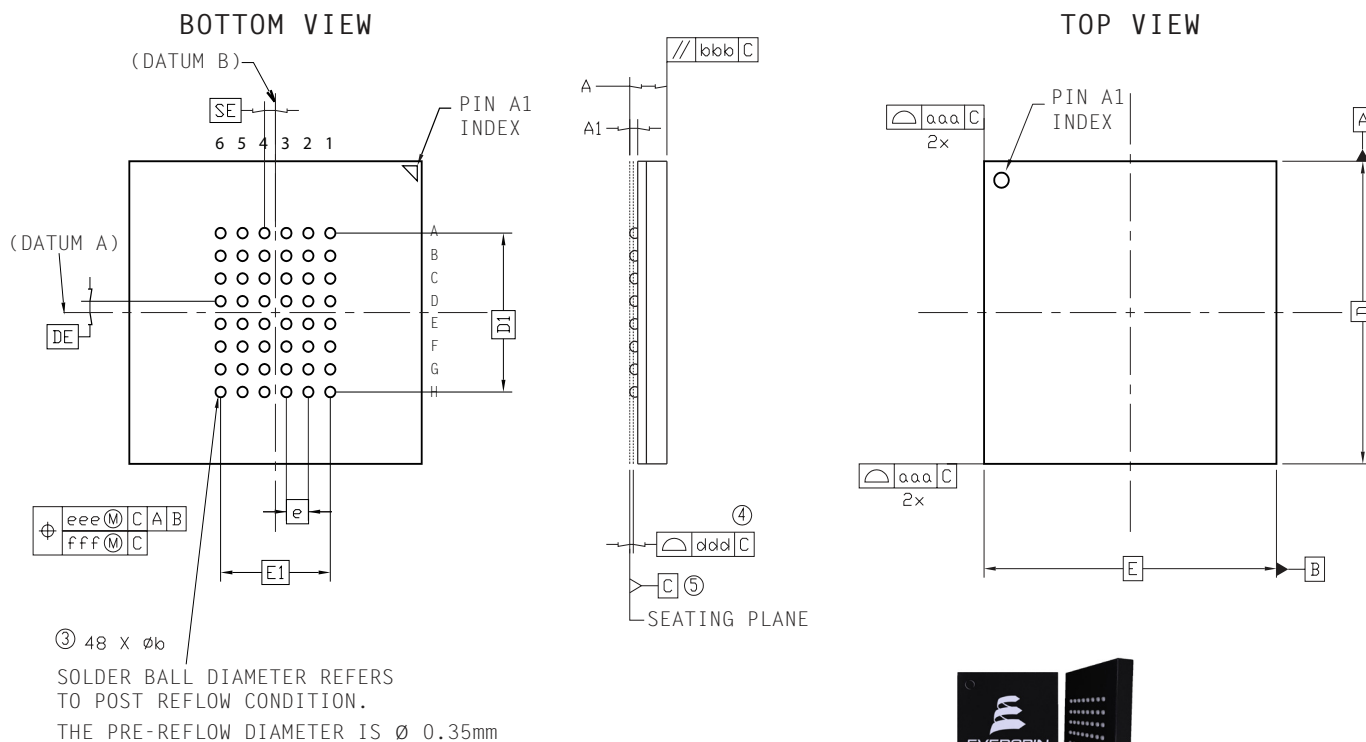
Example Ordering Part Number		Memory	Density	Type	I/O Width	Rev.	Temp	Package	Speed	Packing	Grade
		MR	3	A	16	A	C	MA	35	R	
MRAM	MR										
256 Kb	256										
1 Mb	0										
2 Mb	1										
4 Mb	2										
8 Mb	3										
16Mb	4										
32Mb	5										
Async 3.3v	A										
Async 3.3v Vdd and 1.8v Vddq	D										
Async 3.3v Vdd and 1.8v Vddq with 2.7v min. Vdd	DL										
8-bit	08										
16-bit	16										
Rev A	A										
Rev B	B										
Commercial	0 to 70°C	Blank									
Industrial	-40 to 85°C	C									
AEC Q-100 Grade 3	-40 to 85°C	P									
Extended	-40 to 105°C	V									
AEC Q-100 Grade 2	-40 to 105°C	N									
Automotive	-40 to 125°C	U									
AEC-Q100 Grade 1	-40 to 125°C	M									
44-TSOP2	YS										
48-BGA	MA										
35 ns	35										
45 ns	45										
Tray	Blank										
Tape and Reel	R										
Engineering Samples	ES										
Customer Samples	CS										
Mass Production	Blank										

Table 4.1 Available Parts

Grade	Temp Range	Package	Shipping Container	Order Part Number
Commercial	0 to +70 °C	48-BGA	Tray	MR3A16AMA35
			Tape & Reel	MR3A16AMA35R
		54-TSOP2	Tray	MR3A16AYS35
			Tape & Reel	MR3A16AYS35R
Industrial	-40 to +85°C	48-BGA	Tray	MR3A16ACMA35
			Tape & Reel	MR3A16ACMA35R
		54-TSOP2	Tray	MR3A16ACYS35
			Tape & Reel	MR3A16ACYS35R

5. MECHANICAL DRAWING

Figure 5.1 48-FBGA



Print Version Not To Scale

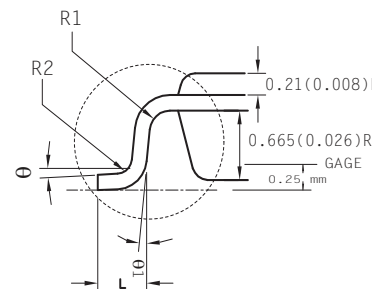
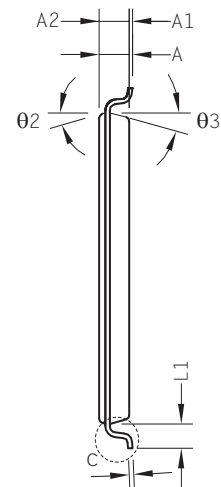
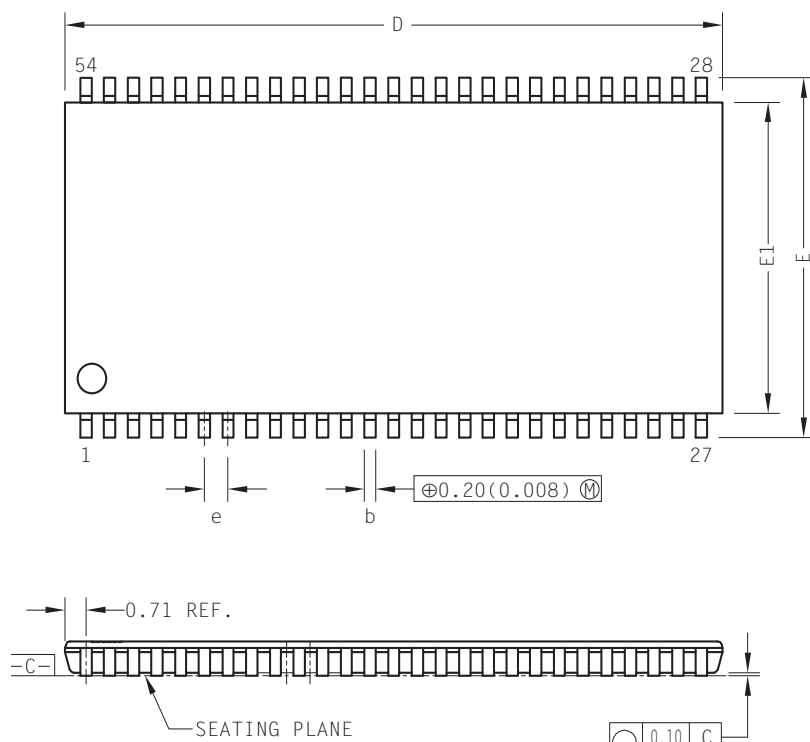
Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D	10.00 BSC		
E	10.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
DE	0.375 BSC		
SE	0.375 BSC		
e	0.75 BSC		

Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.10
eee	0.15
fff	0.08

- Dimensions in Millimeters.
- The 'e' represents the basic solder ball grid pitch.
- 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
- Dimension 'ddd' is measured parallel to primary datum C.
- Primary datum C (seating plane) is defined by the crowns of the solder balls.
- Package dimensions refer to JEDEC MO-205 Rev. G.

5. MECHANICAL DRAWING

Figure 5.2 54-TSOP2



Ref	Min	Nominal	Max
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.45
c	0.12		0.21
D	22.10	22.22	22.35
E	11.56	11.76	11.95
E1	10.03	10.16	10.29
e	0.80 BSC		
L	0.40	0.50	0.60
L1	0.80 REF		
R1	0.12	-	-
R2	0.12	-	0.25
θ	0°	-	8°
$\theta 1$	0.40	-	-
$\theta 2$	15° REF		
$\theta 3$	15° REF		

Print Version Not To Scale

1. Dimensions in Millimeters.
2. Package dimensions refer to JEDEC MS-024



6. REVISION HISTORY

Rev	Date	Description of Change
1.0	October 1, 2019	Initial data sheet release
1.1	March 11, 2020	Updatd Figure 4.1 to correct temperature designators.

7. HOW TO CONTACT US

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