



iCE40 UltraPlus 8:1 Mic Aggregation Demo

User Guide

FPGA-UG-02035-1.3

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Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|------------------|-------------------------------|
| CIC | Cascaded integrator-comb |
| DAC | Digital to Analog Converter |
| FPGA | Field Programmable Gate Array |
| I ² S | Inter-IC Sound |
| MDP | Mobile Development Platform |
| MSB | Most significant bit |
| PCM | Pulse Code Modulation |
| PDM | Pulse Density Modulation |
| TDM | Time-division multiplexing |

1. Introduction

This demo addresses a market opportunity to transfer data from up to eight Pulse Density Modulation (PDM) microphones on a single data wire using an I²S 8-ch aggregation format. I²S bus is widely used to communicate Pulse Code Modulation (PCM) audio data between integrated circuits in an electronic device. The standard I²S protocol is designed to transfer only two channels on a data line (LEFT and RIGHT).

1.1. Demo Design Overview

The iCE40 UltraPlus™ 8:1 Mic Aggregation demo implements a customized I²S bus using the iCE40 UltraPlus FPGA. The demo uses FPGA-B on the primary iCE40 UltraPlus Mobile Development Platform (MDP), plus a daughter board with eight PDM microphones for the input sources. Sound generated by the microphones can be heard through the onboard audio port.

Figure 1.1 shows an overview diagram of the 8:1 Mic Aggregation demo.

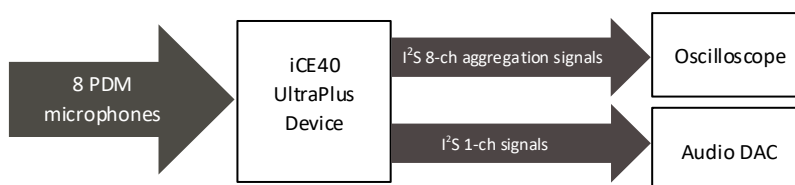


Figure 1.1. 8:1 Mic Aggregation Demo Overview

2. Functional Description

Figure 2.1 shows the 8:1 Mic Aggregation demo block diagram.

Each of the eight microphone's PDM format data streams are converted to PCM format using an efficient CIC Filter followed by a Compensation Filter. The eight PCM format streams then enter a serializer TDM (time division multiplexing) block that outputs the serialized data in an I²S 8-ch aggregation format to board header J30.

To drive audio to the headset jack, the I²S 8-ch aggregation format is sent to an I²S Decoder block. This, in turn, selects either the average of all eight PCM channels or one of the 8 channels to convert into standard 2-ch I²S format and send to the audio DAC amplifier. Channel selection is made by the board's MODE push button.

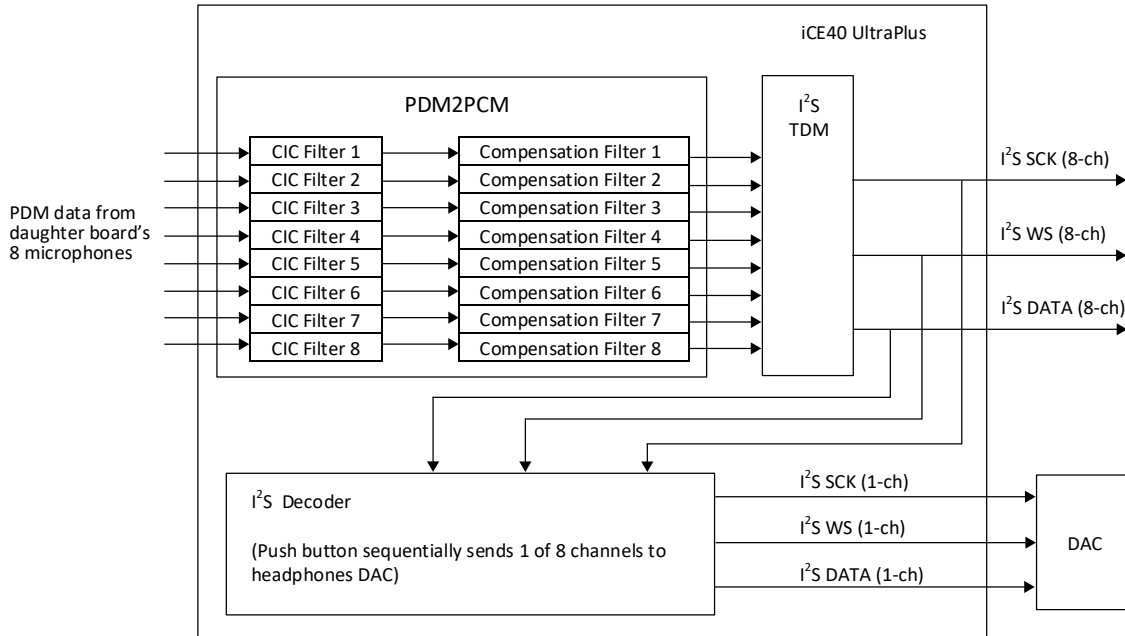


Figure 2.1. 8:1 Mic Aggregation Demo Block Diagram

3. Demo Package

The following hardware and software are required to run the iCE40 8:1 Mic Aggregation demo:

- **Hardware**
 - iCE40 UltraPlus MDP (PN: iCE40UP5K-MDP-EVN)
 - 8 to 1 Mic Aggregator Board (daughter board) (PN: LF-81AGG-EVN)
 - Standard 3.5 mm headphones
- **Software**
 - Lattice Radiant Programmer (Version 1.0 or later)
- **Demo Directory Structure**

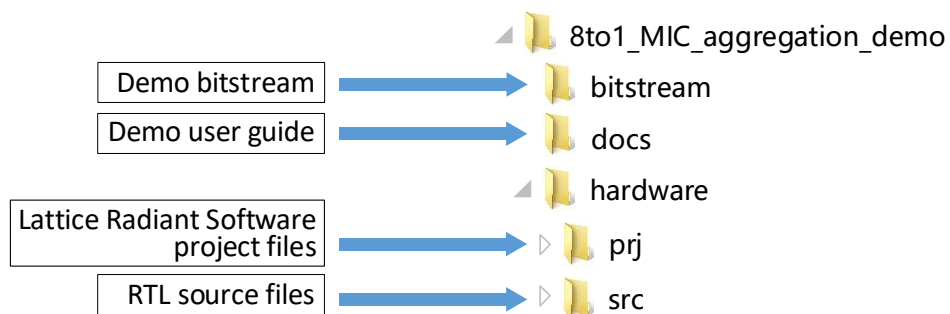


Figure 3.1. Directory Structure

4. iCE40 UltraPlus MDP and Resources

Figure 4.1 shows the top side of the iCE40 UltraPlus MDP and resources used for the demo.

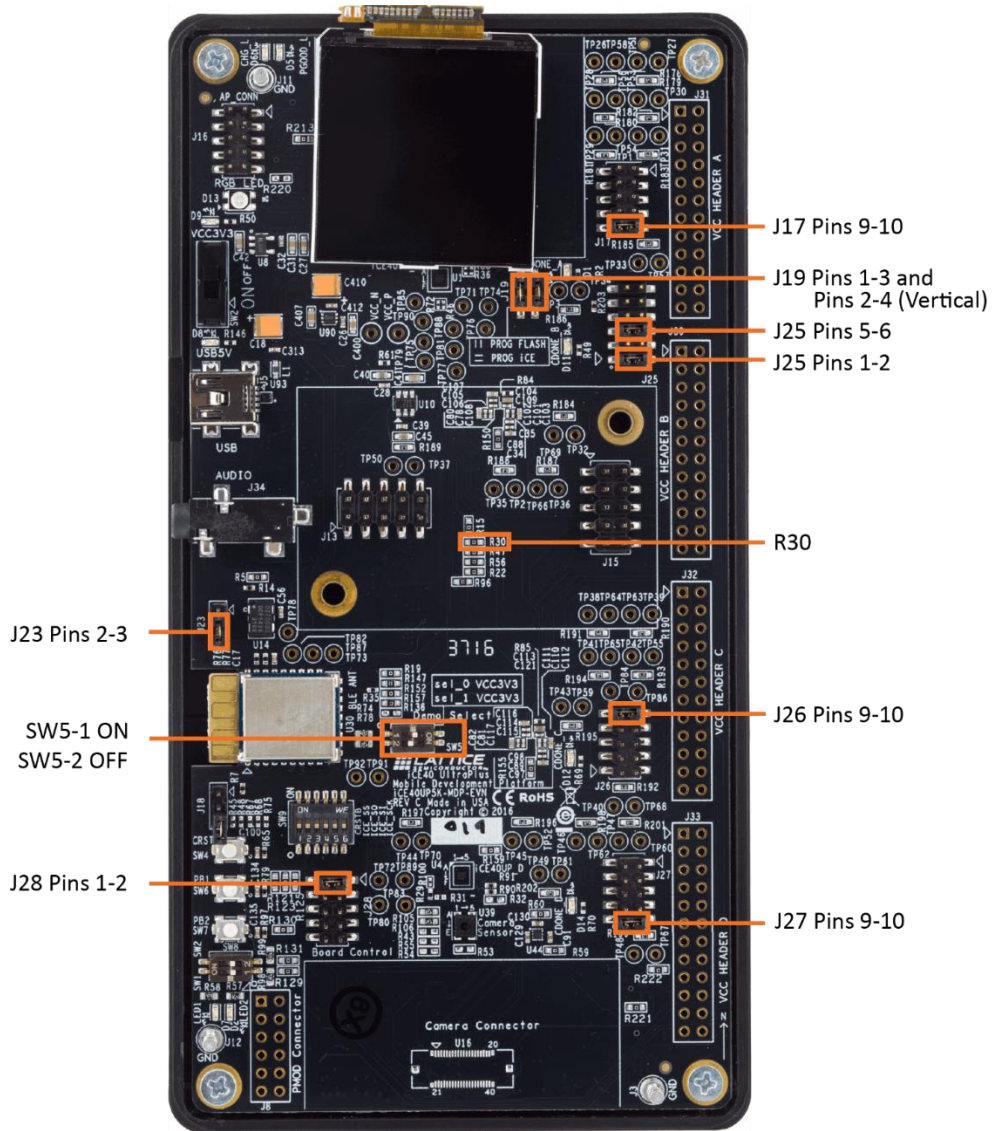


Figure 4.1. iCE40 UltraPlus MDP Configuration

4.1. Configuring the iCE40 UltraPlus MDP

Note that this demo uses FPGA-B. Refer to [Figure 4.1](#) for the location of jumpers and switches on the board.

To configure the board:

1. Install 0 Ω (0603) resistor or wire short at R30 if not installed.
2. Shunt pins 9-10 on J17, J26 and J27.
3. Shunt pins 1-2 and pins 5-6 on J25.
4. Shunt pins 1-2 on J28.
5. Shunt pins 2-3 on J23.
6. Shunt pins 1-3 and pins 2-4 (Vertical) on J19.
7. Set SW5-1 to ON and SW5-2 to OFF.
8. Connect the 8 to 1 Mic Aggregator Board on top of the MDP board.
9. Connect a standard 3.5 mm headphones to the audio jack at J34.

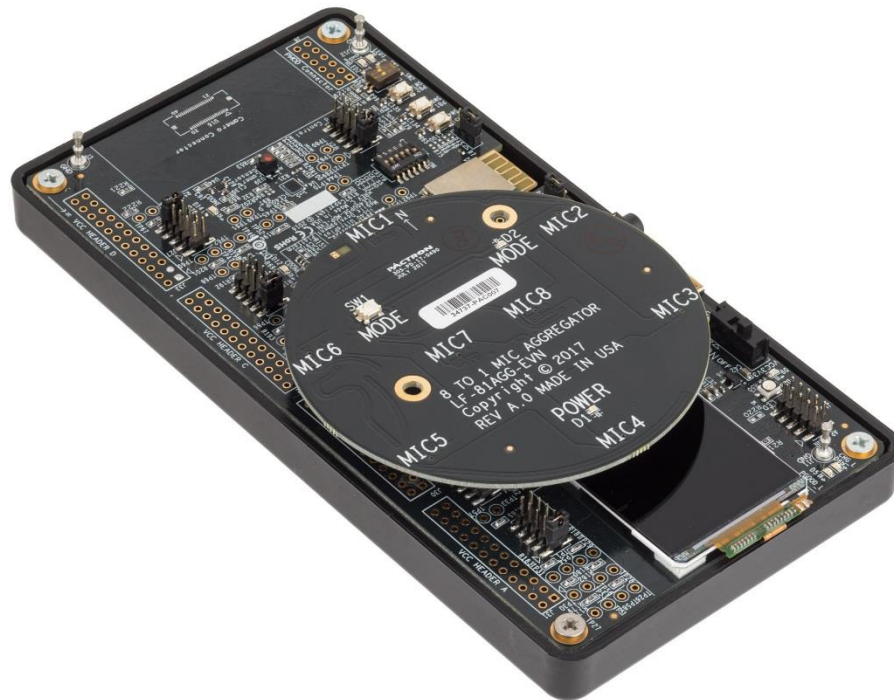


Figure 4.2. iCE40 UltraPlus MDP and 8 to 1 Mic Aggregator Board

5. Programming the Bitstreams to the iCE40 UltraPlus MDP

To program SPI flash using Lattice Radiant Programmer:

1. Connect the iCE40 UltraPlus MDP to the PC using a USB cable.
2. Power ON the iCE40 UltraPlus MDP.
3. Start the Lattice Radiant Programmer software tool (version 1.0 or later).
4. In the **Getting Started** dialog box, select **Create a new project file from a scan** and click **OK**.
5. Select the **Device Family** and **Device** as shown in [Figure 5.2](#).
6. Right-click on the device and select **Device Properties**. Apply the settings as shown in [Figure 5.1](#).

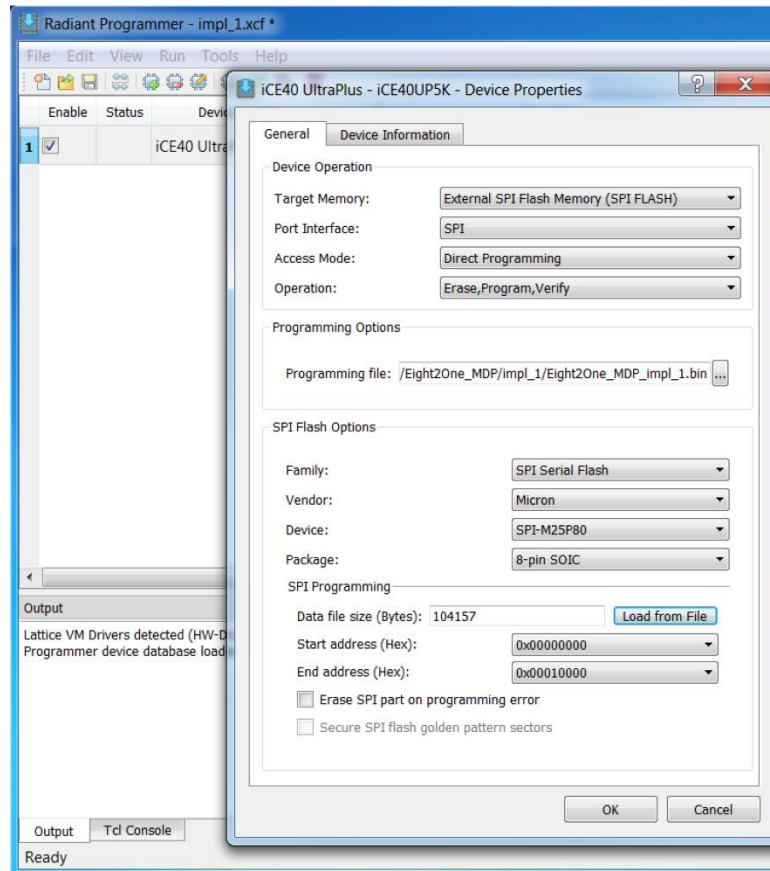


Figure 5.1. Device Properties

- Target Memory: Set to External SPI Flash Memory (SPI FLASH).
 - Port Interface: Set to SPI.
 - Access Mode: Set to Direct Programming.
 - Operation: Set to Erase, Program, Verify mode.
 - **Programming File**: Load the bitstream file for demo located in folder (/Demo/Bin/*.bin).
 - **SPI Flash Options**: Select the Flash chip as shown in [Figure 5.1](#).
 - Load from File: Click to refresh fields such as Data file size and End address (Hex).
7. Click **OK** to exit the **Device Properties** dialog box.
 8. Click the **Program** button on the main interface to download the bitstream file.

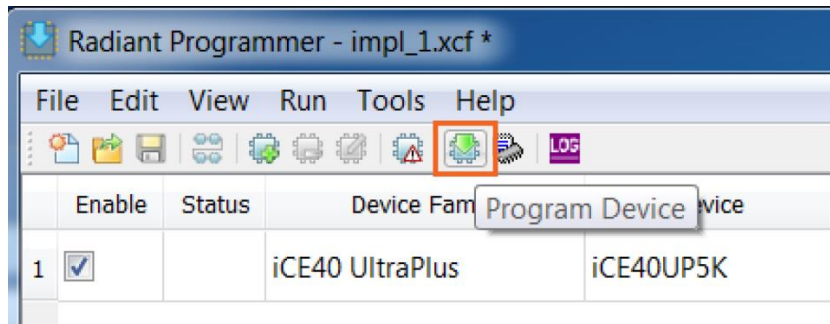


Figure 5.2. Program Device Button

6. Running the Demo

6.1. Using Headphones

When a bitstream is loaded into the FPGA-B on the iCE40 UltraPlus MDP, the daughter board's green POWER LED and yellow MODE LED turn ON to indicate default selection mode of all eight microphones. Sound is heard over the headphones.

To sequence through each individual microphone, push and release the MODE button on the 8 to 1 Mic Aggregator Board.

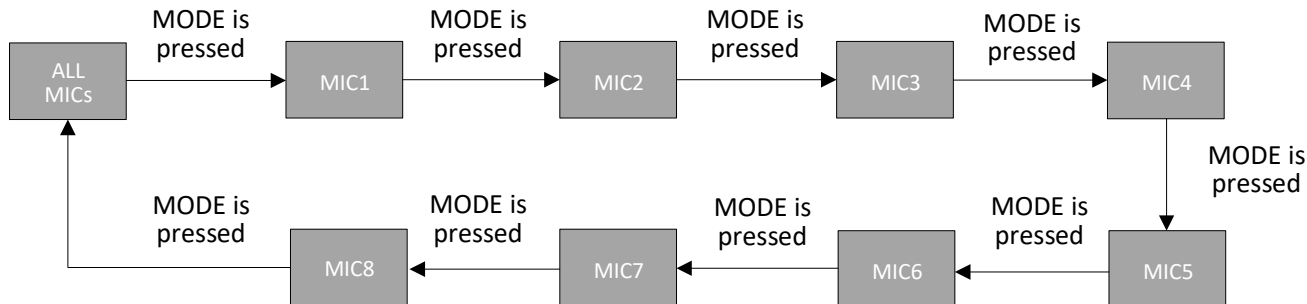


Figure 6.1. Mode Push Button Control Sequences Selected Microphone

The MODE LED is ON while the ALL MICs mode is selected and while the MODE button is pressed.



Figure 6.2. 8 to 1 Mic Aggregator Board (Daughter Board)

6.2. Oscilloscope Connection Points

You can use an oscilloscope to observe the I²S 8-channel aggregation signals and the I²S 2-channel standard signals. The signals are available at FPGA-B header J30 on the iCE40 UltraPlus MDP.

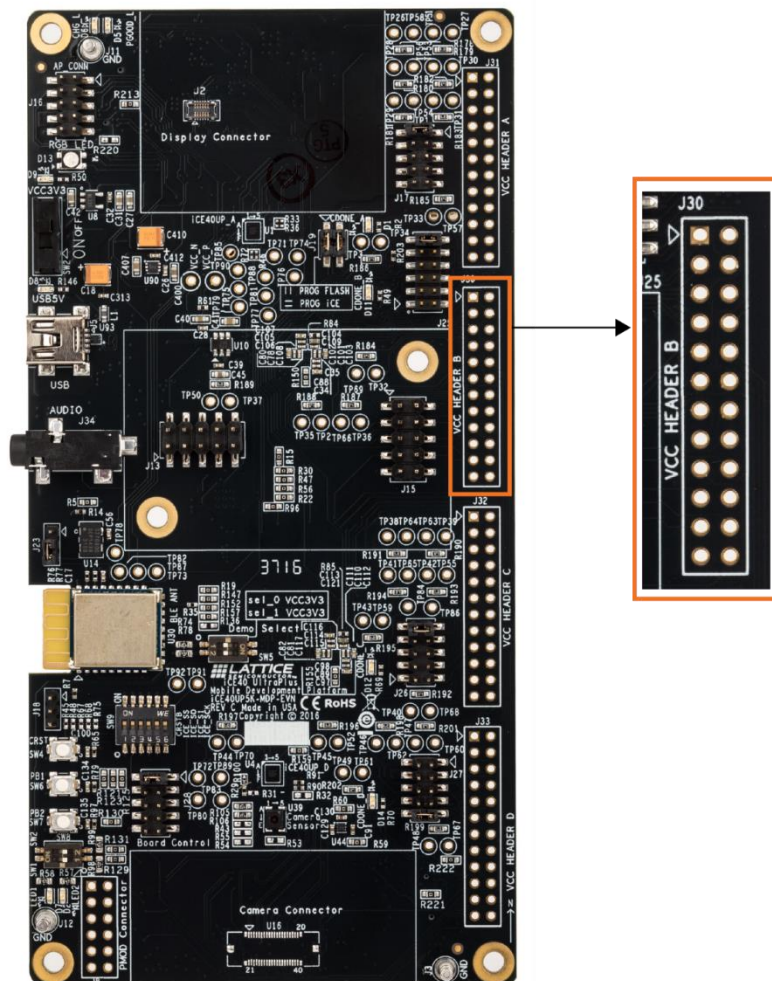


Figure 6.3. J30 Section on MDP Board

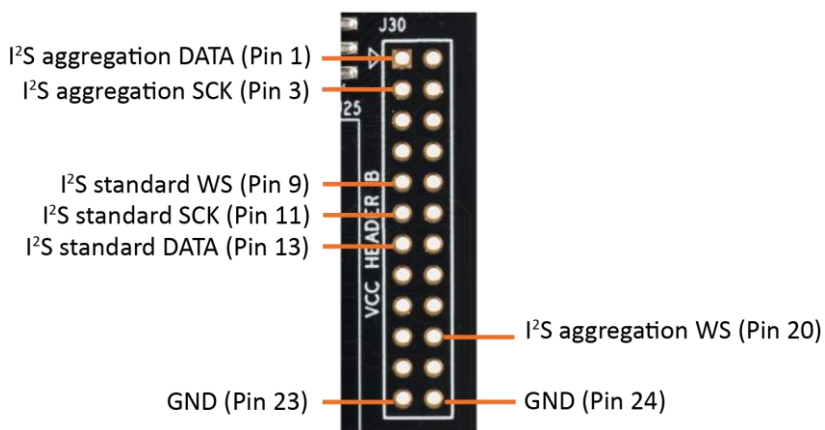


Figure 6.4. Header to Connect to the Oscilloscope

6.3. I²S Aggregation Signal Format

Figure 6.5 shows the aggregation TDM format for eight channels. The vertical lines indicate the first most significant bit (MSB) of each microphone channel.

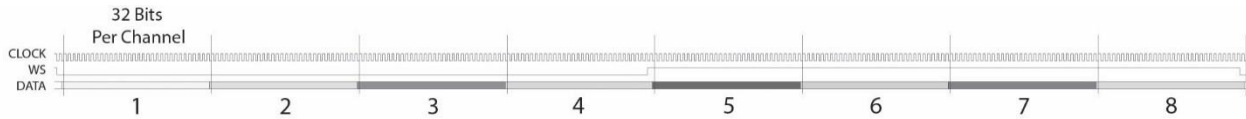


Figure 6.5. Aggregation TDM Format for 8 Channels

Figure 6.6 shows the I²S aggregation for channel 1.

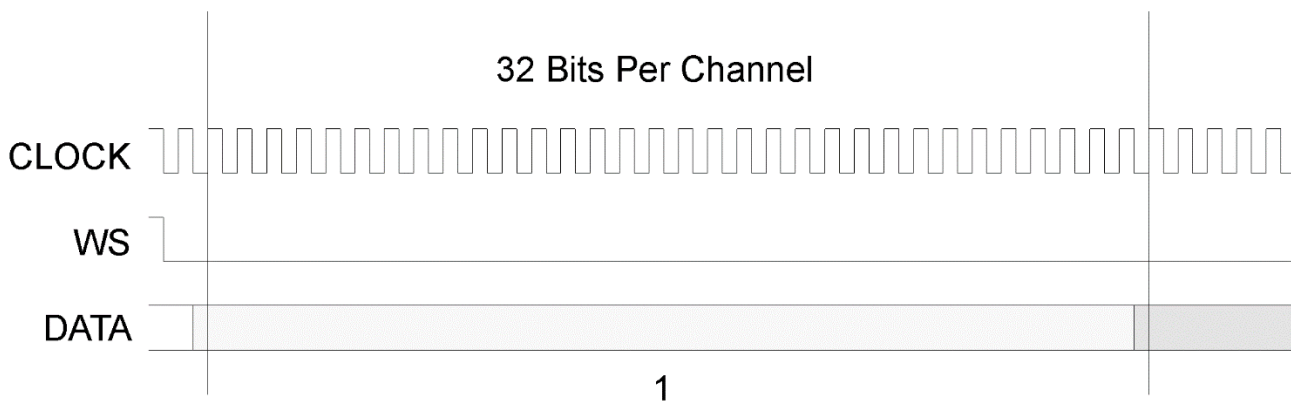


Figure 6.6. I²S Aggregation for Channel 1

Figure 6.7 shows the I²S aggregation for channel 8.

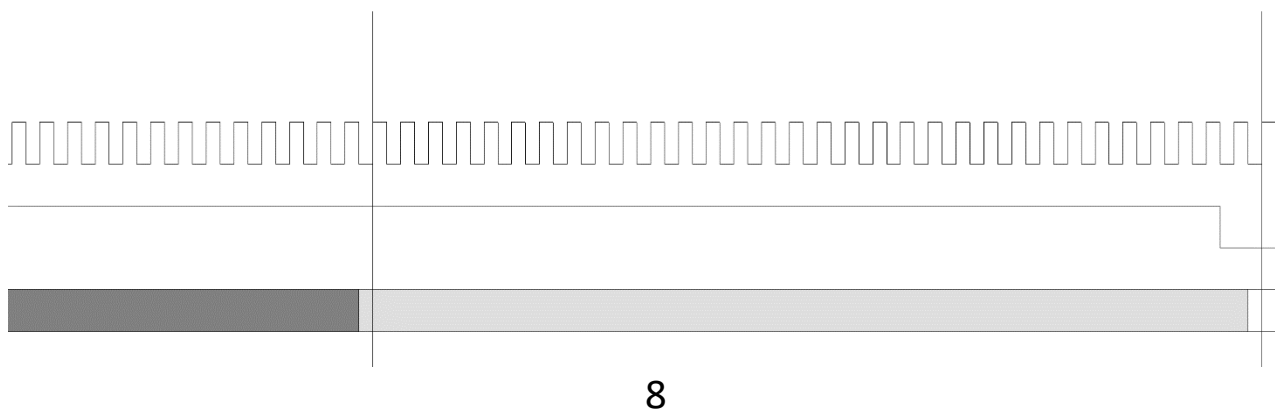


Figure 6.7. I²S Aggregation for Channel 8

6.4. Measured Oscilloscope I²S Aggregation Signals

Figure 6.8 shows the measured I²S aggregation signals for the eight channels.

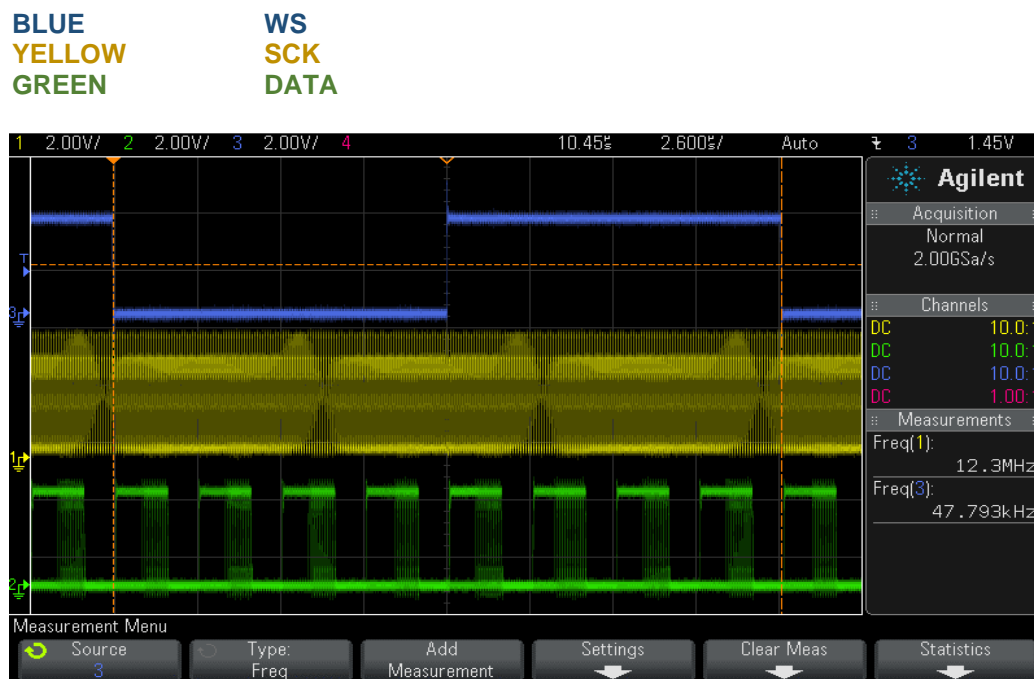


Figure 6.8. Measured I²S Aggregation Signals for 8 Channels

Figure 6.9 shows the measured I²S aggregation signals for channel 1.

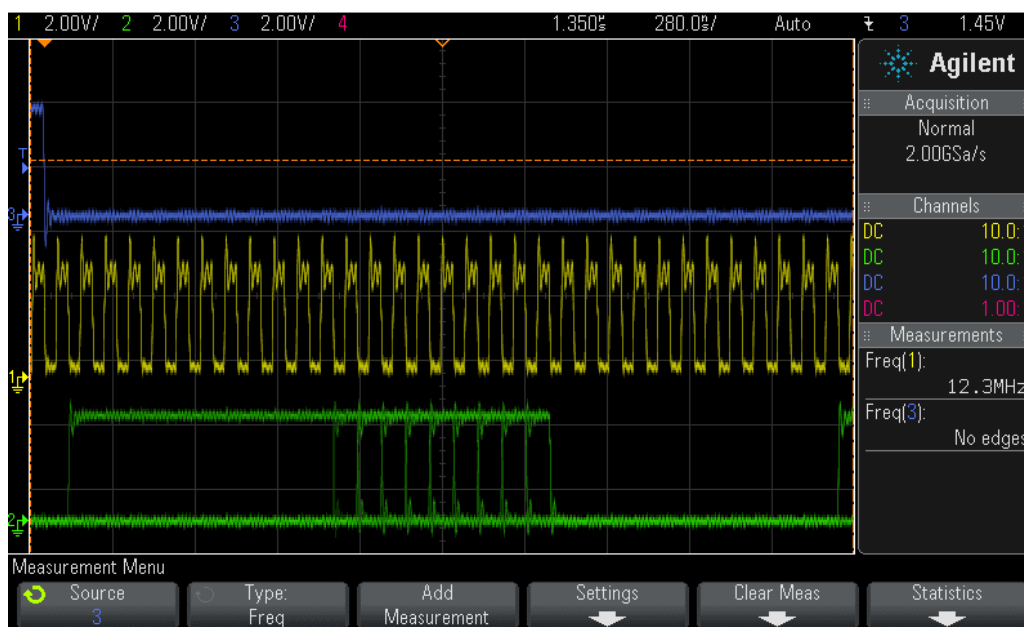
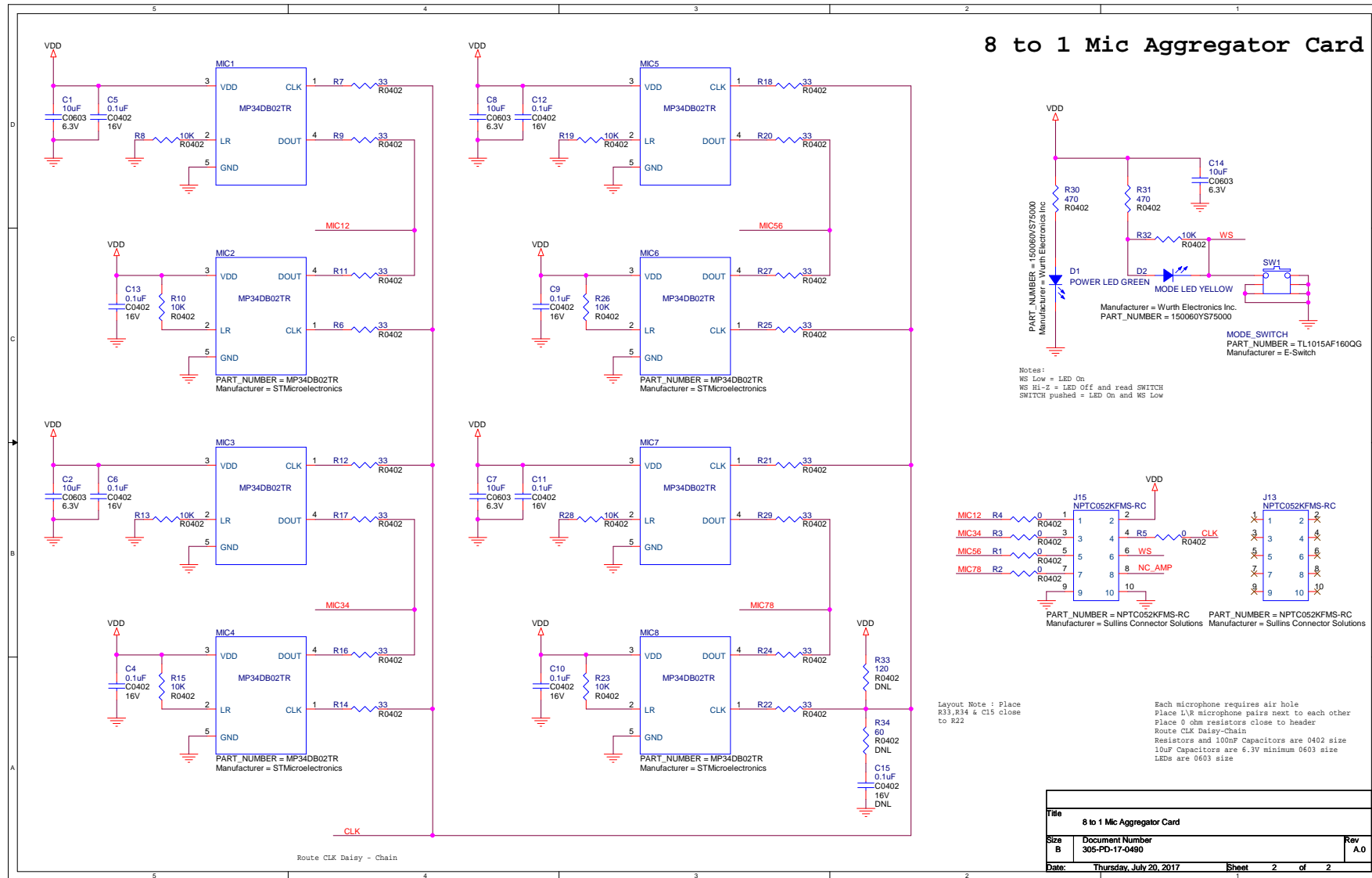


Figure 6.9. Measured I²S Aggregation Signals for Channel 1

Appendix A. Schematic Diagram



8 to 1 Mic Aggregator Card

Appendix B. Bill of Materials

8 to 1 Mic Aggregator Board Bill of Materials

| Item | Reference Designator | Qty | Description | Package | Manufacturer | Part Number | Notes |
|------|--|-----|---|----------------------|---------------------|--------------------|-------|
| 1 | C1,C2,C7,C8,C14 | 5 | Capacitor Ceramic 10 uF 20% 6.3 V X5R 0603 | 0603 | Murata Electronics | GRM188R61A475ME15D | — |
| 2 | C4,C5,C6,C9,C10,C11,C12,C13 | 8 | Capacitor Ceramic 0.1 uF 10% 16 V X7R 0402 | 0402 | Murata Electronics | GRM155R71C104KA88J | — |
| 3 | C15 | 1 | Capacitor Ceramic 0.1 uF 10% 16 V X7R 0402 | 0402 | Murata Electronics | GRM155R71C104KA88J | DNL |
| 4 | D1 | 1 | LED Green 0603 | 0603 | Würth | 150060VS75000 | — |
| 5 | D2 | 1 | LED Yellow 0603 | 0603 | Würth | 150060YS75000 | — |
| 6 | J13,J15 | 2 | Connector Header Female 2x5 0.1" Pitch | 2x5 0.1" Pitch | Sullins | NPTC052KFMS-RC | — |
| 7 | MIC1,MIC2,MIC3,MIC4,MIC5,MIC6,MIC7,MIC8 | 8 | Microphone PDM Omnidirectional -26 DB | RHLGA (3x4x1) mm 4LD | STMicro-electronics | MP34DB02TR | — |
| 8 | R1,R2,R3,R4,R5 | 5 | Resistor 0.0 Ω 5% 1/16W 0402 | 0402 | Yageo | RC0402JR-070RL | — |
| 9 | R6,R7,R9,R11,R12,R14,R16,R17,R18,R20,R21,R22,R24,R25,R27,R29 | 16 | Resistor 33 Ω 5% 1/16W 0402 | 0402 | Yageo | RC0402JR-0733RL | — |
| 10 | R8,R10,R13,R15,R19,R23,R26,R28,R32 | 9 | Resistor 10 K Ω 5% 1/16W 0402 | 0402 | Yageo | RC0402JR-0710KL | — |
| 11 | R30,R31 | 2 | Resistor 470 Ω 5% 1/16W 0402 | 0402 | Yageo | RC0402FR-07470RL | — |
| 12 | R33 | 1 | Resistor 120 Ω 1% 1/16W 0402 | 0402 | Yageo | RC0402FR-07120RL | DNL |
| 13 | R34 | 1 | Resistor 62 Ω 5% 1/16W 0402 | 0402 | Yageo | RC0402FR-0762RL | DNL |
| 14 | SW1 | 1 | Switch Push Button Momentary SPST-NO 0.05A 12 V | 3.90 mm x 2.90 mm | E-Switch | TL1015AF160QG | — |
| 15 | 8 to 1 MIC AGGREGATOR CARD REVA.0 PCB | 1 | Bare PCB | — | Pactron | 305-PD-17-0490 | — |

Technical Support Assistance

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Document Revision 1.3, October 2020

| Section | Change Summary |
|---|---|
| Disclaimers | Added this section. |
| Acronyms in This Document | Added this section. |
| Demo Package | Updated Figure 3.1. Directory Structure . |
| iCE40 UltraPlus MDP and Resources | Updated the iCE40 UltraPlus MDP configuration procedure. |
| Programming the Bitstreams to the iCE40 UltraPlus MDP | Updated SPI flash programming procedure. |
| — | Minor adjustments in formatting and style |

Document Revision 1.2, September 2020

| Section | Change Summary |
|---|---|
| All | Updated the software tool to Lattice Radiant Software (Version 1.0) or to Lattice Radiant Programmer. |
| Programming the Bitstreams to the iCE40 UltraPlus MDP | Updated Device Properties image (Figure 5.1) and description. |
| | Added Figure 5.2, Program Device Button. |
| Resource Utilization | Removed this section. |

Document Revision 1.1, November 2017

| Section | Change Summary |
|------------------------|---|
| Introduction | Added contents. |
| Functional Description | Added contents. |
| Resource Utilization | Updated Table 7.1 Resource Utilization. |

Document Revision 1.0, October 2017

| Section | Change Summary |
|---------|------------------|
| All | Initial release. |



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