



### **General Description**

The WSD4090DN56 advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

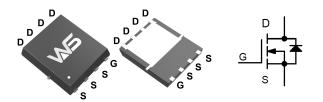
## **Product Summery**

BVDSS	RDSON	ID
40V	4.0mΩ	90A

## **Applications**

- Battery protection
- Load switch
- Uninterruptible power supply

## **DFN5X6-8L Pin Configuration**



## **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	90	Α
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	62	Α
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	190	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	56	mJ
I <sub>AS</sub>	Avalanche Current	34	Α
P <sub>D</sub> @T <sub>c</sub> =25℃	Total Power Dissipation⁴	52.1	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	$^{\circ}$
TJ	Operating Junction Temperature Range	-55 to 150	$^{\circ}$

#### **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit	
$R_{ heta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>		62	°C/W	
R <sub>eJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>		2.4	°C/W	



## Electrical Characteristics (TJ=25 °C, unless otherwise noted)

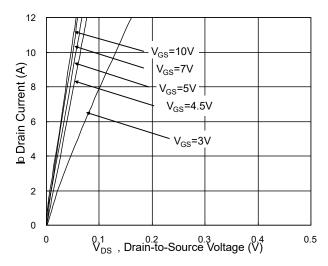
Symbol	<u>Parameter</u>	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25℃, I <sub>D</sub> =1mA		0.043		V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =20A		4.0	5.5	mΩ
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =15A		5.9		mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.6	2.9	4.0	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient			-6.94		mV/℃
	Danier Course Lockers Courset	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25℃			2	
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55℃			10	- uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$			±100	nA
gfs	Forward Transconductance	VDS=10V,ID=5A		24		S
$Q_g$	Total Gate Charge (10V)	V <sub>DS</sub> =20V , V <sub>GS</sub> =10V , I <sub>D</sub> =40A		20		nC
Q <sub>gs</sub>	Gate-Source Charge			5.7		
Q <sub>gd</sub>	Gate-Drain Charge			9.4		
T <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD}$ =30V , $V_{GEN}$ =10V , $R_{G}$ =1 $\Omega$ , $I_{D}$ =1A , $RL$ =15 $\Omega$ .		10.9		- ns
Tr	Rise Time			16.4		
T <sub>d(off)</sub>	Turn-Off Delay Time			18		
T <sub>f</sub>	Fall Time			29		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V , V <sub>GS</sub> =0V , f=1MHz		1492	1940	pF
C <sub>oss</sub>	Output Capacitance			391		
C <sub>rss</sub>	Reverse Transfer Capacitance			59		
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			70	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =20A , T <sub>J</sub> =25℃			1.3	V

#### Note

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =20V, $V_{GS}$ =10V,L=0.1mH,I<sub>AS</sub>=34A
- 4.The power dissipation is limited by 150  $^{\circ}\mathrm{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



## **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

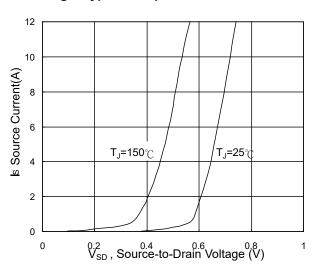


Fig.3 Forward Characteristics of Reverse

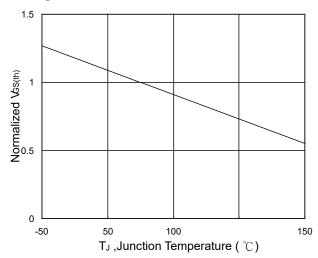


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

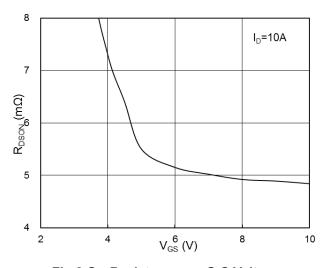


Fig.2 On-Resistance vs. G-S Voltage

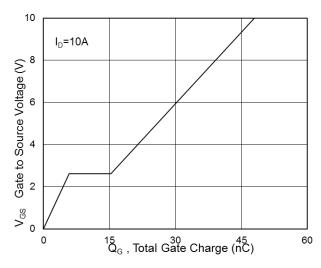


Fig.4 Gate-Charge Characteristics

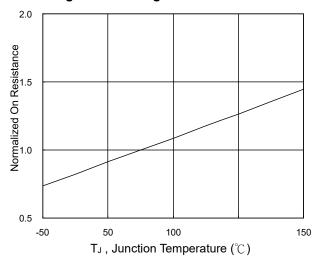
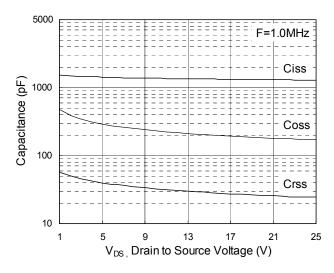


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>



# **Typical Characteristics**



1000.00 100.00 100us 10.00 10ms 100ms 1.00 DC # 0.10  $T_C=25\,^{\circ}\mathrm{C}$ Single Pulse 0.01 0.1 10 100  $V_{DS}(V)$ 

Fig.7 Capacitance

Fig.8 Safe Operating Area

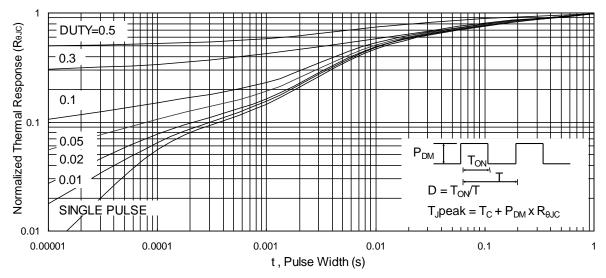


Fig.9 Normalized Maximum Transient Thermal Impedance



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