

# **AC6921A Datasheet**

**Zhuhai Jieli Technology Co.,LTD**

**Version: V1.0**

**Date: 2018.04.20**

## AC6921A Features

### High performance 32-bit RISC CPU

- RISC 32-bit CPU
- DC-160MHz operation
- Support DSP instructions
- 64Vectored interrupts
- 4 Levels interrupt priority

### Flexible I/O

- 33 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

### Peripheral Feature

- One full speed USB 2.0 OTG controller
- One audio interface supports IIS, left adjusted, right adjusted and DSP mode
- Four multi-function 16-bit timers, support capture and PWM mode
- Three 16-bit PWM generator for motor driving
- One 16-bit active parallel port
- One full-duplex basic UART
- Two full-duplex advanced UART
- Three SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- One SPDIF receiving interface without analog amplify
- One Quadrate decoder
- Watchdog
- 2 Crystal Oscillator
- 16-bit Stereo DAC with headphone amplifier, SNR  $\geq$  95dB
- 1 channel ADC , SNR  $\geq$  90dB
- 1 channel MIC amplifier
- 2 channels Stereo analog MUX
- 14 channels 10-bit ADC
- 2 channels 8 levels Low Voltage Detector
- Power-on reset
- Embedded PMU support low power mode

### Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V5.0+BR+EDR+BLE specification

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and  $\pi/4$  DQPSK all packet types
- Provides +2dbm transmitting power
- receiver with -89dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdpl2cap profile

### FM Tuner

- Support worldwide frequency band 76-108MHz
- Fully integrated digital low-IF tuner & frequency synthesizer
- Autonomous search tuning
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
- Programmable de-emphasis (50/75 uS)
- Receive signal strength indicator (RSSI)
- Radio search in multi-channel simultaneously
- Digital volume control

### Power Supply

- VBAT is 2.2V to 5.5V
- VDDIO is 2.2V to 3.6V
- RTCVDD is 2.2V to 3.6V

### Packages

- LQFP48(7mm\*7mm)

### Temperature

- Operating temperature: -20°C to +70°C
- Storage temperature: -65°C to +150°C

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

# 1、 Pin Definition

## 1.1 Pin Assignment

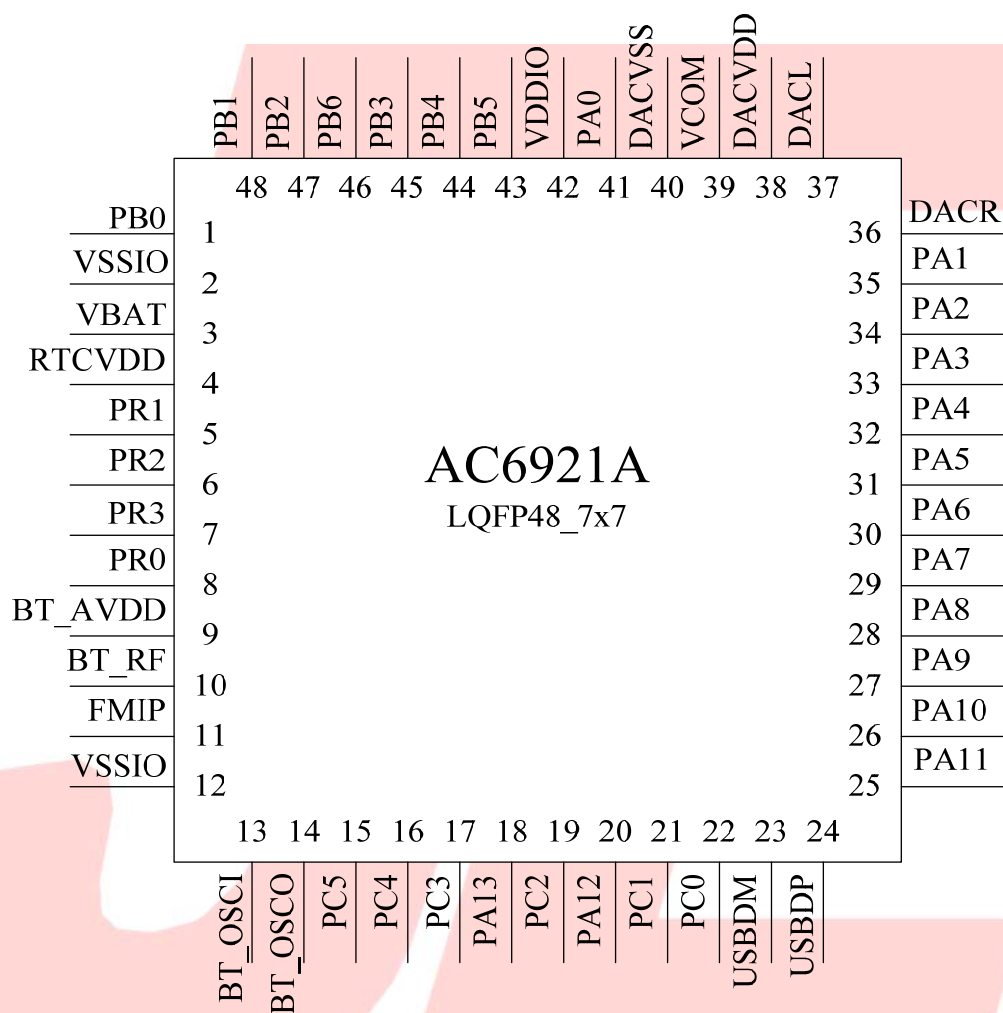


Figure 1-1 AC6921A\_LQFP48 Package Diagram

## 1.2 Pin Description

**Table 1-1 AC6921A\_LQFP48 Pin Description**

| PIN NO. | Name    | I/O Type | High Drive (mA) | Function           | Other Function   |
|---------|---------|----------|-----------------|--------------------|--|
| 1       | PB0     | I/O      | 8               | GPIO               | CLKOUT0:<br>UART1TXA: Uart1 Data Out(A);<br>SPI2CLKA: SPI2 Clock(A);<br>SD1DAT0B: SD1 Data0(B);<br>ALNK_SCLKB: Audio Link Serial Clock (B);<br>SD0DAT3B: SD0 Data3(B);<br>ADC6: ADC Input Channel 6;<br>Touch0: Touch Input Channel 0; |
| 2       | VSSIO   | P        | /               | Ground             |  |
| 3       | VBAT    | P        | /               | LDO Power          |  |
| 4       | RTCVDD  | P        | /               | RTC Power 3.3v     |  |
| 5       | PR1     | I/O      | 10              | RTCIO1 (output 0V) | RESET1:<br>ADC12: ADC Input Channel 12;  |
| 6       | PR2     | I/O      | 10              | RTCIO2 (pull up)   | RESET2:<br>ADC12: ADC Input Channel 12;  |
| 7       | PR3     | I/O      | 10              | RTCIO3 (pull up)   | RESET3:  |
| 8       | PR0     | I/O      | 10              | RTCIO0             | RESET0:<br>OSCO_32K  |
| 9       | BT_AVDD | P        | /               | BT Power 1.3v      |  |
| 10      | BT_RF   | P        | /               |                    |  |
| 11      | FMIP    | I        | /               |                    |  |
| 12      | VSSIO   | P        | /               | Ground             |  |
| 13      | BT_OSCI | I        | /               | BT OSC In          |  |
| 14      | BT_OSCO | O        | /               | BT OSC Out         |  |
| 15      | PC5     | I/O      | 24              | GPIO               | SD1CLKA: SD1 Clock(A);<br>SPI1DOB: SPI1 Data Out(B);<br>UART2RXD: Uart2 Data In(B);<br>IIC_SDA_B: IIC SDA(B);<br>COM0: LCD COM Output 0;<br>SEG21: LCD SEG Output21;   |
| 16      | PC4     | I/O      | 24              | GPIO               | SD1CMDA: SD1 Command(A);<br>SPI1CLKB: SPI1 Clock(B);   |

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

|    |       |     |    |                                     |   |
|----|-------|-----|----|-------------------------------------|---|
|    |       |     |    |                                     | UART2TXD: Uart2 Data Out(B);<br>IIC_SCL_B: IIC SCL(B);<br>COM1: LCD COM Output 1;<br>SEG20: LCD SEG Output20;   |
| 17 | PC3   | I/O | 24 | GPIO                                | SD1DAT0A: SD1 Data0(A);<br>SPI1DIB: SPI1 Data In(B);<br>UART0RXC: Uart0 Data In(C);<br>TMR3: Timer3 Clock Input;<br>COM2: LCD COM Output 2;<br>SEG19: LCD SEG Output19;<br>ADC10: ADC Input Channel 10; |
| 18 | PA13  | I/O |    | GPIO                                | ALNK_DAT2A: Audio Link Data2(A);<br>SEG13: LCD SEG Output13;  |
| 19 | PC2   | I/O | 24 | GPIO                                | IIC_SDA_C: IIC SDA(C);<br>UART0TXC: Uart0 Data Out(C);<br>COM3: LCD COM Output 3;<br>SEG18: LCD SEG Output18;   |
| 20 | PA12  | I/O | 24 | GPIO                                | CAP2: Timer2 Capture;<br>ALNK_DAT1A: Audio Link Data1(A);<br>SEG12: LCD SEG Output12;   |
| 21 | PC1   | I/O | 24 | GPIO                                | IIC_SCL_C: IIC SCL(C);<br>SD1DAT2A: SD1 Data2(A);<br>UART1RXB: Uart1 Data In(B);<br>COM4: LCD COM Output 4;<br>SEG17: LCD SEG Output17;   |
| 22 | PC0   | I/O | 24 | GPIO                                | SD1DAT3A: SD1 Data3(A);<br>UART1TXB: Uart1 Data Out(B);<br>COM5: LCD COM Output 5;<br>SEG16: LCD SEG Output16;  |
| 23 | USBDM | I/O | 4  | USB Negative<br>Data<br>(pull down) | UART1RXD: Uart1 Data In(D);<br>SPI2DOB: SPI2 Data Out(B);<br>IIC_SDA_A: IIC SDA(A);<br>ADC11: ADC Input Channel 11;   |
| 24 | USBDP | I/O | 4  | USB Positive<br>Data<br>(pull down) | UART1TXD: Uart1 Data Out(D);<br>SPI2CLKB: SPI2 Clock(B);<br>IIC_SCL_A: IIC SCL(A);  |
| 25 | PA11  | I/O | 24 | GPIO                                | TMR1: Timer1 Clock Input;<br>ALNK_DAT0A: Audio Link Data0(A);<br>SPI2DIB: SPI2 Data In(B);<br>SEG11: LCD SEG Output11;<br>Touch7: Touch Input Channel 7;  |
| 26 | PA10  | I/O | 24 | GPIO                                | SD0DAT1A: SPI0 Data1(A);<br>BT_FREQ:  |

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

|    |     |     |    |      |   |
|----|-----|-----|----|------|---|
|    |     |     |    |      | UART2RXB: Uart2 Data In(B);<br>ADC5: ADC Input Channel 5;<br>ALNK_LRCKA: Audio Link Word Select(A);<br>SEG10: LCD SEG Output10;   |
| 27 | PA9 | I/O | 24 | GPIO | SD0DAT2A: SD1 Data2(A);<br>BT_Priority:<br>UART2TXB: Uart2 Data Out(B);<br>ADC4: ADC Input Channel 4;<br>ALNK_SCLKA: Audio Link Serial Clock(A);<br>SEG9: LCD SEG Output9;  |
| 28 | PA8 | I/O | 24 | GPIO | SD0DAT3A: SD0 Data3(A);<br>Wlan_Active:<br>UART0RXD: Uart0 Data In(B);<br>ALNK_DAT3A: Audio Link Data3(A);<br>SEG8: LCD SEG Output8;<br>Touch15: Touch Input Channel 15;  |
| 29 | PA7 | I/O | 24 | GPIO | SD0CLKA: SD0 Clock(A);<br>BT_Active:<br>UART0TXD: Uart0 Data Out(D);<br>TMR0: Timer0 Clock Input;<br>ALNK_MCLKA: ALNK Master Clock(A);<br>SEG7: LCD SEG Output7;<br>Touch14: Touch Input Channel 14;              |
| 30 | PA6 | I/O | 24 | GPIO | SD0CMA: SD0 Command(A);<br>UART0RXA: Uart0 Data In(A);<br>UART1_RTS: Uart1 Request to send;<br>ADC3: ADC Input Channel 3;<br>IIC_SDA_D: IIC SDA(D);<br>SEG6: LCD SEG Output6;<br>Touch13: Touch Input Channel 13; |
| 31 | PA5 | I/O | 24 | GPIO | SD0DAT0A: SD0 Data0(A);<br>UART0TXA: Uart0 Data Out(A);<br>UART1_CTS: Uart1 Clear to send;<br>ADC2: ADC Input Channel 2;<br>IIC_SCL_D: IIC SCL(D);<br>SEG5: LCD SEG Output5;<br>Touch12: Touch Input Channel 12;  |
| 32 | PA4 | I/O | 24 | GPIO | PWM1: Timer1 PWM Output;<br>AMUX1R: Simulator Channel1 Right;<br>ADC1: ADC Input Channel 1;   |

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

|    |        |     |    |                   |  |
|----|--------|-----|----|-------------------|--|
|    |        |     |    |                   | UART2RXA: Uart2 Data In(A);<br>SEG4: LCD SEG Output4;<br>Touch11: Touch Input Channel 11;  |
| 33 | PA3    | I/O | 24 | GPIO              | AMUX1L: Simulator Channel1 Left;<br>ADC0: ADC Input Channel 0;<br>UART2TXA: Uart2 Data Out(A);<br>SEG3: LCD SEG Output3;<br>Touch10: Touch Input Channel 10;   |
| 34 | PA2    | I/O | 24 | GPIO              | PLNK_DAT1: PLNK Data1;<br>CLKOUT1:<br>CAP3: Timer3 Capture;<br>UART1RXC: Uart1 Data In(C);<br>SEG2: LCD SEG Output2;<br>Touch9: Touch Input Channel 9;   |
| 35 | PA1    | I/O | 24 | GPIO              | PLNK_SCLK: PLNK Serial Clock;<br>PWM0: Timer0 PWM Output;<br>UART1TXC: Uart1 Data Out(C);<br>SEG1: LCD SEG Output1;<br>Touch8: Touch Input Channel 8;  |
| 36 | DACR   | O   | /  | DAC Right Channel |  |
| 37 | DACL   | O   | /  | DAC Left Channel  |  |
| 38 | DACVDD | P   | /  | DAC Power         |  |
| 39 | VCOM   | P   | /  | DAC Reference     |  |
| 40 | DACVSS | P   | /  | Ground            |  |
| 41 | PA0    | I/O | 24 | GPIO              | PLNK_DAT0: PLNK Data0;<br>MIC: MIC Input Channel;<br>UART0RXB: Uart0 Data In(B);<br>SEG0: LCD SEG Output0;   |
| 42 | VDDIO  | P   | /  | IO Power 3.3v     |  |
| 43 | PB5    | I/O | 8  | GPIO              | UART0TXB: Uart0 Data Out(B);<br>AMUX0R: Simulator Channel0 Right;<br>SPI1DOA: SPI1 Data Out(A);<br>SD1DAT3B: SD1 Data3(A);<br>ALNK_DAT3B: Audio Link Data3(B);<br>SD0CLKB: SD0 Clock(B);<br>ADC9: ADC Input Channel 9;<br>Touch5: Touch Input Channel 5; |
| 44 | PB4    | I/O | 8  | GPIO              | PWM3: Timer3 PWM Output;<br>AMUX0L: Simulator Channel0 Left;<br>SPI1CLKA: SPI1 Clock(A);   |

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.



|    |     |     |   |      |  |
|----|-----|-----|---|------|--|
|    |     |     |   |      | SD1DAT2B: SD1 Data2(B);<br>ALNK_DAT2B: Audio Link Data2(B);<br>SD0CMDB: SD0 Command(B);<br>ADC8: ADC Input Channel 8;<br>SPI0_DAT2AB(2): SPI0 Data2(AB);<br>Touch4: Touch Input Channel 4;   |
| 45 | PB3 | I/O | 8 | GPIO | PWM2: Timer2 PWM Output;<br>UART2RXC: Uart2 Data In(C);<br>SPI1DIA: SPI1 Data In(A);<br>SD1DAT1B: SD1 Data1(B);<br>ALNK_DAT1B: Audio Link Data1(B);<br>SD0DAT0B: SD0 Data0(B);<br>AMUX2R: Simulator Channel2 Right;<br>SPI0_DAT3AB(3): SPI0 Data3(AB);<br>Touch3: Touch Input Channel 3; |
| 46 | PB6 | I/O | 8 | GPIO | ALNK_MCLKB: Audio Link Master Clock(B);<br>AMUX2L: Simulator Channel2 Left;<br>SPI0_DIB(1): SPI0 Data In(B);<br>Touch6: Touch Input Channel 6;   |
| 47 | PB2 | I/O | 8 | GPIO | UART2TXC: Uart2 Data Out(C);<br>SPI2DIA: SPI2 Data In(A);<br>SD1CLKB: SD1 Clock(B);<br>ALNK_DAT0B: Audio Link Data0(B);<br>SD0DAT1B: SD0 Data1(B);<br>SPI0_CLKB: SPI0 Clock(B);<br>Touch2: Touch Input Channel 2;  |
| 48 | PB1 | I/O | 8 | GPIO | TMR2: Timer2 Clock Input;<br>UART1RXA: Uart1 Data In(A);<br>SPI2DOA: SPI2 Data Out(A);<br>SD1CMDB: SD1 Command(B);<br>ALNK_LRCKB: Audio Link Word Select(B);<br>SD0DAT2B: SD0 Data2(B);<br>ADC7: ADC Input Channel 7;<br>Touch1: Touch Input Channel 1;                                  |

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 2、Electrical Characteristics

### 2.1 PMU Characteristics

Table 2-1

| Symbol              | Parameter       | Min | Typ | Max | Unit | Test Conditions           |
|---------------------|-----------------|-----|-----|-----|------|---------------------------|
| V <sub>BAT</sub>    | Voltage Input   | 2.2 | 3.7 | 5.5 | V    |                           |
| V <sub>3.3</sub>    | Voltage output  | –   | 3.3 | –   | V    | LDO5V = 5V, 100mA loading |
| V <sub>1.2</sub>    |                 | –   | 1.2 | –   | V    | LDO5V = 5V, 50mA loading  |
| V <sub>13</sub>     | Voltage output  |     | 1.3 |     | V    | LDO5V=5V, 100mA loading   |
| V <sub>DACVDD</sub> | DAC Voltage     | –   | 3.1 | –   | V    | LDO5V = 5V, 10mA loading  |
| I <sub>L3.3</sub>   | Loading current | –   | –   | 150 | mA   | LDO5V = 5V                |

### 2.2 IO Input/Output Electrical Logical Characteristics

Table 2-2

| IO input characteristics  |                           |            |     |            |      |                 |
|---------------------------|---------------------------|------------|-----|------------|------|-----------------|
| Symbol                    | Parameter                 | Min        | Typ | Max        | Unit | Test Conditions |
| V <sub>IL</sub>           | Low-Level Input Voltage   | -0.3       | –   | 0.3* VDDIO | V    | VDDIO = 3.3V    |
| V <sub>IH</sub>           | High-Level Input Voltage  | 0.7* VDDIO | –   | VDDIO+0.3  | V    | VDDIO = 3.3V    |
| IO output characteristics |                           |            |     |            |      |                 |
| V <sub>OL</sub>           | Low-Level Output Voltage  | –          | –   | 0.33       | V    | VDDIO = 3.3V    |
| V <sub>OH</sub>           | High-Level Output Voltage | 2.7        | –   | –          | V    | VDDIO = 3.3V    |

### 2.3 Internal Resistor Characteristics

Table 2-3

| Port                | General Output | High Drive | Internal Pull-Up Resistor | Internal Pull-Down Resistor | Comment  |
|---------------------|----------------|------------|---------------------------|-----------------------------|--|
| PA0~PA12<br>PC0~PC5 | 8mA            | 24mA       | 10K                       | 10K                         | 1、PR0 default input disable<br>2、PR1 default output 0<br>3、PR2 & PR3 default pull up<br>4、USBDM & USBDP default pull down<br>5、internal pull-up/pull-down resistance   accuracy ±20% |
| PB0~PB6             | 4mA            | 8mA        | 10K                       | 10K                         |  |
| PR0~PR3             | 8mA            | 10mA       | 10K                       | 10K                         |  |
| USBDM<br>USBDP      | 4mA            | –          | 1.5K                      | 15K                         |  |

#### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 2.4 DAC Characteristics

Table 2-4

| Parameter          | Min | Typ | Max | Unit | Test Conditions  |
|--------------------|-----|-----|-----|------|--|
| Frequency Response | 20  | –   | 20K | Hz   | 1KHz/0dB<br>10Kohm loading<br>With A-Weighted Filter   |
| THD+N              | –   | -69 | –   | dB   |  |
| S/N                | –   | 95  | –   | dB   |  |
| Crosstalk          | –   | -80 | –   | dB   |  |
| Output Swing       |     | 1   |     | Vrms |  |
| Dynamic Range      |     | 90  |     | dB   | 1KHz/-60dB<br>10Kohm loading<br>With A-Weighted Filter |
| DAC Output Power   | 11  |     | –   | mW   | 32ohm loading  |

## 2.5 ADC Characteristics

Table 2-5

| Parameter     | Min | Typ | Max | Unit | Test Conditions  |
|---------------|-----|-----|-----|------|--|
| Dynamic Range |     | 85  |     | dB   | 1KHz/-60dB<br>10Kohm loading<br>With A-Weighted Filter |
| S/N           | –   | 90  | –   | dB   | 1KHz/-60dB   |
| THD+N         | –   | -72 | –   | dB   | 10Kohm loading   |
| Crosstalk     | –   | -80 | –   | dB   | With A-Weighted Filter                                 |

## 2.6 BT Characteristics

### 2.6.1 Transmitter

#### Basic Data Rate

Table 2-6

| Parameter              | Min   | Typ | Max | Unit | Test Conditions                                |
|------------------------|-------|-----|-----|------|--|
| RF Transmit Power      |       | 0   | 4   | dBm  | 25°C,<br>Power Supply<br>Voltage=5V<br>2441MHz |
| RF Power Control Range |       | 20  |     | dB   |  |
| 20dB Bandwidth         |       | 950 |     | KHz  |  |
| Adjacent Channel       | +2MHz | -40 |     | dBm  |  |
|                        | -2MHz | -38 |     | dBm  |  |
| Transmit Power         | +3MHz | -44 |     | dBm  |  |
|                        | -3MHz | -35 |     | dBm  |  |

**Enhanced Data Rate** **Table 2-7**

| Parameter                            |           | Min | Typ | Max | Unit | Test Conditions       |
|--------------------------------------|-----------|-----|-----|-----|------|-----------------------|
| Relative Power                       |           |     | 1.2 |     | dB   | 25°C,<br>Power Supply |
| $\pi/4$ DQPSK<br>Modulation Accuracy | DEVM RMS  |     | 6   |     | %    |                       |
|                                      | DEVM 99%  |     | 10  |     | %    |                       |
|                                      | DEVM Peak |     | 15  |     | %    |                       |
| Adjacent Channel                     | +2MHz     |     | -40 |     | dBm  | Voltage=5V<br>2441MHz |
|                                      | -2MHz     |     | -38 |     | dBm  |                       |
| Transmit Power                       | +3MHz     |     | -44 |     | dBm  |                       |
|                                      | -3MHz     |     | -35 |     | dBm  |                       |

## 2.6.2 Receiver

**Basic Data Rate** **Table 2-8**

| Parameter                                  |       | Min | Typ | Max | Unit | Test Conditions       |
|--|-------|-----|-----|-----|------|-----------------------|
| Sensitivity                                |       |     | -89 |     | dBm  | 25°C,<br>Power Supply |
| Co-channel Interference Rejection          |       |     | -13 |     | dB   |                       |
| Adjacent Channel<br>Interference Rejection | +1MHz |     | +5  |     | dB   |                       |
|  | -1MHz |     | +2  |     | dB   |                       |
|  | +2MHz |     | +37 |     | dB   |                       |
| Interference Rejection                     | -2MHz |     | +36 |     | dB   | Voltage=5V<br>2441MHz |
|  | +3MHz |     | +40 |     | dB   |                       |
|  | -3MHz |     | +35 |     | dB   |                       |

**Enhanced Data Rate** **Table 2-9**

| Parameter                                  |       | Min | Typ | Max | Unit | Test Conditions       |
|--|-------|-----|-----|-----|------|-----------------------|
| Sensitivity                                |       |     | -89 |     | dBm  | 25°C,<br>Power Supply |
| Co-channel Interference Rejection          |       |     | -13 |     | dB   |                       |
| Adjacent Channel<br>Interference Rejection | +1MHz |     | +5  |     | dB   |                       |
|  | -1MHz |     | +2  |     | dB   |                       |
|  | +2MHz |     | +37 |     | dB   |                       |
| Interference Rejection                     | -2MHz |     | +36 |     | dB   | Voltage=5V<br>2441MHz |
|  | +3MHz |     | +40 |     | dB   |                       |
|  | -3MHz |     | +35 |     | dB   |                       |

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 2.7 FM Receiver Characteristics

Table 2-10

| Parameter                             | Min | Typ | Max | Unit              | Test Conditions                             |
|---------------------------------------|-----|-----|-----|-------------------|---|
| Input Frequency                       | 76  |     | 108 | MHz               |   |
| Usable Sensitivity                    | 3   | 4   | 8   | dB $\mu$ V<br>EMF | (S+N)/N=26dB                                |
| Adjacent Channel Selectivity          |     | 48  |     | dB                | $\pm$ 200kHz                                |
| IIP3                                  |     | 88  |     | dB $\mu$ V<br>EMF | $\Delta$ f1=200 kHz,<br>$\Delta$ f2=400 kHz |
| Audio Output Voltage                  | 0   |     | 3   | V                 | Empty Load                                  |
| Audio Frequency Response              | 20  |     | 20k | Hz                | DacTest                                     |
| Audio (S+N)/N                         |     | 52  |     | dB                |   |
| Stereo Separation                     |     | 40  |     | dB                |   |
| Audio Total Harmonic Distortion (THD) |     | 0.4 |     | %                 |   |

### 3、 Package Information

#### 3.1 LQFP48(7mm\*7mm)

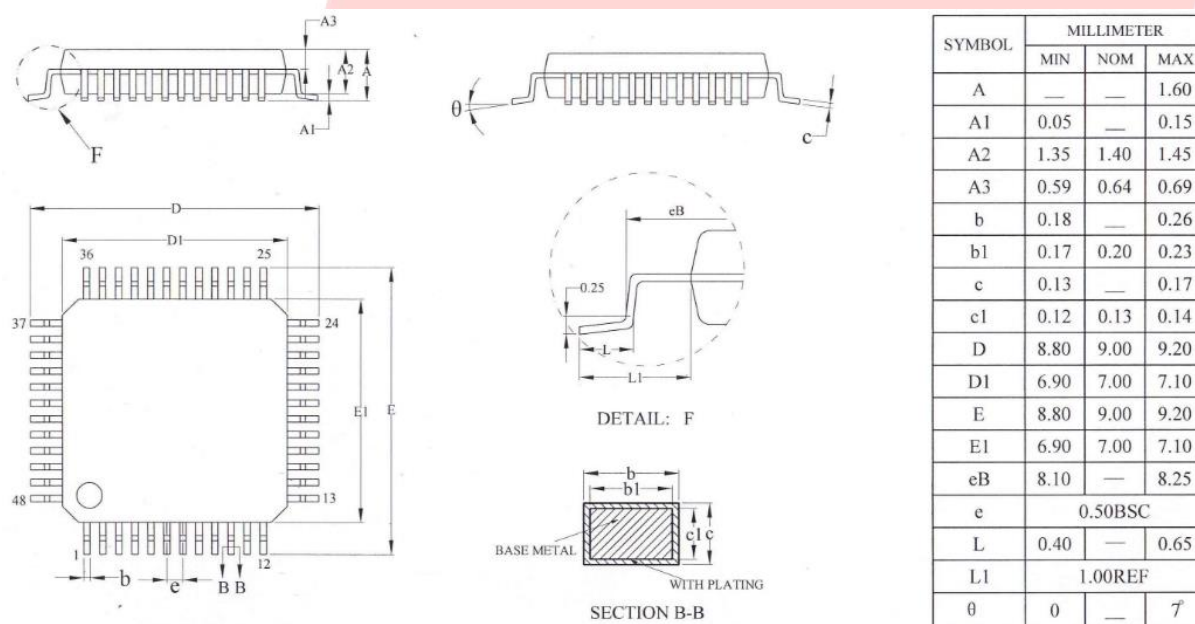


Figure 3-1. AC6921A\_LQFP48 Package

## 4、 Revision History

| Date       | Revision | Description     |
|------------|----------|-----------------|
| 2018.04.20 | V1.0     | Initial Release |
|            |          |                 |



ZHUHAI