XC6604 Series

ETR03071-002

0.5V Low Input, 1A High Speed LDO Regulator with Adjustable Current Limit

■GENERAL DESCRIPTION

The XC6604 series is a low voltage input (0.5V) operation and provides high accuracy ±15mV / ±20mV and can supply large current efficiently due to its ultra low on-resistance even at low output voltages.

The series is ideally suited to the applications which require high current in low input/output voltages and consists of a N-ch driver transistor, a voltage reference, an error amplifier, a current limiter, a fold-back circuit, a thermal shutdown (TSD) circuit, an under voltage lock out (UVLO) circuit, a soft-start circuit and a phase compensation circuit.
Output voltage is selectable in 0.1V increments within a range of 0.5V to 1.8V using laser trimming technology and ceramic capacitors can be used for the output stabilization capacitor (C_L). When the output current reaches the current limit, the output voltage drops as well as the output current is decreased as a function of the foldback circuit. The current limit can be adjustable with connecting a resistor to the I_{LIM} pin.

The CE function enables the output to be turned off and the series to be put in stand-by mode resulting in greatly reduced power consumption. At the time of entering the stand-by mode, the series enables the electric charge at the output capacitor (C_L) to be discharged via the internal switch. As a result the V_{OUT} pin quickly returns to the V_{SS} level.

The CE pull-down function keeps the IC to be in stand-by mode even if the CE pin is left open.

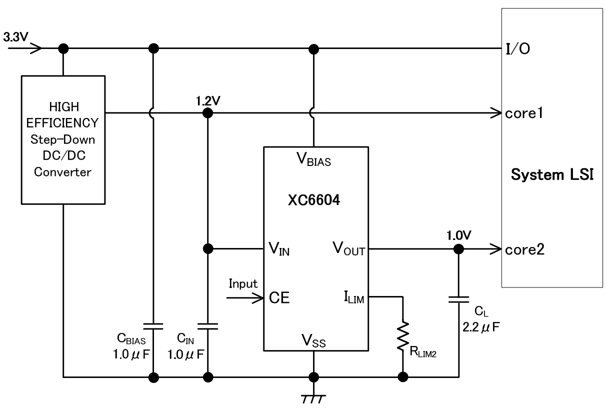
■APPLICATIONS

- Smart phones / Mobile phones
- Digital still cameras / Camcorders
- Note PCs / Tablet PCs
- E-book Readers / Electronic dictionaries
- Wireless LAN

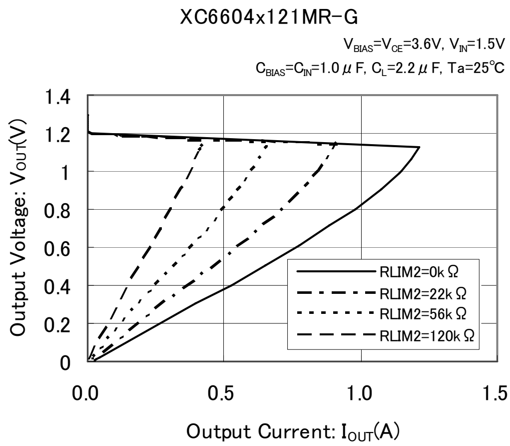
■FEATURES

Maximum Output Current	:	1A (1.3A Limit)
ON Resistance	:	0.15Ω@V_{BIAS}=3.6V, V_{OUT}=1.2V
Bias Voltage Range	:	2.5V～6.0V
Input Voltage Range	:	0.5V～3.0V
Output Voltage Range	:	0.5V～1.8V (0.1V increments)
Output Voltage Accuracy	:	±0.015V@V_{OUT}<1.2V ±0.020V@V_{OUT}≧1.2V
Ripple Rejection	:	60dB@f=1kHz (V_{BIAS_PSRR}) 75dB@f=1kHz (V_{IN_PSRR})
Low Power Consumption	:	100 μA (V_{BIAS}), 6.5 μA (V_{IN})@V_{OUT}=1.2V
Stand-by Current	:	0.01 μA (V_{BIAS}), 0.01 μA (V_{IN})
Under-voltage Lockout	:	1.8V (V_{BIAS}), 0.4V (V_{IN})
Thermal Shutdown	:	150℃@detect, 125℃@release
Protection Circuit	:	Foldback Current Limit, TSD, UVLO
Function	:	Soft-start CE Pull-Down (Active High) C_L High Speed Discharge
Operating Ambient Temperature	:	-40℃～+85℃
Output Capacitor	:	Ceramic Capacitor Compatible (2.2 μF)
Packages	:	USP-6C, SOT-26W
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

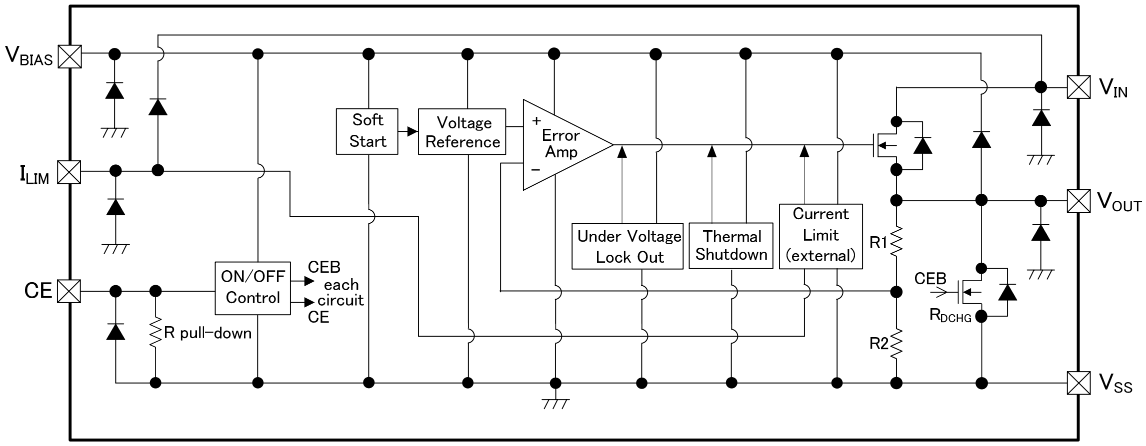


■TYPICAL PERFORMANCE CHARACTERISTICS

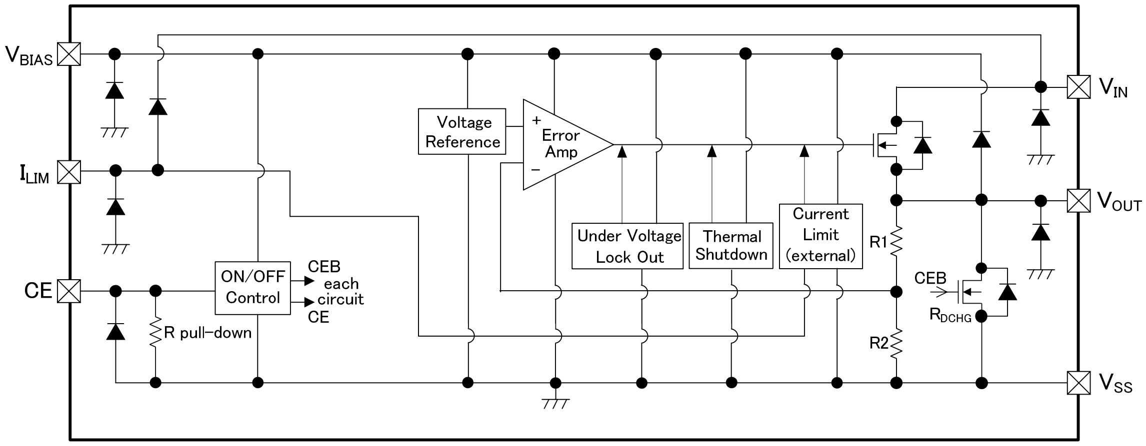


■BLOCK DIAGRAMS

Type A



Type B



■PRODUCT CLASSIFICATION

●Ordering Information

XC6604①②③④⑤⑥-⑦

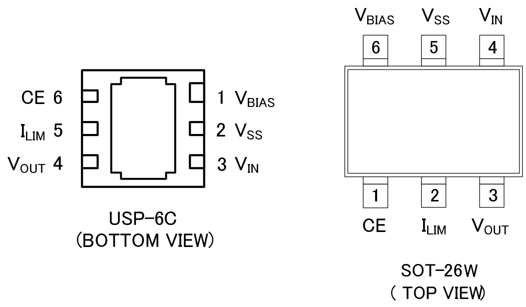
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	Refer to Selection Guide
		B	
②③	Output Voltage	05～18	e.g. 1.2V → ②=1, ③=2
④	Output Voltage Accuracy	1	±0.015V (V_{OUT}<1.2V), ±0.020V (V_{OUT}≧1.2V)
⑤⑥-⑦ (*1)	Packages (Order Unit)	ER-G	USP-6C (3,000/Reel)
		MR-G	SOT-26W (3,000/Reel)

(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection Guide

TYPE	SOFT-START	CURRENT LIMITTER	THERMAL SHUTDOWN	UVLO	CE PULL-DOWN RESISTOR	C_L AUTO DISCHARGE
A	Yes	Adjustable	Yes	Yes	Yes	Yes
B	No	Adjustable	Yes	Yes	Yes	Yes

■PIN CONFIGURATION



*The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the V_{SS} (No. 2) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
USP-6C	SOT-26W		
1	6	V_{BIAS}	Power Supply Input
2	5	V_{SS}	Ground
3	4	V_{IN}	Driver Transistor Input
4	3	V_{OUT}	Output
5	2	I_{LIM}	Current Limit Resistance Connection
6	1	CE	ON/OFF Control

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
CE	L	Stand-by
	H	Active
	OPEN	Stand-by

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Bias Voltage		V_{BIAS}	-0.3～+6.5	V
Input Voltage		V_{IN}	-0.3～+6.5	V
Output Current		I_{OUT}	1.65 (*1)	A
Output Voltage (*2)		V_{OUT}	-0.3～V_{BIAS}+0.3 or +6.5	V
			-0.3～V_{IN}+0.3 or +6.5	
CE Input Voltage		V_{CE}	-0.3～+6.5	V
I_{LIM} Pin Voltage (*3)		I_{LIM}	-0.3～V_{IN}+0.3 or +6.5	V
Power Dissipation	USP-6C	Pd	120	mW
			1000 (PCB mounted) (*4)	
	SOT-26W		250	
			600 (PCB mounted) (*4)	
Operating Ambient Temperature		Topr	-40～+85	℃
Storage Temperature		Tstg	-55～+125	℃

* All voltages are described based on the V_{SS} pin.
(*1) I_{OUT}≦Pd/(V_{IN}-V_{OUT})
(*2) The maximum value should be either V_{BIAS}+0.3, V_{IN}+0.3 or +6.5 in the lowest.
(*3) The maximum value should be either V_{IN}+0.3 or +6.5 in the lowest.
(*4) The power dissipation measured with the test board condition is listed as reference data.
Please refer to page 26～27 for details.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Bias Voltage	V_{BIAS}			2.5	-	6.0	V	①
Input Voltage	V_{IN}			0.5	-	3.0	V	①
Output Voltage	$V_{OUT(E)}$ (*1)	I_{OUT}=100mA	$V_{OUT(T)}<1.2V$	-0.015	$V_{OUT(T)}$ (*2)	+0.015	V	①
			$V_{OUT(T)}\geqq 1.2V$	-0.020		+0.020		
Maximum Output Current (*3)	I_{OUTMAX}	$V_{OUT(T)}<1.2V$, $V_{BIAS}=V_{CE}=2.5V$		1.0	-	-	A	①
		$V_{OUT(T)}\geqq 1.2V$, $V_{BIAS}=V_{CE}=V_{OUT(T)}+1.3V$						
Load Regulation	ΔV_{OUT}	$1mA\leqq I_{OUT}\leqq 1A$		-	37	68	mV	①
Dropout Voltage	Vdif (*4)	I_{OUT}=1A		-	E-1 (*5)		mV	①
Supply Current 1 (*6)	I_{BIAS}	I_{OUT}=0A		76	100	143	μA	②
Supply Current 2	I_{IN}	I_{OUT}=0A	$V_{OUT(T)}<1.2V$	0.1	-	8.7	μA	②
			$V_{OUT(T)}\geqq 1.2V$	3.9	-	14.2		
Stand-by Current 1	I_{BIAS_STB}	V_{BIAS}=6.0V, V_{IN}=3.0V, $V_{CE}=V_{SS}$		-	0.01	0.10	μA	②
Stand-by Current 2	I_{IN_STB}	V_{BIAS}=6.0V, V_{IN}=3.0V, $V_{CE}=V_{SS}$		-	0.01	0.15	μA	②
Bias Line Regulation	$\Delta V_{OUT}/(\Delta V_{BIAS}\cdot V_{OUT})$	$V_{OUT(T)}<1.2V$, $V_{CE}=V_{BIAS}$, $2.5V\leqq V_{BIAS}\leqq 6.0V$		-	0.01	0.10	%/V	①
		$V_{OUT(T)}\geqq 1.2V$, $V_{CE}=V_{BIAS}$, $V_{OUT(T)}+1.3V\leqq V_{BIAS}\leqq 6.0V$						
Input Line Regulation	$\Delta V_{OUT}/(\Delta V_{IN}\cdot V_{OUT})$	$V_{OUT(T)}+0.1V\leqq V_{IN}\leqq 3.0V$		-	0.01	0.10	%/V	①
Bias UVLO Voltage	V_{BIAS_UVLOD}			V_{SS}	-	1.28	V	①
Bias UVLO Release Voltage	V_{BIAS_UVLOR}			2.5	-	6.0	V	①
Input UVLO Voltage	V_{IN_UVLOD}			V_{SS}	-	0.23	V	①
Input UVLO Release Voltage	V_{IN_UVLOR}			0.5	-	3.0	V	①
Output Voltage Temperature Characteristics	$\Delta V_{OUT}/(\Delta Topr\cdot V_{OUT})$	I_{OUT}=100mA -40℃≦Topr≦85℃		-	±30	-	ppm/℃	①
Bias Ripple Rejection Ratio	V_{BIAS_PSRR}	$V_{BIAS}=V_{CE}=3.6V_{DC}+0.2V_{p-pAC}$ I_{OUT}=100mA, f=1kHz, C_{BIAS}=OPEN		-	60	-	dB	③
Input Ripple Rejection Ratio	V_{IN_PSRR}	$V_{IN}=V_{OUT(T)}+0.3V_{DC}+0.2V_{p-pAC}$ I_{OUT}=100mA, f=1kHz, C_{IN}=OPEN		-	75	-	dB	③
Current Limit (*3)	I_{LIM}	V_{OUT}={V_{OUT}@I_{OUT}=1A}×0.95		1.0	1.3	-	A	①
Adjustable Current Limit Accuracy (*8)	I_{LIM_ADJ}	-		(-35)	-	(35)	%	①
Short - Circuit Current	I_{SHORT}	$V_{OUT}=V_{SS}$		-	90	-	mA	①
Thermal Shutdown Detect Temperature	T_{TSD}	Junction Temperature		-	150	-	℃	①
Thermal Shutdown Release Temperature	T_{TSR}	Junction Temperature		-	125	-	℃	①
Thermal Shutdown Hysteresis Width	$T_{TSD}-T_{TSR}$	Junction Temperature		-	25	-	℃	①
C_L Auto-Discharge Resistance	R_{DCHG}	$V_{CE}=V_{SS}$, $V_{OUT}=V_{OUT(T)}$		130	190	255	Ω	①
CE "H" Level Voltage	V_{CEH}			0.65	-	6.00	V	④
CE "L" Level Voltage	V_{CEL}			V_{SS}	-	0.41	V	④
CE "H" Level Current	I_{CEH}	$V_{BIAS}=V_{CE}$=6.0V		3.2	6.0	10.6	μA	④
CE "L" Level Current	I_{CEL}	V_{BIAS}=6.0V, $V_{CE}=V_{SS}$		-0.1	-	0.1	μA	④
Soft-Start Time (*7) (Type A)	t_{SS}	V_{CE}=0V→3.6V, tr=5μs		225	430	600	μs	⑤
Output Rise Time (*7) (Type B)	t_{ON}	V_{CE}=0V→3.6V, tr=5μs		-	-	110	μs	⑤
Inrush Current (Type A)	I_{RUSH}	C_L=2.2μF	$V_{OUT(T)}\leqq 1.2V$	-	-	70	mA	⑤
			$V_{OUT(T)}>1.2V$	-	-	85		
		C_L=10μF	$V_{OUT(T)}\leqq 1.2V$	-	-	155		
			$V_{OUT(T)}>1.2V$	-	-	215		

NOTE:
Unless otherwise stated, $V_{BIAS}=V_{CE}$=3.6V, $V_{IN}=V_{OUT(T)}$+0.3V, I_{OUT}=1mA , $C_{BIAS}=C_{IN}$=1.0μF, C_L=2.2μF, I_{LIM} Pin=V_{SS}

(*1) $V_{OUT(E)}$ = Effective output voltage

(*2) $V_{OUT(T)}$ = Nominal output voltage

(*3) Mount conditions affect heat dissipation. Maximum output current is not guaranteed when TSD starts to operate earlier.

(*4) Vdif＝{$V_{IN1}-V_{OUT1}$}

V_{IN1} is an input voltage when V_{OUT1} appears at the output during decreasing input voltage gradually.

V_{OUT1} is a voltage equal to 98% of the output voltage where $V_{BIAS}=V_{CE}$=3.6 and $V_{IN}=V_{OUT(T)}$+0.3V at I_{OUT}=1A is input to the V_{IN} pin.

(*5) Please refer to the table E-1 named DROPOUT VOLTAGE CHART

(*6) Supply current 1 (I_{BIAS}) may be fluctuated because that some bias current flows into the output.

(*7) A time between the CE input goes over the CE H threshold and the output reaches $V_{OUT(E)}$x0.9V.

(*8) Design value

■ELECTRICAL CHARACTERISTICS (Continued)

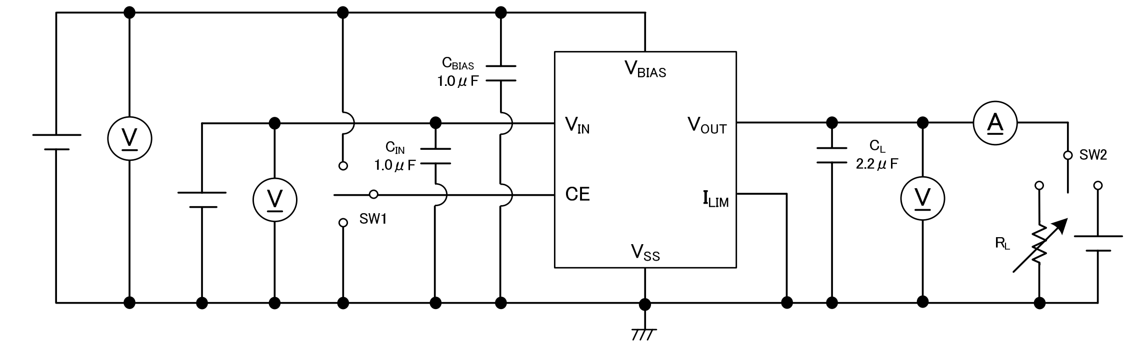
●Dropout Voltage Chart

<table>
<tr><th rowspan="4">NOMINAL OUTPUT VOLTAGE</th><th colspan="15">E-1</th></tr>
<tr><th colspan="15">DROPOUT VOLTAGE (mV)</th></tr>
<tr><th colspan="3">V_{BIAS}=3.0V</th><th colspan="3">V_{BIAS}=3.3V</th><th colspan="3">V_{BIAS}=3.6V</th><th colspan="3">V_{BIAS}=4.2V</th><th colspan="3">V_{BIAS}=5.0V</th></tr>
<tr><th rowspan="2">V_{GS} (V)</th><th colspan="2">Vdif(mV)</th><th rowspan="2">V_{GS} (V)</th><th colspan="2">Vdif(mV)</th><th rowspan="2">V_{GS} (V)</th><th colspan="2">Vdif(mV)</th><th rowspan="2">V_{GS} (V)</th><th colspan="2">Vdif(mV)</th><th rowspan="2">V_{GS} (V)</th><th colspan="2">Vdif(mV)</th></tr>
<tr><th>$V_{OUT(T)}$</th><th>TYP.</th><th>MAX.</th><th>TYP.</th><th>MAX.</th><th>TYP.</th><th>MAX.</th><th>TYP.</th><th>MAX.</th><th>TYP.</th><th>MAX.</th></tr>
<tr><td>0.5</td><td>2.5</td><td>152</td><td>218</td><td>2.8</td><td rowspan="3">146</td><td rowspan="3">213</td><td>3.1</td><td rowspan="6">146</td><td rowspan="6">213</td><td>3.7</td><td rowspan="5">140</td><td rowspan="5">208</td><td>4.5</td><td rowspan="7">137</td><td rowspan="7">206</td></tr>
<tr><td>0.6</td><td>2.4</td><td rowspan="2">155</td><td rowspan="2">223</td><td>2.7</td><td>3.0</td><td>3.6</td><td>4.4</td></tr>
<tr><td>0.7</td><td>2.3</td><td>2.6</td><td>2.9</td><td>3.5</td><td>4.3</td></tr>
<tr><td>0.8</td><td>2.2</td><td>158</td><td>228</td><td>2.5</td><td>152</td><td>218</td><td>2.8</td><td>3.4</td><td>4.2</td></tr>
<tr><td>0.9</td><td>2.1</td><td>162</td><td>233</td><td>2.4</td><td rowspan="2">155</td><td rowspan="2">223</td><td>2.7</td><td>3.3</td><td>4.1</td></tr>
<tr><td>1.0</td><td>2.0</td><td>165</td><td>238</td><td>2.3</td><td>2.6</td><td>3.2</td><td rowspan="7">146</td><td rowspan="7">213</td><td>4.0</td></tr>
<tr><td>1.1</td><td>1.9</td><td>167</td><td>243</td><td>2.2</td><td>158</td><td>228</td><td>2.5</td><td>152</td><td>218</td><td>3.1</td><td>3.9</td></tr>
<tr><td>1.2</td><td>1.8</td><td>169</td><td>253</td><td>2.1</td><td>162</td><td>233</td><td>2.4</td><td rowspan="2">155</td><td rowspan="2">223</td><td>3.0</td><td>3.8</td><td rowspan="6">140</td><td rowspan="6">208</td></tr>
<tr><td>1.3</td><td>1.7</td><td>179</td><td>268</td><td>2.0</td><td>165</td><td>238</td><td>2.3</td><td>2.9</td><td>3.7</td></tr>
<tr><td>1.4</td><td>1.6</td><td>189</td><td>283</td><td>1.9</td><td>167</td><td>243</td><td>2.2</td><td>158</td><td>228</td><td>2.8</td><td>3.6</td></tr>
<tr><td>1.5</td><td>1.5</td><td>202</td><td>303</td><td>1.8</td><td>169</td><td>253</td><td>2.1</td><td>162</td><td>233</td><td>2.7</td><td>3.5</td></tr>
<tr><td>1.6</td><td>1.4</td><td>213</td><td>328</td><td>1.7</td><td>179</td><td>268</td><td>2.0</td><td>165</td><td>238</td><td>2.6</td><td>3.4</td></tr>
<tr><td>1.7</td><td>1.3</td><td>225</td><td>373</td><td>1.6</td><td>189</td><td>283</td><td>1.9</td><td>167</td><td>243</td><td>2.5</td><td>152</td><td>218</td><td>3.3</td></tr>
<tr><td>1.8</td><td>1.2</td><td>255</td><td>423</td><td>1.5</td><td>202</td><td>303</td><td>1.8</td><td>169</td><td>253</td><td>2.4</td><td>155</td><td>223</td><td>3.2</td><td>146</td><td>213</td></tr>
</table>

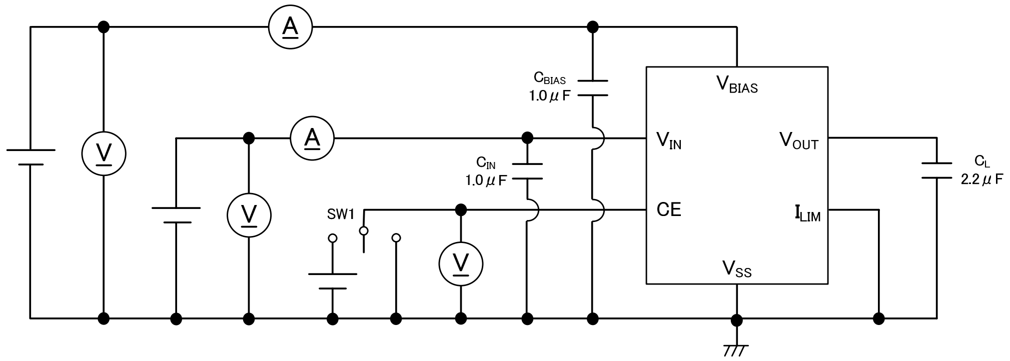
* Dropout voltage is defined as the V_{GS}(=V_{BIAS}–$V_{OUT(E)}$) of the driver transistor.

■TEST CIRCUITS

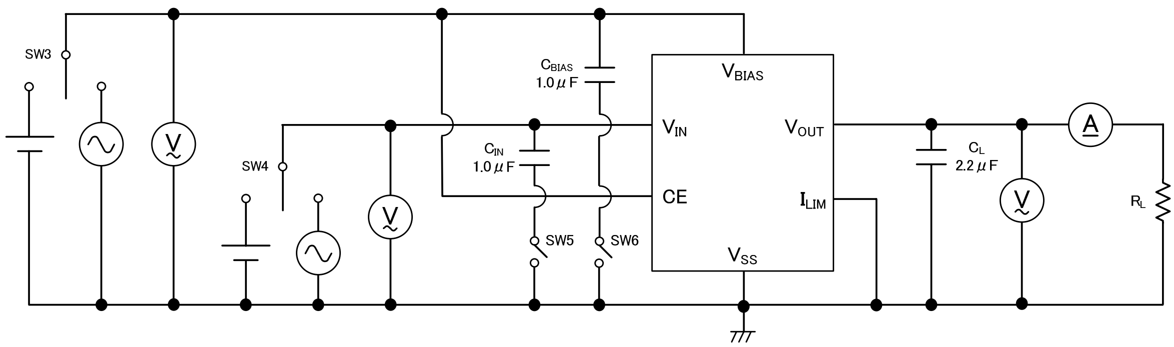
CIRCUIT①



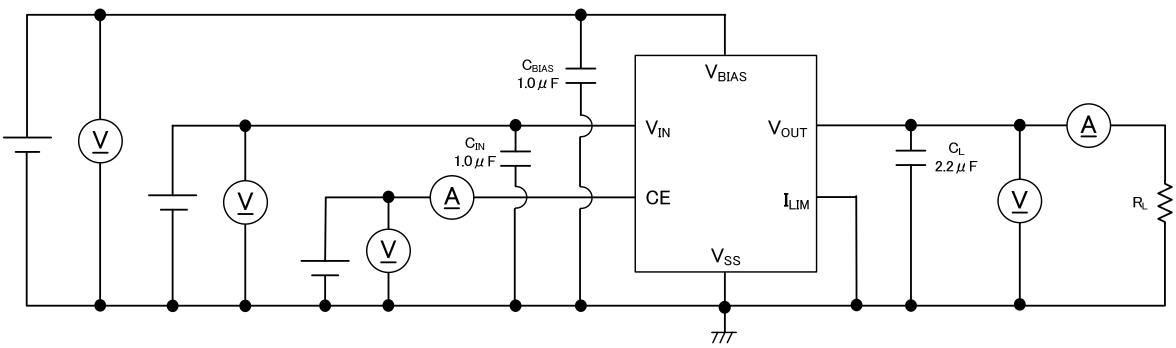
CIRCUIT②



CIRCUIT③

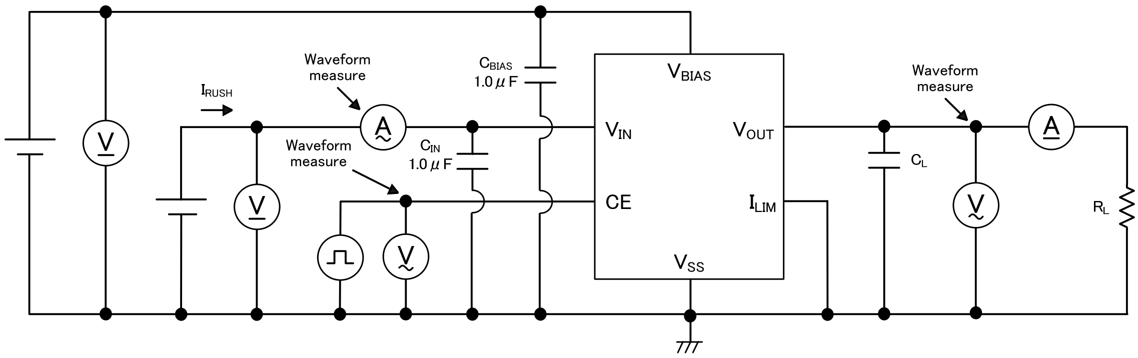


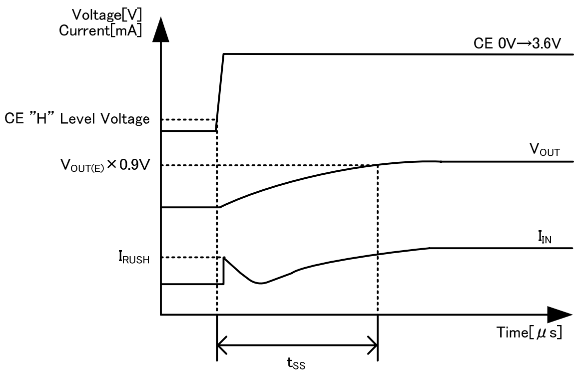
CIRCUIT④



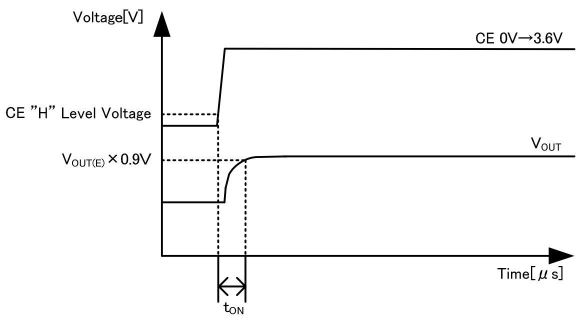
■TEST CIRCUITS (Continued)

CIRCUIT⑤





XC6604 Series, Type A



XC6604 Series, Type B

■OPERATIONAL DESCRIPTION

The voltage divided by resistors R1 and R2 is compared with the internal reference voltage by the error amplifier. The V_{OUT} pin is then driven by the subsequent output signal. The output voltage at the V_{OUT} pin is controlled and stabilized by a system of negative feedback.

V_{BIAS} pin is power supply pin for output voltage control circuit, protection circuit and CE circuit. Also, the V_{BIAS} pin supplies some current as output current. V_{IN} pin is connected to a driver transistor and provides output current.

In order to obtain high efficient output current through low on-resistance, please take enough V_{GS} (=V_{BIAS} – $V_{OUT(E)}$) of the driver transistor.

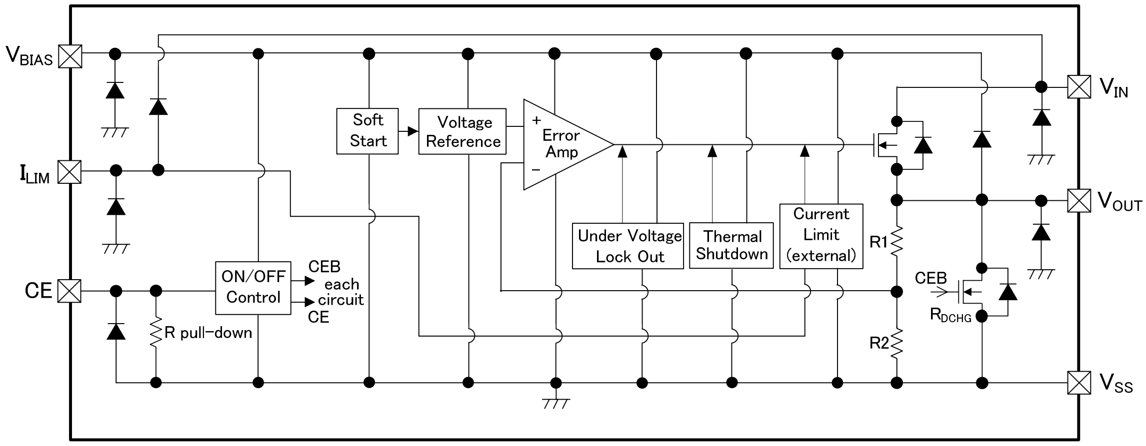


Figure1: XC6604 Series, Type A

<Current Limiter, Short-Circuit Protection>

The XC6604 series includes a combination of a fixed current limiter circuit and a foldback short-circuit protection. When the output current reaches the current limit, the output voltage drops and this operation makes the output current foldback to be decreased.

The current limit can be set freely with connecting a resistor to the I_{LIM} pin.

Please note about the foldback circuit characteristics below;

- Output voltage may not rise when the output voltage is lower than 0V at the IC operation start.
- Current over the foldback current limit will not flow at the IC operation start.
- Please use type A (with soft-start time) to prevent from inrush current, because the circuit may not response to a drastic current change such as the inrush current.

When the I_{LIM} pin is left open, driver transistor will be forced off.

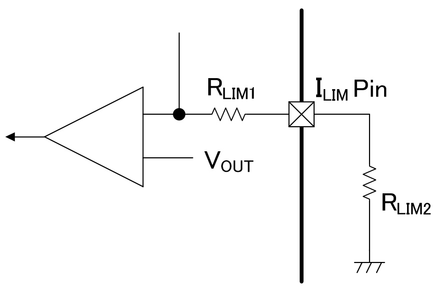
Current Limit is calculated by the following formulas.

$$I_{LIM} = V_{OUT(T)} / (R_{LIM1} + R_{LIM2}) \times 79645.7 \ [A]$$
$$R_{LIM1} = V_{OUT(T)} / (16.3 \times 10^{-6}) \quad [\Omega]$$

I_{LIM}: Current Limit
$V_{OUT(T)}$: Nominal Output Voltage
R_{LIM1}: Internal Current Limit Resistance
R_{LIM2}: External Current Limit Resistance

Figure 2: XC6604 Series, Range of adjustable current limit

OUTPUT VOLTAGE RANGE	ADJUSTABLE CURRENT LIMIT
$V_{OUT(T)}$	I_{LIM}
0.5V～1.8V	0.5A～1.3A



XC6604 Series, R_{LIM2} Connecting

■OPERATIONAL DESCRIPTION (Continued)

<Soft-Start Function>
With the XC6604 (Type A), the inrush current (I_{RUSH}) from V_{IN} to V_{OUT} for charging C_L at start-up can be reduced and makes the V_{IN} stable. As for the XC6604, the soft-start time in the type A is optimized internally. On the other hand, the type B of the XC6604 does not have the soft-start time function.

<Thermal Shutdown Circuit (TSD) >
When the junction temperature of the built-in driver transistor reaches the temperature limit, the thermal shutdown circuit operates and the driver transistor will be set to OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature.

<Under Voltage Lock Out (UVLO) >
When the V_{BIAS} pin and V_{IN} pin voltage drops, the output driver transistor is set to OFF by UVLO function to prevent false output caused by unstable operation of the internal circuitry. When the V_{BIAS} pin voltage and the V_{IN} pin voltage rises at release voltage, the UVLO function is released. The driver transistor is turned ON and start to operate voltage regulation.

<CE Pin>
The XC6604 internal circuitry can be shutdown via the signal to the CE pin. In shutdown mode with CE low level voltage, the V_{OUT} pin will be pulled down to the V_{SS} level via C_L discharge resistance (R_{DCHG}) placed in parallel to R1 and R2.
The CE pin has pull-down circuitry so that CE input current flows during IC operation. If the CE pin voltage is taken from V_{BIAS} pin or V_{SS} pin then logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry when medium voltage is input.

<C_L High Speed Auto-Discharge>
XC6604 series can quickly discharge the electric charge at the output capacitor (C_L) via the internal transistor located between the V_{OUT} pin and the V_{SS} pin when a low signal to the CE pin which enables a whole IC circuit put into OFF state. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it could avoids malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R_{DCHG}) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value (R_{DCHG}) and an output capacitor value (C_L) as τ ($\tau = C_L \times R_{DCHG}$), the output voltage after discharge via the internal transistor is calculated by the following formula. Please also note R_{DCHG} is depended on V_{BIAS}. When V_{BIAS} is larger, R_{DCHG} is smaller.

$$V = V_{OUT(E)} \times e^{-t/\tau} \quad or \quad t = \tau \ln (V_{OUT(E)} / V)$$

V: Output voltage during discharge
$V_{OUT(E)}$: Initial Output voltage
t: Discharge time
τ : $C_L \times R_{DCHG}$

<Low ESR Capacitor>
With the XC6604 series, a stable output voltage is achievable even if used with low ESR capacitors, as a phase compensation circuit is built-in. The output capacitor (C_L) should be connected as close to V_{OUT} pin and V_{SS} pin to obtain stable phase compensation. Values required for the phase compensation are as the table below.
For a stable power input, please connect a bias capacitor (C_{BIAS}) between the V_{BIAS} pin and the V_{SS} pin. Also, please connect an input capacitor (C_{IN}) between the V_{IN} pin and the V_{SS} pin. In order to ensure the stable phase compensation while avoiding run-out of values, please use the capacitor (C_{BIAS}, C_{IN} and C_L) which does not depend on bias or temperature too much. The table below (Figure 3) shows recommended values of C_{BIAS}, C_{IN} and C_L.

Figure 3: Recommended Values of C_{BIAS}, C_{IN} and C_L (MIN.)

OUTPUT VOLTAGE RANGE	BIAS CAPACITOR	INPUT CAPACITOR	OUTPUT CAPACITOR
$V_{OUT(T)}$	C_{BIAS}	C_{IN}	C_L
0.5V～1.8V	1.0μF	1.0μF	2.2μF

■NOTES ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low for the V_{BIAS}, V_{IN} and V_{SS} wiring in particular.

3. Please wire the C_{BIAS}, C_{IN} and C_L as close to the IC as possible.

4. Capacitances of these capacitors (C_{BIAS}, $C_{IN,}$ C_L) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.

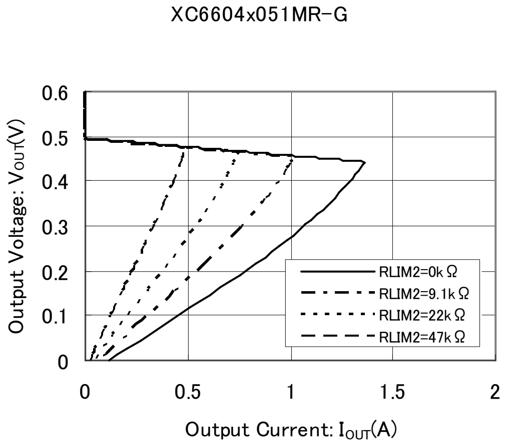
5. When it is used in a quite small input / output dropout voltage, output may go into unstable operation. Please test it thoroughly before using it in production.

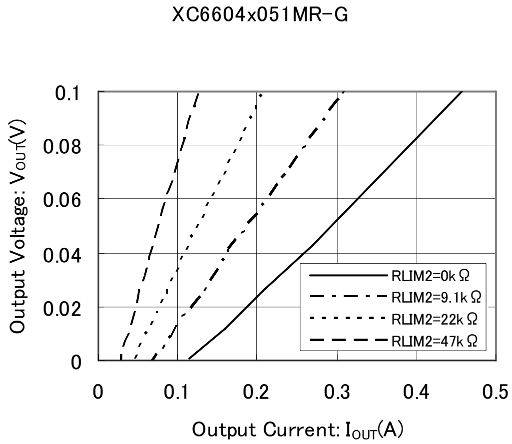
6. Torex places an importance on improving our products and their reliability.
   We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

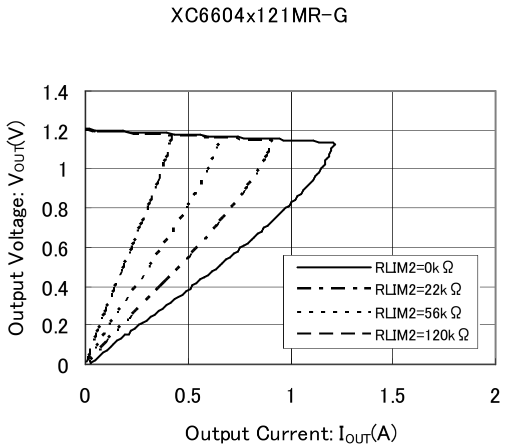
■TYPICAL PERFORMANCE CHARACTERISTICS

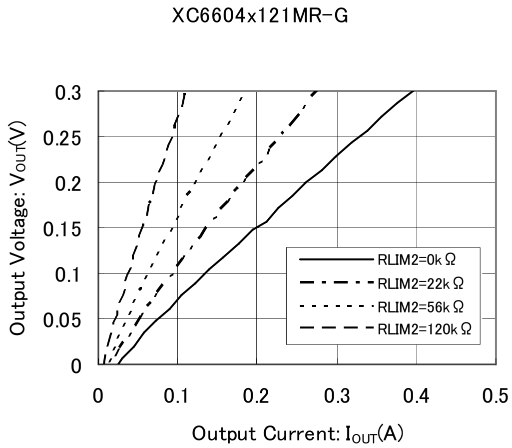
* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin= V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

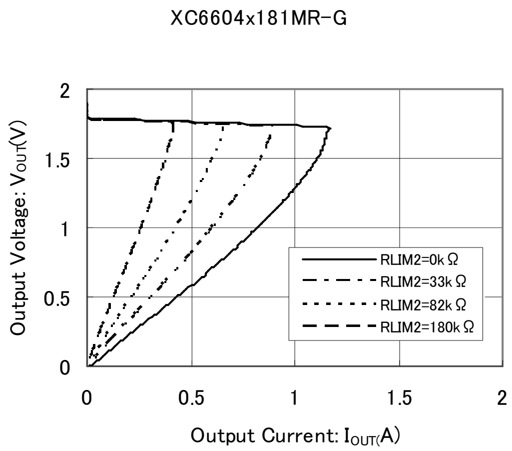
(1) Output Voltage vs. Output Current

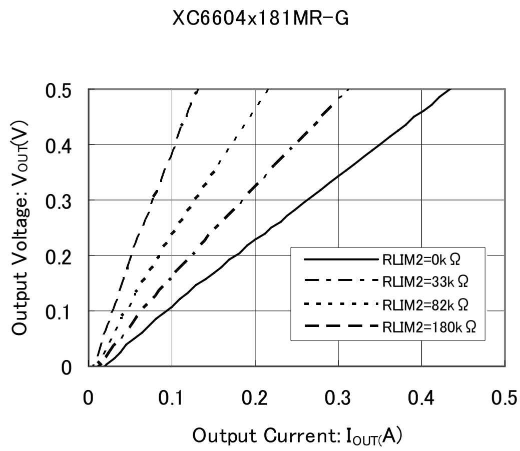












* Mount conditions affect heat dissipation. Thermal shutdown may start to operate before reaching the current limit.

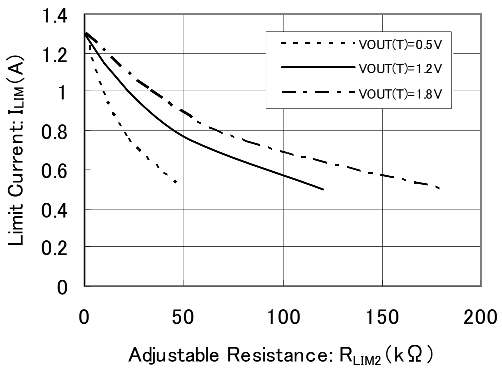
* If start-up current is required over the current limit, IC operation will not start. Please use the current within the range of use.

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin= V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

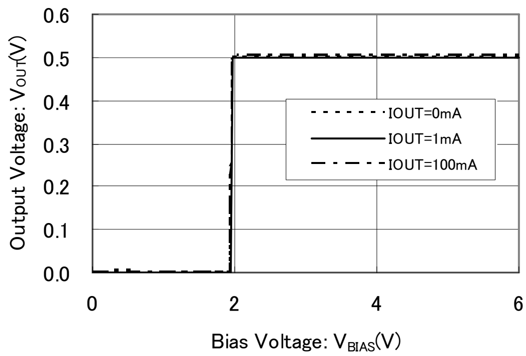
(2) Limit Current vs. Adjustable Resistance

XC6604xxx1xR-G

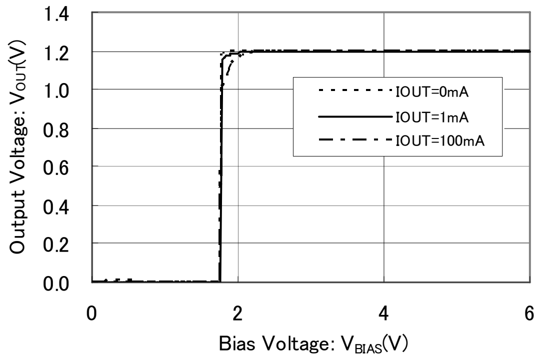


(3) Output Voltage vs. Bias Voltage

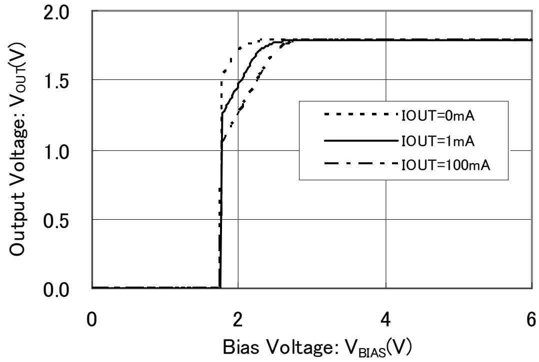
XC6604x051xR-G



XC6604x121xR-G



XC6604x181xR-G

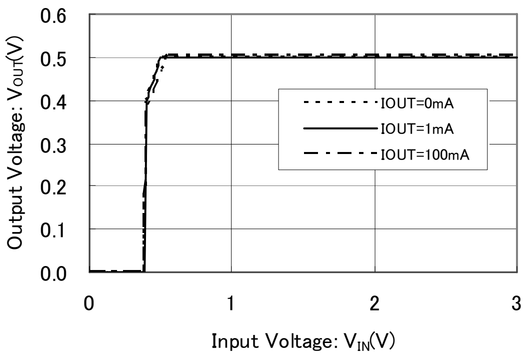


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

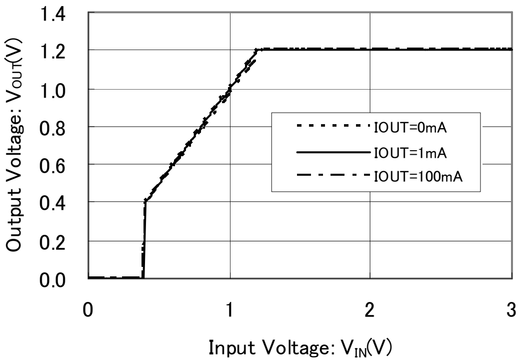
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, I_{LIM} Pin=V_{SS}, C_{BIAS}=C_{IN}=1.0 μ F, C_L=2.2 μ F, Ta=25℃

(4) Output Voltage vs. Input Voltage

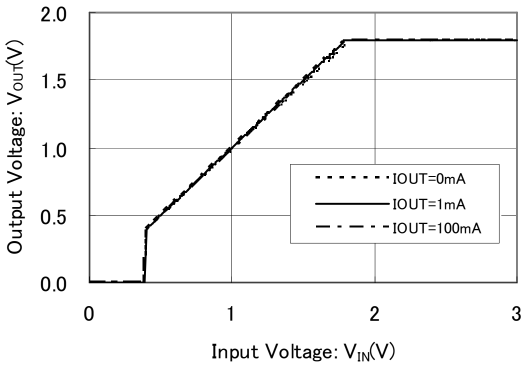
XC6604x051xR-G



XC6604x121xR-G

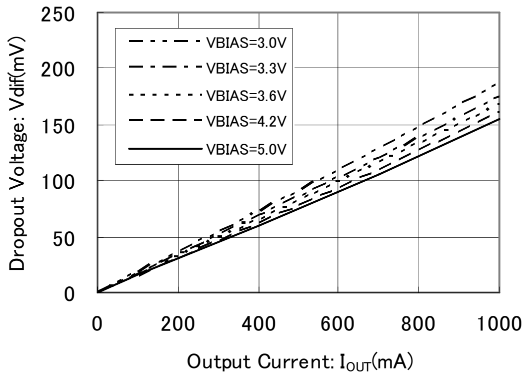


XC6604x181xR-G

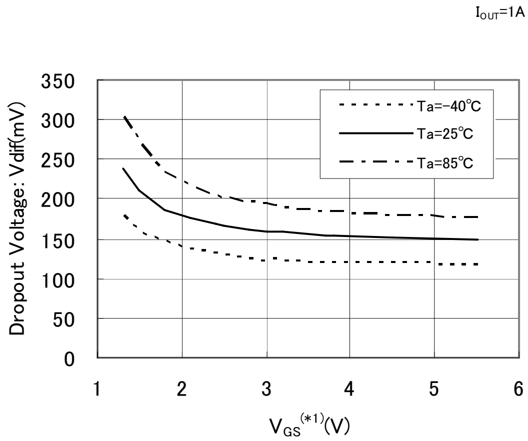


(5) Dropout Voltage vs. Output Current

XC6604x121MR-G



XC6604xxx1MR-G



(*1) V_{GS} is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{OUT(E)}$.

A value of the dropout voltage is determined by the value of the V_{GS}.

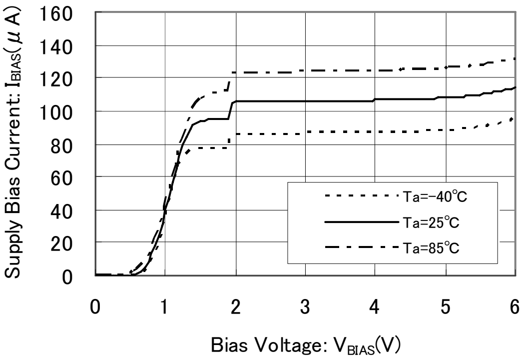
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, I_{LIM} Pin=V_{SS}, C_{BIAS}=C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(6) Supply Bias Current vs. Bias Voltage

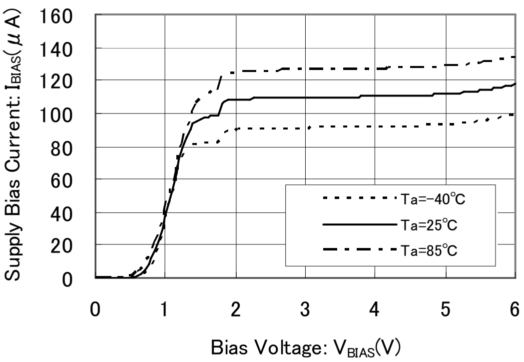
XC6604x051xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
V_{CE}=V_{BIAS}, I_{OUT}=0mA



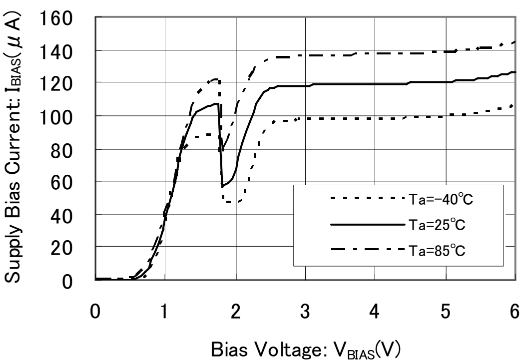
XC6604x121xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
V_{CE}=V_{BIAS}, I_{OUT}=0mA



XC6604x181xR-G

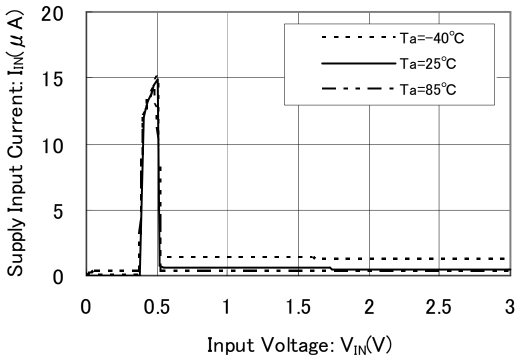
C_{IN}=C_{BIAS}=C_L=OPEN
V_{CE}=V_{BIAS}, I_{OUT}=0mA,



(7) Supply Input Current vs. Input Voltage

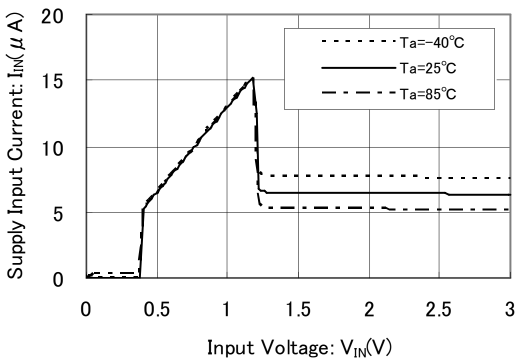
XC6604x051xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
I_{OUT}=0mA



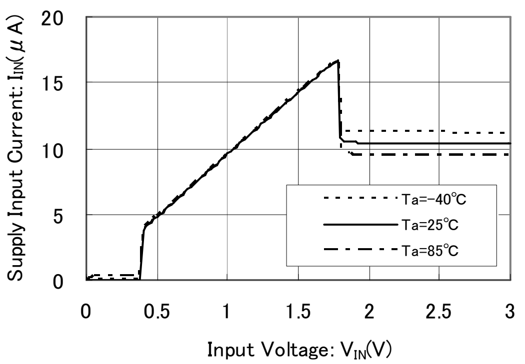
XC6604x121xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
I_{OUT}=0mA



XC6604x181xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
I_{OUT}=0mA

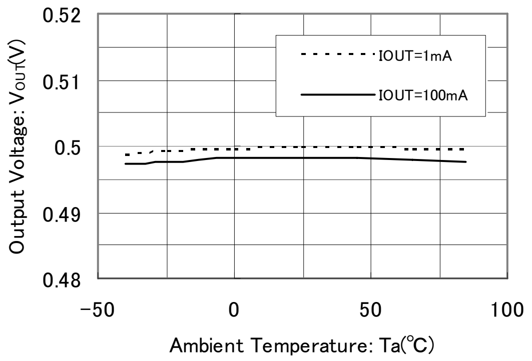


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

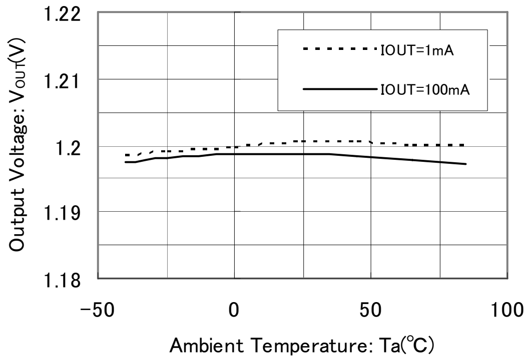
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, I_{LIM} Pin=V_{SS}, C_{BIAS}=C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(8) Output Voltage vs. Ambient Temperature

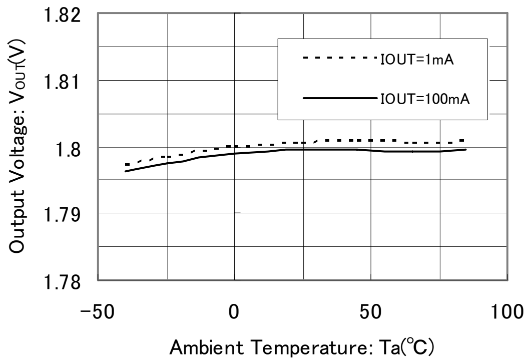
XC6604x051xR-G



XC6604x121xR-G



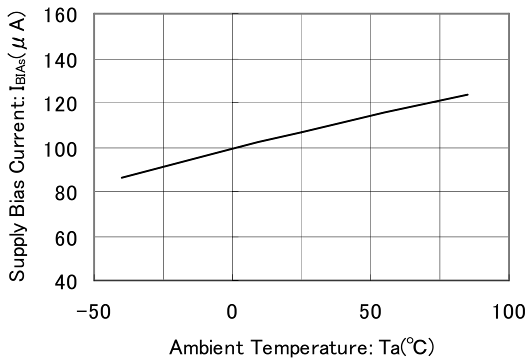
XC6604x181xR-G



(9) Supply Bias Current vs. Ambient Temperature

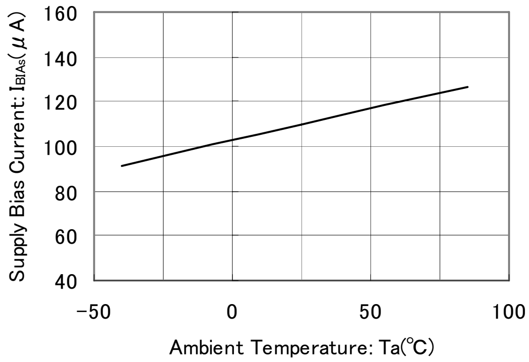
XC6604x051xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
I_{OUT}=0mA



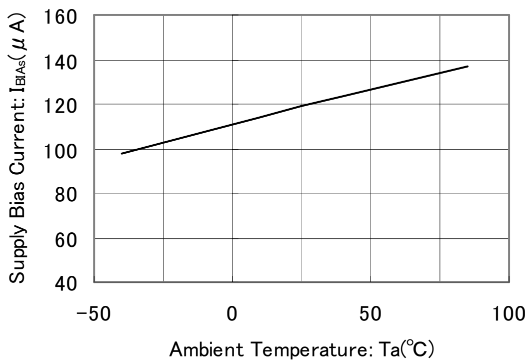
XC6604x121xR-G

C_{IN}=C_{BIAS}=C_L=OPEN
I_{OUT}=0mA



XC6604x181xR-G

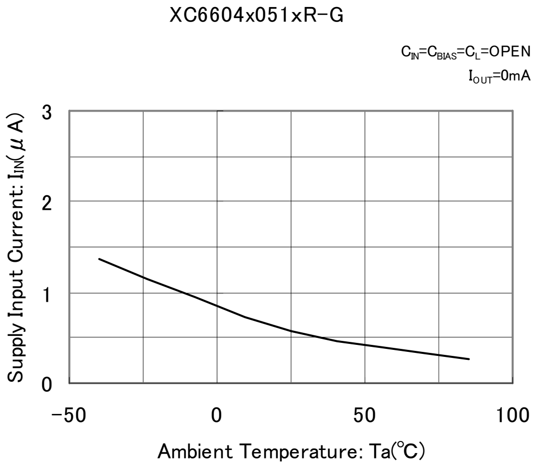
C_{IN}=C_{BIAS}= C_L=OPEN
I_{OUT}=0mA

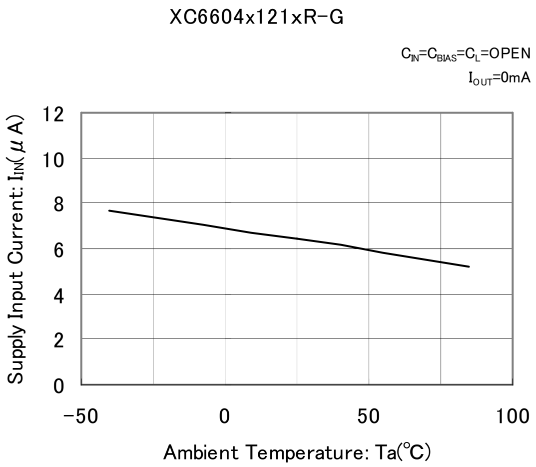


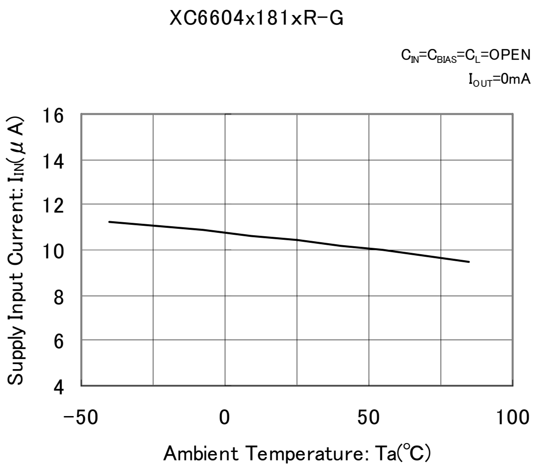
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin=V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

(10) Supply Input Current vs. Ambient Temperature







■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

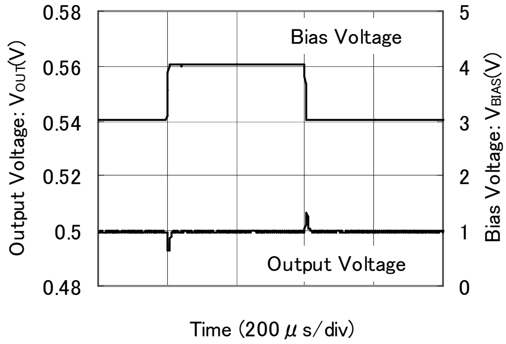
* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin=V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

(11) Bias Transient Response

XC6604x051xR-G

C_{BIAS}=OPEN

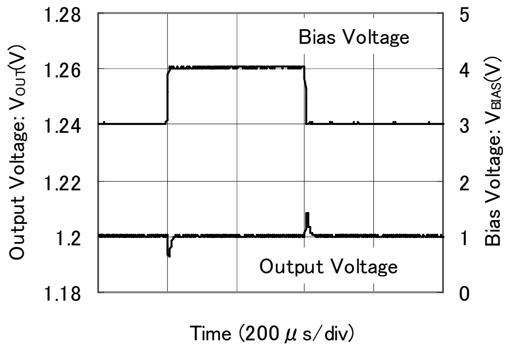
V_{BIAS}=3.0V→4.0V(tr=tf=5 μ s), I_{OUT}=100mA



XC6604x121xR-G

C_{BIAS}=OPEN

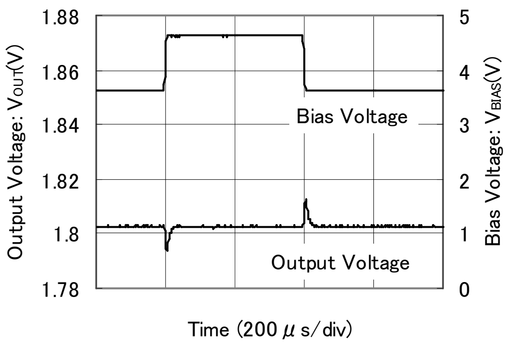
V_{BIAS}=3.0V→4.0V(tr=tf=5 μ s) I_{OUT}=100mA



XC6604x181xR-G

C_{BIAS}=OPEN

V_{BIAS}=3.6V→4.6V(tr=tf=5 μ s) I_{OUT}=100mA

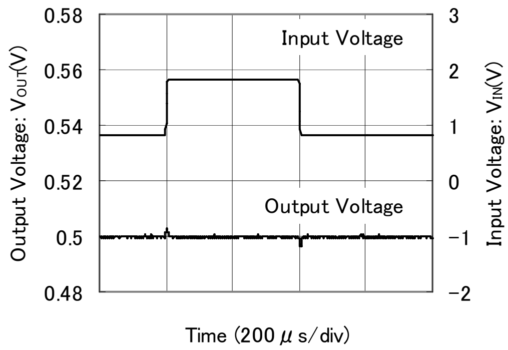


(12) Input Transient Response

XC6604x051xR-G

C_{IN}=OPEN

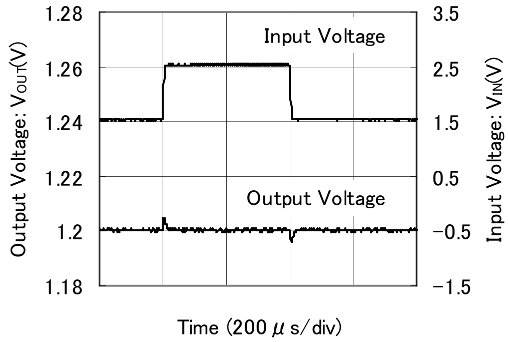
V_{IN}=0.8V→1.8V(tr=tf=5 μ s), I_{OUT}=100mA



XC6604x121xR-G

C_{IN}=OPEN

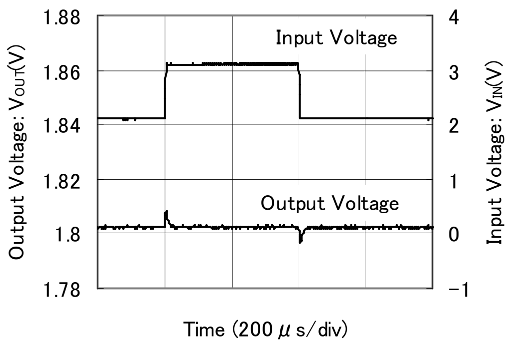
V_{IN}=1.5V→2.5V(tr=tf=5 μ s), I_{OUT}=100mA



XC6604x181xR-G

C_{IN}=OPEN

V_{IN}=2.1V→3.1V(tr=tf=5 μ s), I_{OUT}=100mA

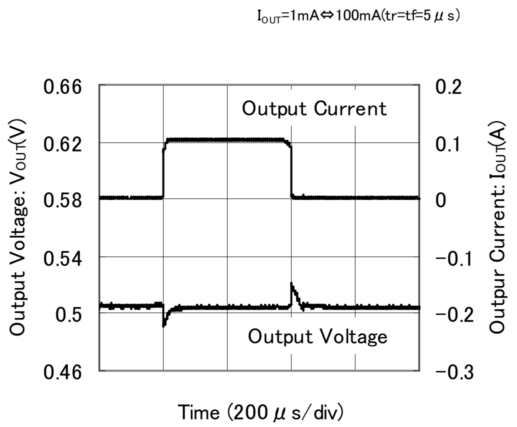


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

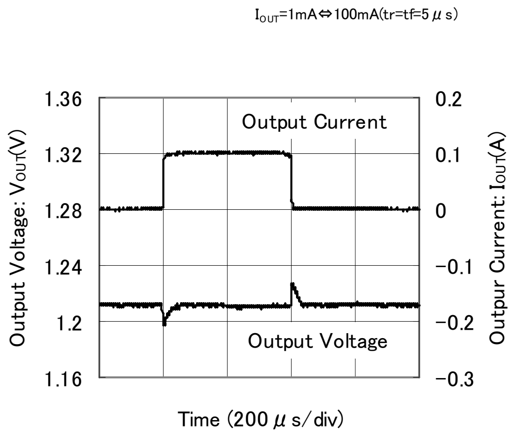
* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin=V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

(13) Load Transient Response

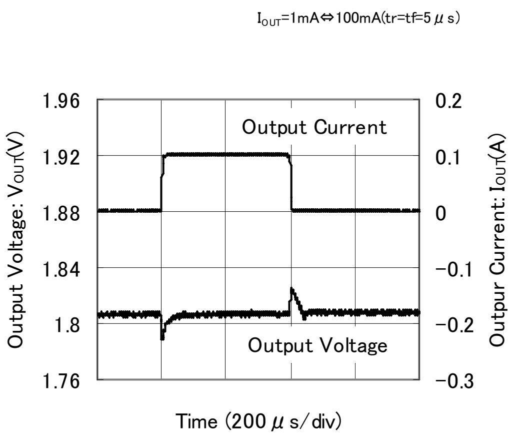
XC6604x051xR-G



XC6604x121xR-G



XC6604x181xR-G



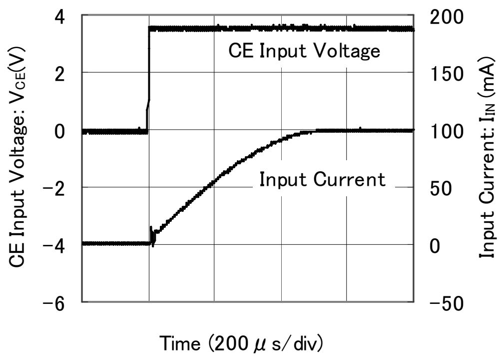
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, I_{LIM} Pin= V_{SS}, C_{BIAS}=C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(14) CE Input Response

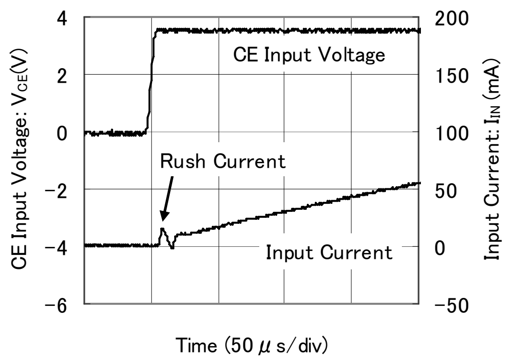
XC6604A051xR-G

V_{CE}=0V→3.6V(tr=5μs)
I_{OUT}=100mA



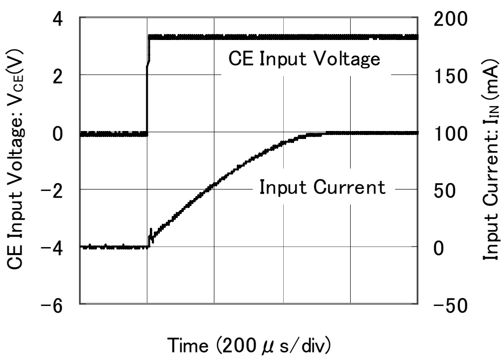
XC6604A051xR-G

V_{CE}=0V→3.6V(tr=5μs)
I_{OUT}=100mA



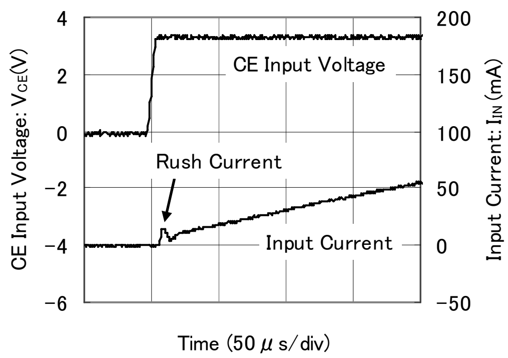
XC6604A121xR-G

V_{CE}=0V→3.6V(tr=5μs)
I_{OUT}=100mA



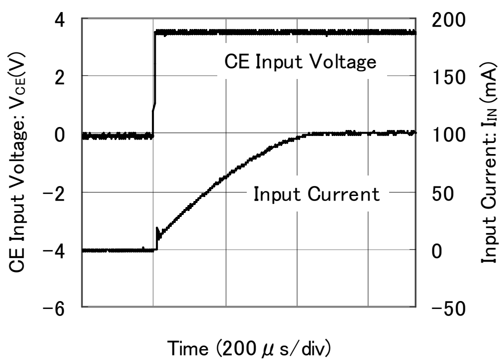
XC6604A121xR-G

V_{CE}=0V→3.6V(tr=5μs)
I_{OUT}=100mA



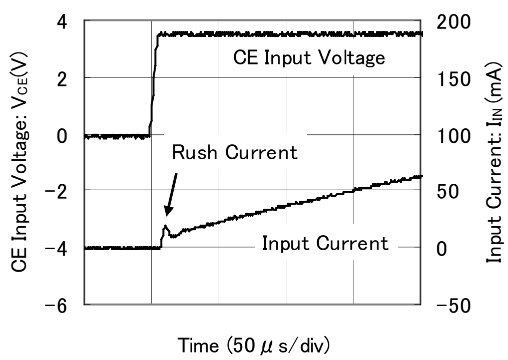
XC6604A181xR-G

V_{CE}=0V→3.6V(tr=5μs)
I_{OUT}=100mA



XC6604A181xR-G

V_{CE}=0V→3.6V(tr=5μs)
I_{OUT}=100mA

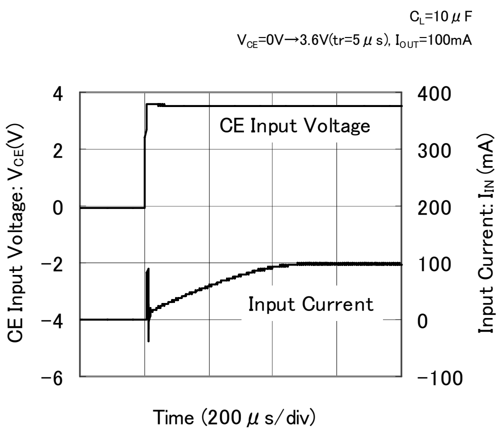


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, I_{LIM} Pin=V_{SS}, C_{BIAS}=C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(14) CE Input Response (Continued)

XC6604A051xR-G



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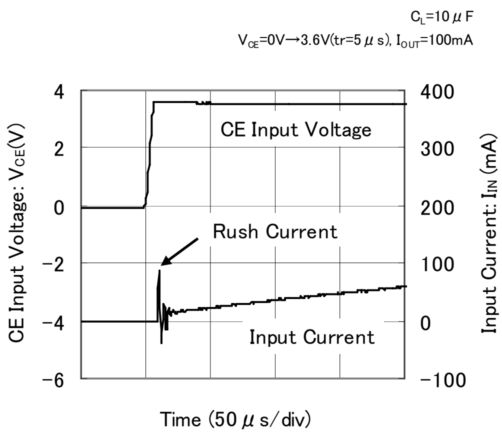

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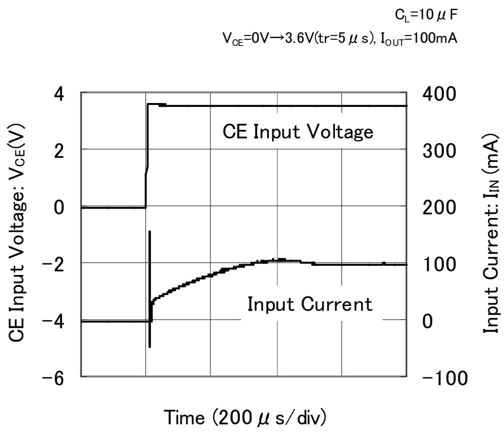

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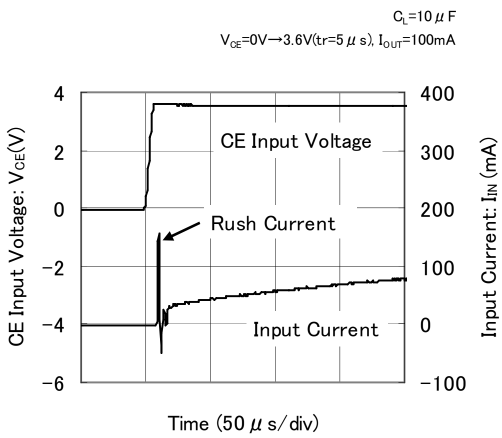

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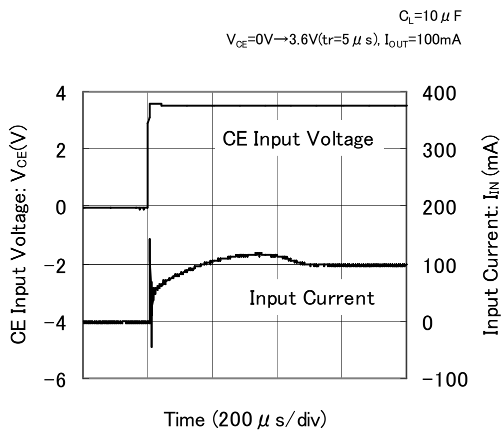

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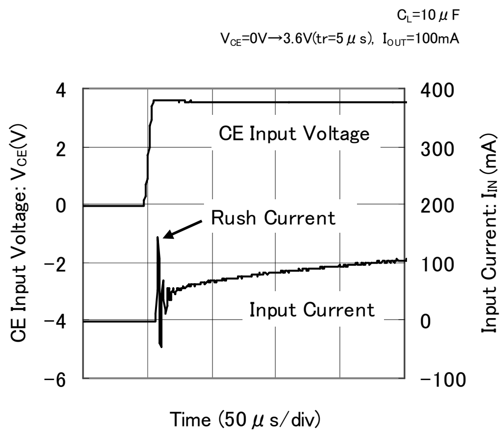
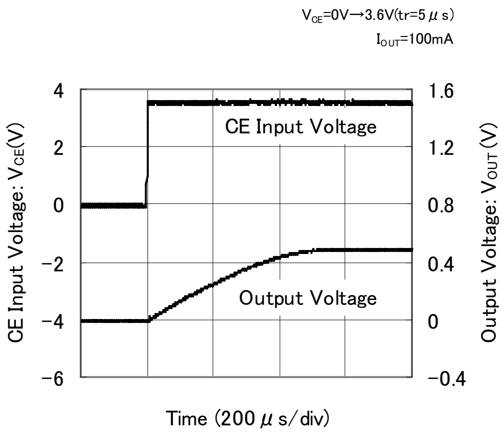


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

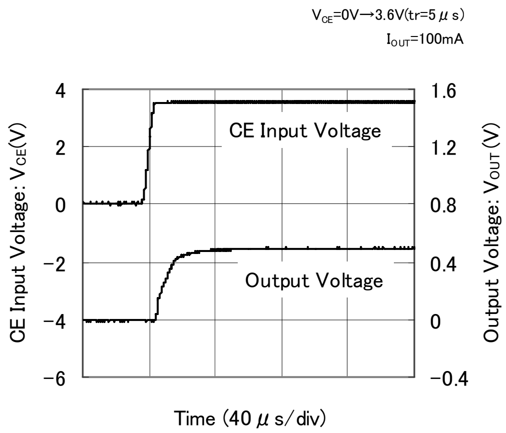
* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin=V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

(15) CE Rising Response Time

XC6604A051xR-G



XC6604B051xR-G



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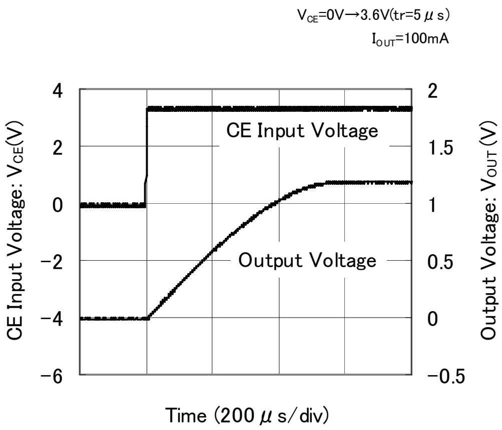
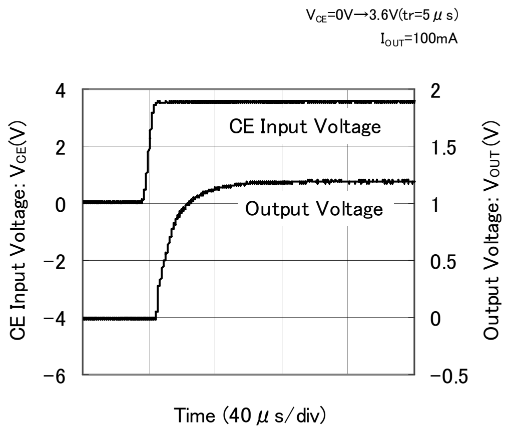
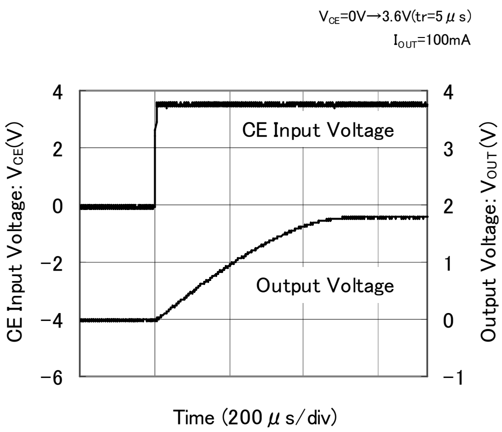


XC6604B121xR-G



XC6604A181xR-G



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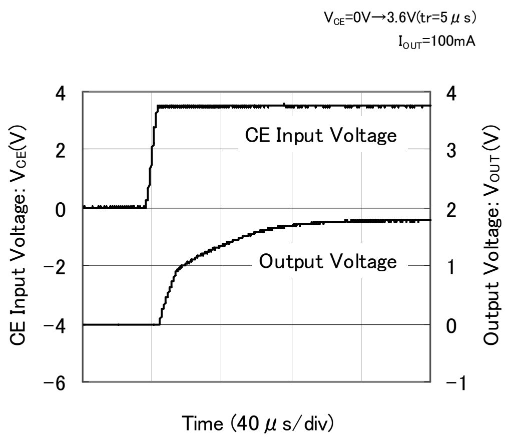
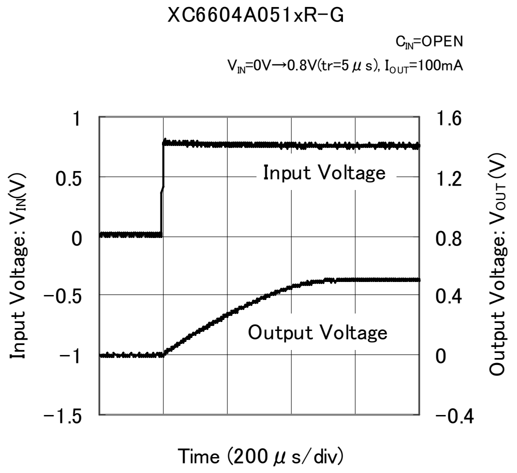
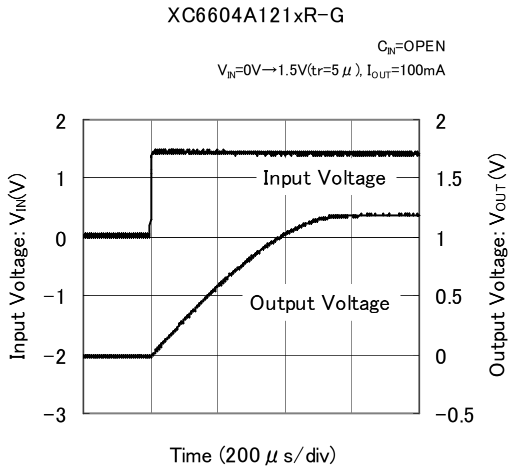


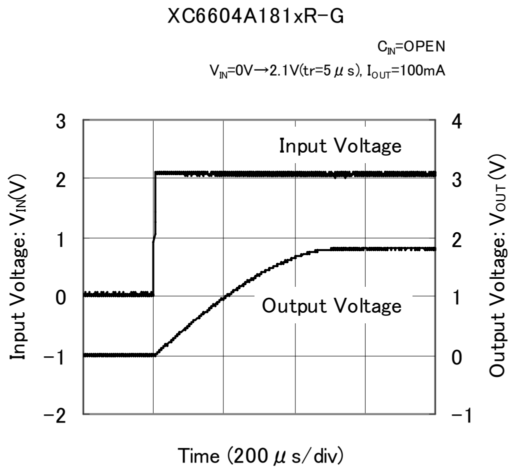
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin=V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

(16) Rising Response Time





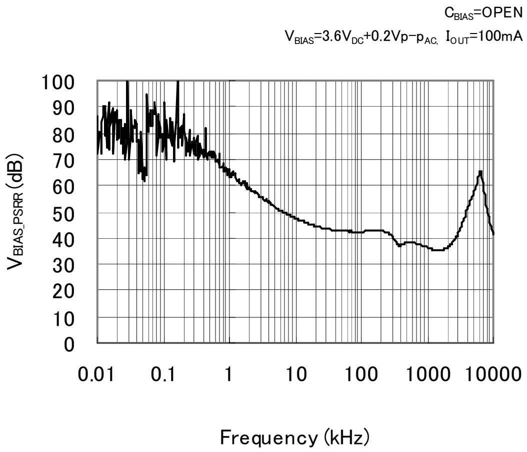


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

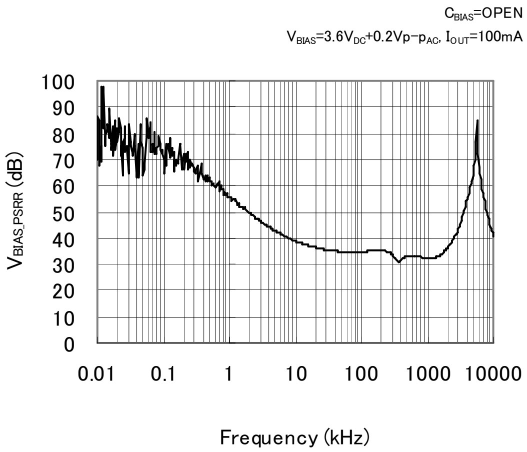
* Unless otherwise stated, $V_{BIAS}=V_{CE}=3.6V$, $V_{IN}=V_{OUT(T)}+0.3V$, $I_{OUT}=1mA$, I_{LIM} Pin=V_{SS}, $C_{BIAS}=C_{IN}=1.0\mu F$, $C_L=2.2\mu F$, Ta=25℃

(17) Bias Voltage Ripple Rejection Rate

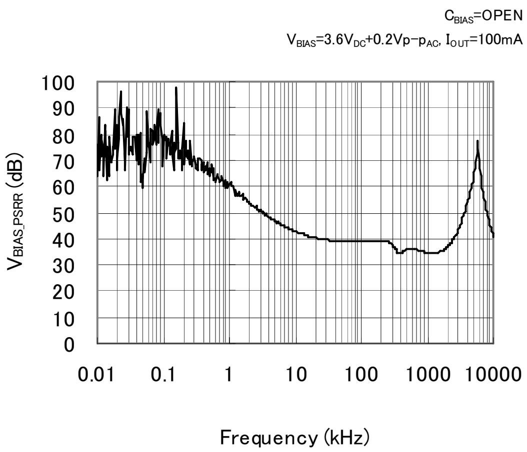
XC6604x051xR-G



XC6604x121xR-G

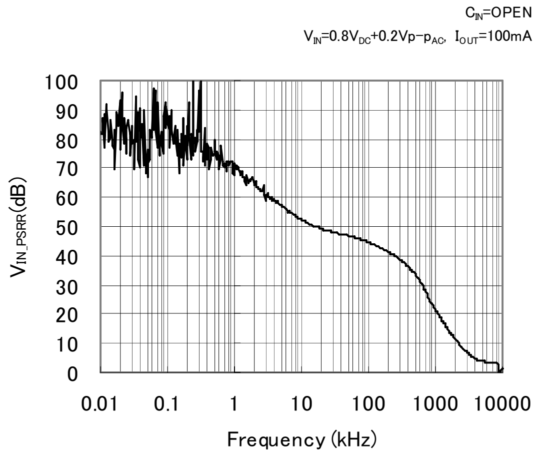


XC6604x181xR-G



(18) Input Voltage Ripple Rejection Rate

XC6604x051xR-G



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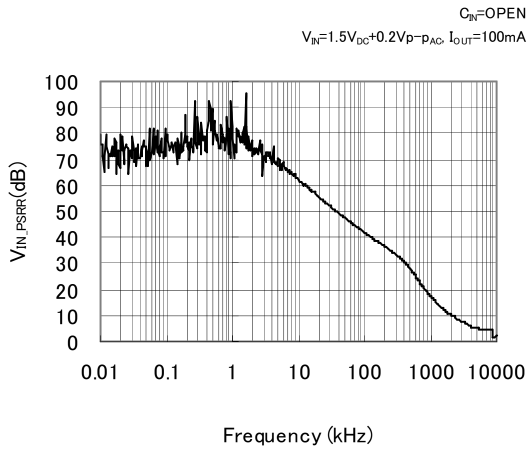

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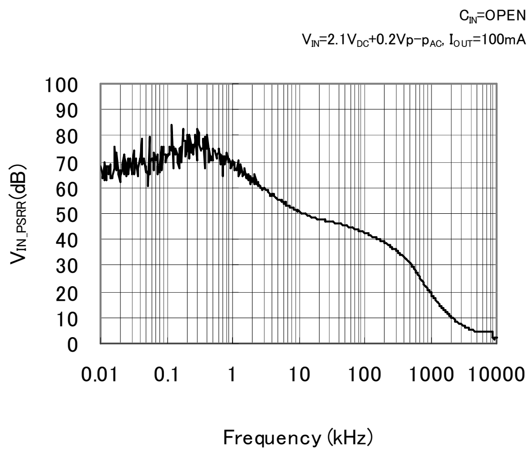
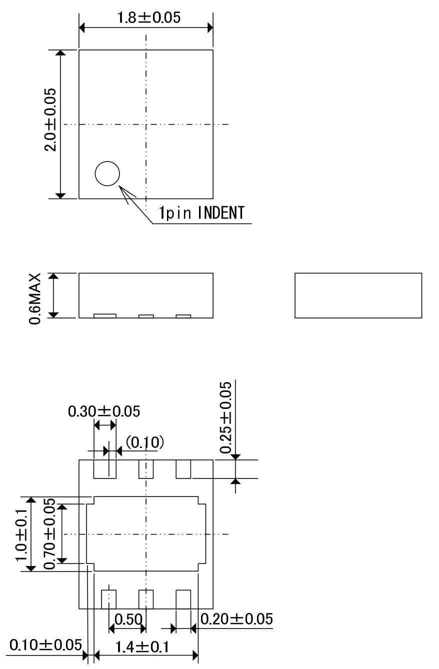
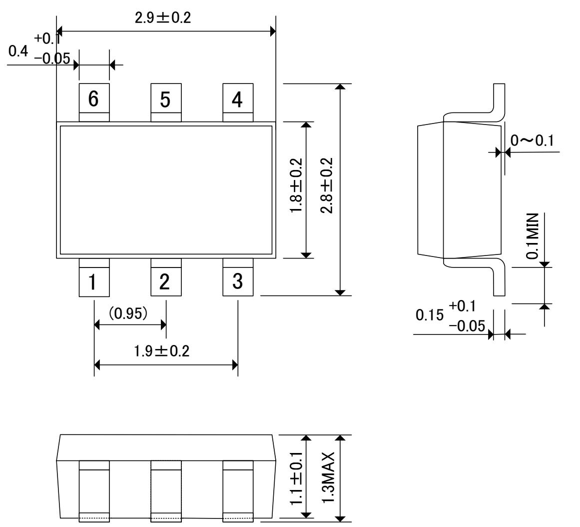


■PACKAGING INFORMATION

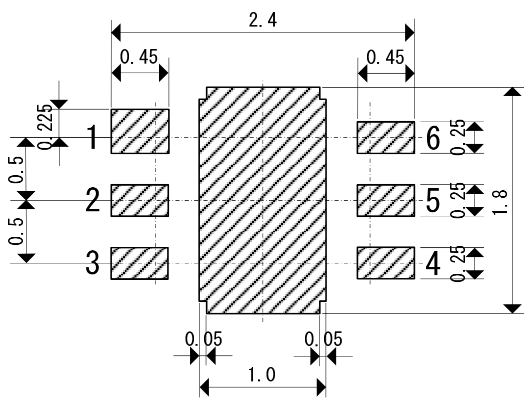
USP-6C
(unit : mm)



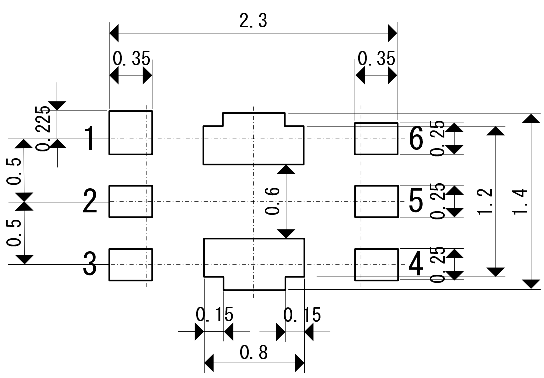
SOT-26W
(unit : mm)



●USP-6C Reference Pattern Layout (unit: mm)



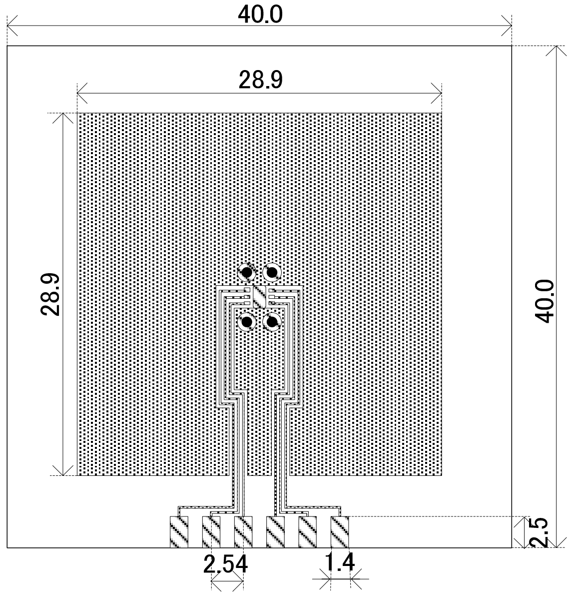
●USP-6C Reference Metal Mask Design (unit: mm)



■PACKAGING INFORMATION (Continued)

● USP-6C Power Dissipation

Power dissipation data for the USP-6C is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.



Evaluation Board (Unit: mm)

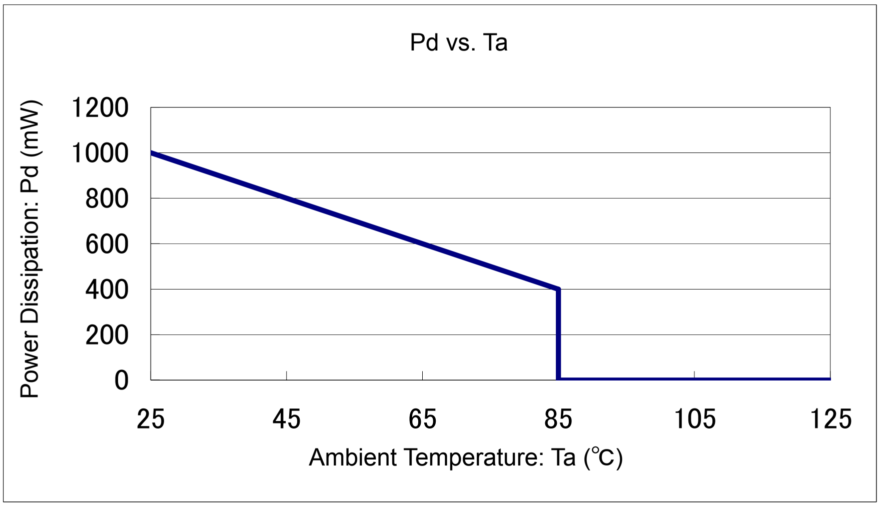
1. Measurement Condition (Reference data)

Condition: Mount on a board
Ambient: Natural convection
Soldering: Lead (Pb) free
Board: Dimensions 40 x 40 mm (1600 mm^2 in one side)
Copper (Cu) traces occupy 50% of the board area
In top and back faces
Package heat-sink is tied to the copper traces
Material: Glass Epoxy (FR-4)
Thickness: 1.6 mm
Through-hole: 4 x 0.8 Diameter

2. Power Dissipation vs. Ambient temperature

Board Mount (Tj max = 125℃)

Ambient Temperature（℃）	Power Dissipation Pd（mW）	Thermal Resistance (℃/W)
25	1000	100.00
85	400	



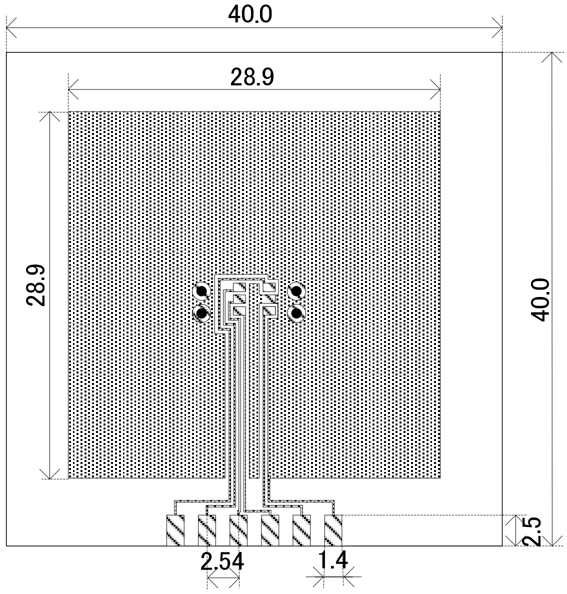
■PACKAGING INFORMATION (Continued)

● SOT-26W Power Dissipation

Power dissipation data for the SOT-26W is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

1. Measurement Condition (Reference data)

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40 x 40 mm (1600 mm^2 in one side) Copper (Cu) traces occupy 50% of the board area In top and back faces Package heat-sink is tied to the copper traces (Board of SOT-26 is used.)
Material:	Glass Epoxy (FR-4)
Thickness:	1.6 mm
Through-hole:	4 x 0.8 Diameter

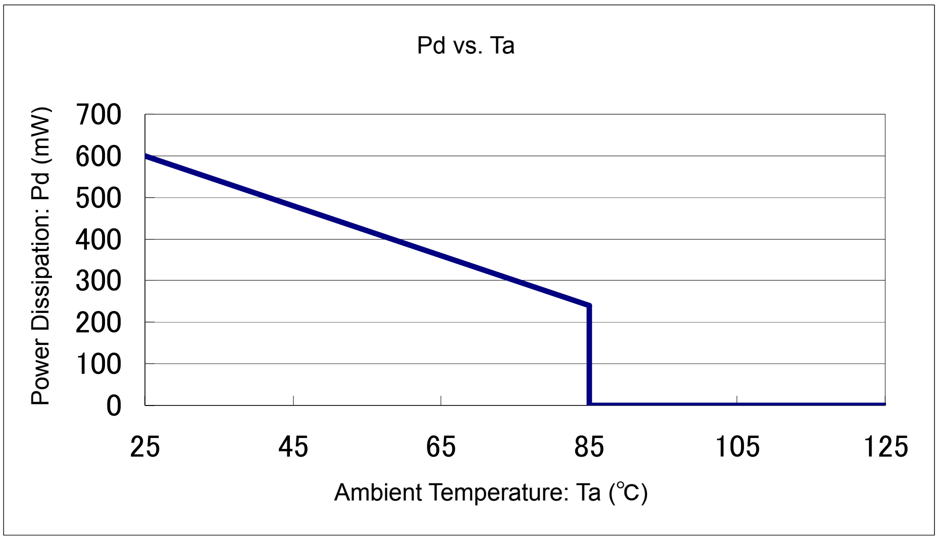


Evaluation Board (Unit: mm)

2. Power Dissipation vs. Ambient temperature

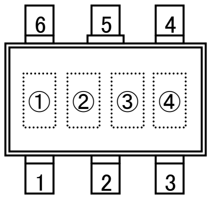
Board Mount (Tj max = 125℃)

Ambient Temperature（℃）	Power Dissipation Pd（mW）	Thermal Resistance (℃/W)
25	600	166.67
85	240	



■MARKING RULE

SOT-26W



① represents product series

MARK	PRODUCT SERIES
T	XC6604A*****-G
U	XC6604B*****-G

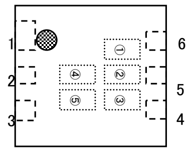
② represents output voltage

MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)
A	0.5	K	1.2
B	0.6	L	1.3
C	0.7	M	1.4
D	0.8	N	1.5
E	0.9	P	1.6
F	1.0	R	1.7
H	1.1	S	1.8

③④ represents production lot number
01 to 09, 0A to 0Z, 11 to 9Z, A1 to A9, AA to Z9, B1 to ZZ in order.
(G, I, J, O, Q, W excluded)
*No character inversion used.

■MARKING RULE (Continued)

USP-6C



① represents product series

MARK	PRODUCT SERIES
U	XC6604******-G

② represents regulator type

MARK	PRODUCT SERIES
A	XC6604A*****-G
B	XC6604B*****-G

③ represents output voltage

MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)
A	0.5	K	1.2
B	0.6	L	1.3
C	0.7	M	1.4
D	0.8	N	1.5
E	0.9	P	1.6
F	1.0	R	1.7
H	1.1	S	1.8

④⑤ represents production lot number
01 to 09, 0A to 0Z, 11 to 9Z, A1 to A9, AA to Z9, B1 to ZZ in order.
(G, I, J, O, Q, W excluded)
*No character inversion used.

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