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NTE74LS160A, NTE74LS161A, NTE74LS162A, NTE74LS163A
Integrated Circuit
TTL − Synchronous 4−Bit Counters

Description:

The NTE74LS160A thru NTE74LS163A are synchronous, presettable counters in a 16−Lead DIP type package that feature an internal carry look−ahead for application in high−speed counting designs. The NTE74LS160A and NTE74LS162A are decade counters and the NTE74LS161A and NTE74LS164A are 4−bit binary counters. Synchronous operation is provided by having all flip−flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count−enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip−flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the NTE74LS160A and NTE74LS161A is asynchronous and a low level at the clear input sets all four of the flip−flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function of the NTE74LS162A and NTE74LS163A is synchronous and a low level at the clear input sets all four flip−flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look−ahead circuitry provides for cascading counters for n−bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count−enable inputs and a ripple carry output. Both count−enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high−level output pulse with a duration approximately equal to the high−level portion of the Q_A output. This high−level overflow ripple carry pulse can be used to enable successively cascaded stages. Transitions at the enable P or T inputs of the NTE74LS160A thru NTE74LS163A are allowed regardless of the level of the clock input.

The NTE74LS160A thru NTE74LS163A feature a fully−independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features:

- Available in 4 Types:
  - Decade with Direct Clear: NTE74LS160A
  - Binary with Direct Clear: NTE74LS161A
  - Decade with Synchronous Clear: NTE74LS162A
  - Binary with Synchronous Clear: NTE74LS163A
- Internal Look−Ahead for Fast Counting
- Carry Output for n−Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode−Clamped Inputs

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Power Dissipation, P_D 93mW
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	–400	μA
Low−Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock Pulse	$t_{w(clock)}$	25	–	–	ns
Width of Clear Pulse	$t_{w(clear)}$	20	–	–	ns
Setup Time Data Inputs A, B, C, D	t_{su}	20	–	–	ns
ENP or ENT		20	–	–	ns
$\overline{\text{LOAD}}$		20	–	–	ns
$\overline{\text{LOAD}}$ Inactive State		20	–	–	ns
$\overline{\text{CLR}}$ (Note 2)		20	–	–	ns
$\overline{\text{CLR}}$ Inactive State		25	–	–	ns
Hold Time at Any Input	t_h	3	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Note 2. This applies only for NTE74LS162A and NTE74LS163A, which have synchronous clear inputs.

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −400μA	2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OL} = 4mA	–	0.25	0.4	V
		I_{OL} = 8mA	–	0.35	0.5	V
Input Current Data or ENP	I_I	V_{CC} = MAX, V_I = 7V	–	–	0.1	mA
$\overline{\text{LOAD}}$, CLK, or ENT			–	–	0.2	mA
$\overline{\text{CLR}}$ (’LS160A, ’LS161A)			–	–	0.1	mA
$\overline{\text{CLR}}$ (’LS162A, ’LS163A)			–	–	0.2	mA
High Level Input Current Data or ENP	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	20	μA
$\overline{\text{LOAD}}$, CLK, or ENT			–	–	40	μA
$\overline{\text{CLR}}$ (’LS160A, ’LS161A)			–	–	20	μA
$\overline{\text{CLR}}$ (’LS162A, ’LS163A)			–	–	40	μA
Low Level Input Current Data or ENP	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−0.4	mA
$\overline{\text{LOAD}}$, CLK, or ENT			–	–	−0.8	mA
$\overline{\text{CLR}}$ (’LS160A, ’LS161A)			–	–	−0.4	mA
$\overline{\text{CLR}}$ (’LS162A, ’LS163A)			–	–	−0.8	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5	−20	–	−100	mA
Supply Current, All Outputs High	I_{CCH}	V_{CC} = MAX, Note 6	–	18	31	mA
Supply Current, All Outputs Low	I_{CCL}	V_{CC} = MAX, Note 7	–	19	32	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 5. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 6. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

Note 7. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 2kΩ, C_L = 15pF, Note 8	25	32	–	MHz
Propagation Delay Time (From CLK Input to RCO Output)	t_{PLH}		–	20	35	ns
	t_{PHL}		–	18	35	ns
Propagation Delay Time (From CLK Input to Any Output)	t_{PLH}		–	13	24	ns
(From $\overline{\text{LOAD}}$ Input High to Q Output)	t_{PHL}		–	18	27	ns

Note 8. .Propagation delay for clearing is measure from the clear input for the NTE74LS160A and NTE74LS161A or from the clock transition for the NTE74LS162A and NTE74LS163A.

Switching Characteristic (Cont'd)s: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From CLK Input to Any Output)	t_{PLH}	R_L = 2kΩ, C_L = 15pF, Note 8	–	13	24	ns
(From $\overline{\text{LOAD}}$ Input Low to Q Output)	t_{PHL}		–	18	27	ns
Propagation Delay Time (From ENT Input to RCO Output)	t_{PLH}		–	9	14	ns
	t_{PHL}		–	9	14	ns
Propagation Delay Time (From $\overline{\text{CLR}}$ Input to Any Q Output)	t_{PLL}		–	20	28	ns

Note 8. .Propagation delay for clearing is measure from the clear input for the NTE74LS160A and NTE74LS161A or from the clock transition for the NTE74LS162A and NTE74LS163A.

Pin Connection Diagram