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NTE4027B & NTE4027BT Integrated Circuit CMOS, Dual J-K Flip-Flop

Description:

The NTE4027B (16-Lead DIP) and NTE4027BT (SOIC-16) dual J-K flip-flops have independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design —
 Logic State is retained Indefinitely with Clock Level either High or Low; Information is Transferred to the Output Only on the Positive-Going Edge of the Clock Pulse
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	-0.5 to +18.0V
Input Voltage (DC or Transient), V_{in}	-0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out}	-0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in}	± 10 mA
Output Current (DC or Transient, Per Pin), I_{out}	± 10 mA
Power Dissipation (Per Package), P_D	500mW
Temperature Derating (from +65° to +125°C)	-7.0mW/°C
Storage Temperature, T_{stg}	-65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L	+260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2)

Parameter	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0 "1" Level $V_{in} = 0$ or V_{DD}	V_{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	Vdc
		15	-	0.05	-	0	0.05	-	0.05	Vdc
	V_{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	Vdc
		15	14.95	-	14.95	15	-	14.95	-	Vdc
Input Voltage "0" Level ($V_O = 4.5$ or $0.5V_{dc}$) ($V_O = 9.0$ or $1.0V_{dc}$) ($V_O = 13.5$ or $1.5V_{dc}$) "1" Level ($V_O = 0.5$ or $4.5V_{dc}$) ($V_O = 1.0$ or $9.0V_{dc}$) ($V_O = 1.5$ or $13.5V_{dc}$)	V_{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	Vdc
		15	-	4.0	-	6.75	4.0	-	4.0	Vdc
	V_{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	Vdc
		15	11.0	-	11.0	8.25	-	11.0	-	Vdc
Output Drive Current Source ($V_{OH} = 2.5V_{dc}$) ($V_{OH} = 4.6V_{dc}$) ($V_{OH} = 9.5V_{dc}$) ($V_{OH} = 13.5V_{dc}$) Sink ($V_{OL} = 0.4V_{dc}$) ($V_{OL} = 0.5V_{dc}$) ($V_{OL} = 1.5V_{dc}$)	I_{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	mAdc
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	mAdc
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	mAdc
	I_{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	mAdc
15		4.2	-	3.4	8.8	-	2.4	-	mAdc	
Input Current	I_{in}	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 0.1	μ Adc
Input Capacitance ($V_{IN} = 0$)	C_{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I_{DD}	5.0	-	1.0	-	0.002	1.0	-	30	μ Adc
		10	-	2.0	-	0.004	2.0	-	60	μ Adc
		15	-	4.0	-	0.006	4.0	-	120	μ Adc
Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L = 50pF$ on all outputs, all buffers switching, Note 3, Note 4)	I_T	5.0	$I_T = (0.8\mu A/kHz) f + I_{DD}$							μ Adc
		10	$I_T = (1.6\mu A/kHz) f + I_{DD}$							μ Adc
		15	$I_T = (2.4\mu A/kHz) f + I_{DD}$							μ Adc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.







Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2)

Parameter	Symbol	V _{DD} Vdc	Min	Typ	Max	Unit		
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5\text{ns/pf}) C_L + 25\text{ns}$ $t_{TLH}, t_{THL} = (0.75\text{ns/pf}) C_L + 12.5\text{ns}$ $t_{TLH}, t_{THL} = (0.55\text{ns/pf}) C_L + 9.5\text{ns}$	$t_{TLH},$ t_{THL}	5.0	–	100	200	ns		
		10	–	50	100	ns		
		15	–	40	80	ns		
Propagation Delay Time Clock to Q, Q $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 90\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 42\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 25\text{ns}$ Set to Q, Q $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 90\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 42\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 25\text{ns}$ Reset to Q, Q $t_{PLH}, t_{PHL} = (1.7\text{ns/pf}) C_L + 265\text{ns}$ $t_{PLH}, t_{PHL} = (0.66\text{ns/pf}) C_L + 67\text{ns}$ $t_{PLH}, t_{PHL} = (0.5\text{ns/pf}) C_L + 50\text{ns}$	$t_{PLH},$ t_{PHL}	5.0	–	175	350	ns		
		10	–	75	150	ns		
		15	–	50	100	ns		
		5.0	–	175	350	ns		
		10	–	75	150	ns		
		15	–	50	100	ns		
		5.0	–	350	450	ns		
		10	–	100	200	ns		
		15	–	75	150	ns		
		Setup Times	t_{su}	5.0	140	70	–	ns
				10	50	25	–	ns
				15	35	17	–	ns
Hold Times	t_h	5.0	140	70	–	ns		
		10	50	25	–	ns		
		15	35	17	–	ns		
Clock Pulse Width	$t_{WH},$ t_{WL}	5.0	330	165	–	ns		
		10	110	55	–	ns		
		15	75	38	–	ns		
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz		
		10	–	9.0	4.5	MHz		
		15	–	13.0	6.5	MHz		
Clock Pulse Rise and Fall Time	$t_{TLH},$ t_{THL}	5.0	–	–	15	μs		
		10	–	–	5.0	μs		
		15	–	–	4.0	μs		
Removal Times Set Reset	t_{rem}	5.0	90	10	–	ns		
		10	45	5	–	ns		
		15	35	3	–	ns		
		5.0	50	–30	–	ns		
		10	25	–15	–	ns		
		15	20	–10	–	ns		
Set and Reset Pulse Width	t_{WH}	5.0	250	125	–	ns		
		10	100	50	–	ns		
		15	70	35	–	ns		

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

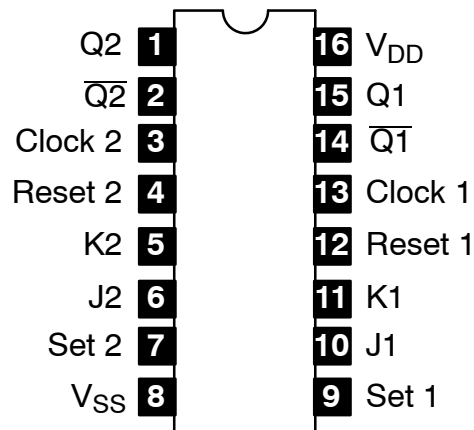
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

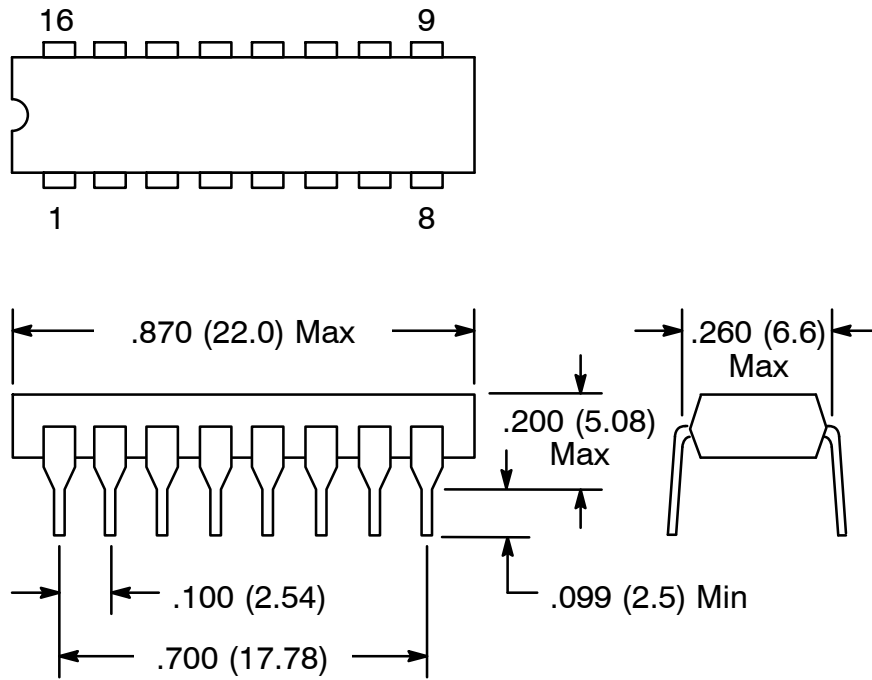
Inputs						Outputs *	
$C \dagger$	J	K	S	R	$Q_n \ddagger$	Q_{n+1}	$\overline{Q_{n+1}}$
	1	X	0	0	0	1	0
	X	0	0	0	1	1	0
	0	X	0	0	0	0	1
	X	1	0	0	1	0	1
	1	1	0	0	Q_0	$\overline{Q_0}$	Q_0
	X	X	0	0	X	Q_n	$\overline{Q_n}$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

X = Don't Care
 † = Level Change
 ‡ = Present State
 * = Next State

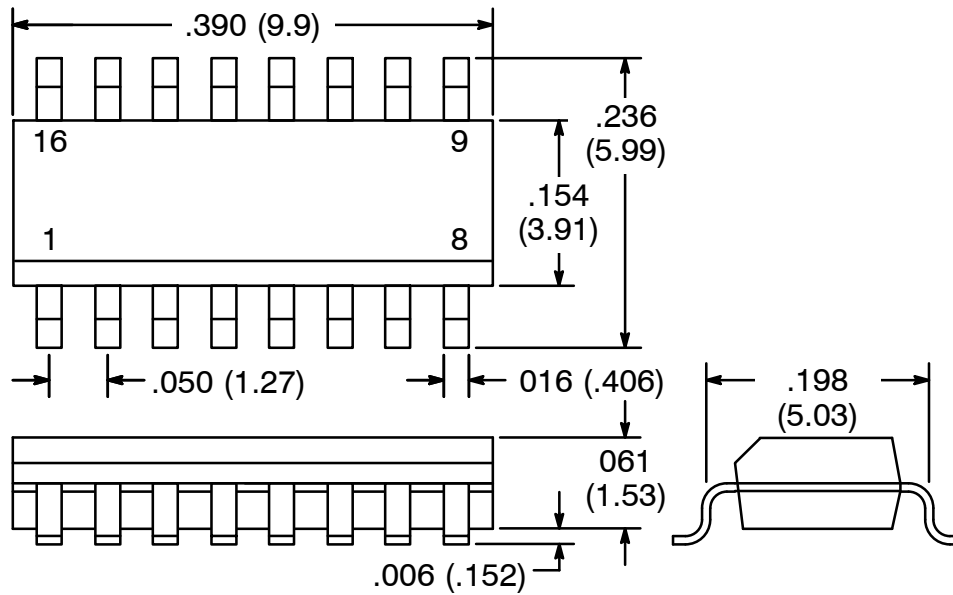
Pin Connection Diagram



NTE4027B



NTE4027BT



NOTE: Pin1 on Beveled Edge