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# HD74HC4024

# 7-stage Binary Counter

REJ03D0325-0300 Rev.3.00 Mar 30, 2006

### **Description**

The HD74HC4024 is a 7-stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input.

#### **Features**

• High Speed Operation:  $t_{pd}$  (Clock to  $Q_1$ ) = 14 ns typ ( $C_L = 50 \text{ pF}$ )

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage:  $V_{CC} = 2$  to 6 V

• Low Input Current: 1 μA max

• Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max (Ta = 25°C)

• Ordering Information

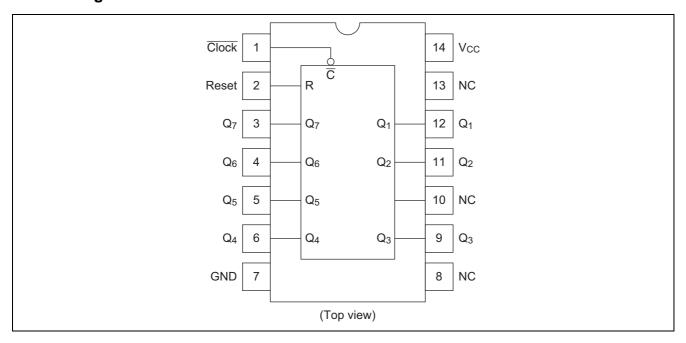
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	
HD74HC4024P	074HC4024P DILP-14 pin		D		
1107411040241	DILI -14 PIII	(DP-14AV)	r		
HD74HC4024FPEL SOP-14 pin (JEITA)		PRSP0014DF-B	FP	EL (2,000 pcs/reel)	
TID7411C4024FFEL	30F-14 pill (JETTA)	(FP-14DAV)	ГГ	EL (2,000 pcs/reel)	
HD74HC4024RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A	RP	EL (2,500 pcs/reel)	
11D1411C4024RFEL	SOF-14 PIII (JEDEC)	(FP-14DNV)	NF		

Note: Please consult the sales office for the above package availability.

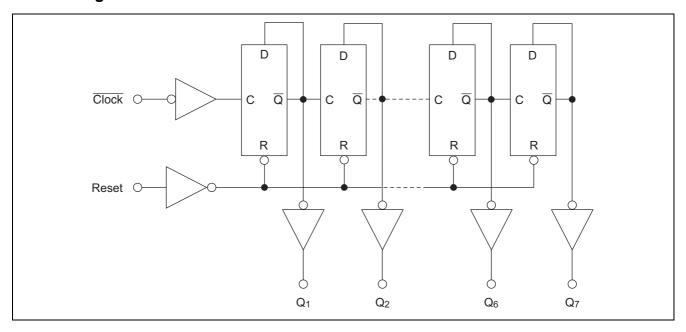
#### **Function Table**

Clock	Reset	Outputs State
L	L	No change
L	Н	All outputs are low
Н	L	No change
Н	Н	All outputs are low
_	L	No change
_	Н	All outputs are low
	L	Advance to next state
	Н	All outputs are low

## **Pin Arrangement**



## **Block Diagram**



### **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
Input / Output voltage	V <sub>IN</sub> , V <sub>OUT</sub>	–0.5 to V <sub>CC</sub> +0.5	V
Input / Output diode current	I <sub>IK</sub> , I <sub>OK</sub>	±20	mA
Output current	I <sub>OUT</sub>	±25	mA
V <sub>CC</sub> , GND current	I <sub>CC</sub> or I <sub>GND</sub>	±50	mA
Power dissipation	P <sub>T</sub>	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## **Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to V <sub>CC</sub>	V	
Operating temperature	Та	-40 to 85	°C	
		0 to 1000		V <sub>CC</sub> = 2.0 V
Input rise / fall time*1	$t_r, t_f$	0 to 500	ns	$V_{CC} = 4.5 \text{ V}$
		0 to 400		V <sub>CC</sub> = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

#### **DC Characteristics**

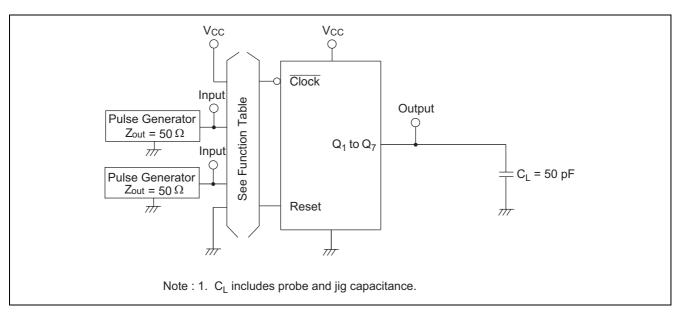
Item	Symbol	V <sub>cc</sub> (V)	T	a = 25°	С	Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Тур	Max	Min	Max			
Input voltage	V <sub>IH</sub>	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	_	_	3.15	_			
		6.0	4.2	_	_	4.2	_			
	V <sub>IL</sub>	2.0		1	0.5	_	0.5	V		
		4.5		1	1.35	_	1.35			
		6.0	_	_	1.8	_	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	_	1.9	_	V	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu A$
		4.5	4.4	4.5	_	4.4	_			
		6.0	5.9	6.0	_	5.9	_			
		4.5	4.18	_	_	4.13	_			$I_{OH} = -4 \text{ mA}$
		6.0	5.68	_	_	5.63	_			$I_{OH} = -5.2 \text{ mA}$
	V <sub>OL</sub>	2.0	_	0.0	0.1	_	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu A$
		4.5	_	0.0	0.1	_	0.1			
		6.0	_	0.0	0.1	_	0.1			
		4.5	_	_	0.26	_	0.33			$I_{OL} = 4 \text{ mA}$
		6.0	_	_	0.26	_	0.33			$I_{OL} = 5.2 \text{ mA}$
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V <sub>CC</sub> or GN	ID
Quiescent supply current	I <sub>CC</sub>	6.0	_	_	4.0	_	40	μΑ	$Vin = V_{CC} \text{ or } GN$	ID, lout = $0 \mu A$

### **AC Characteristics**

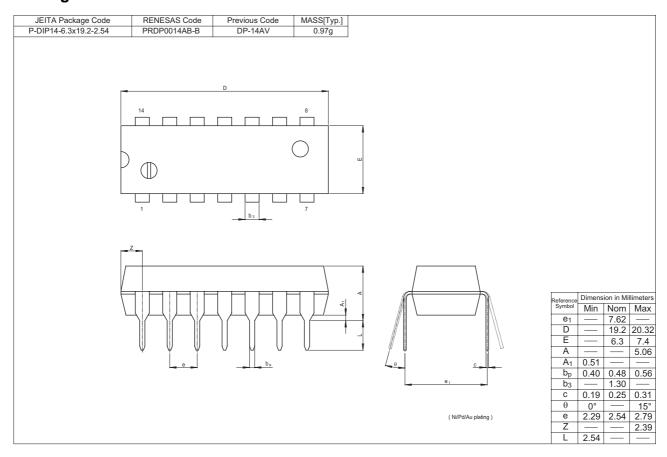
( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

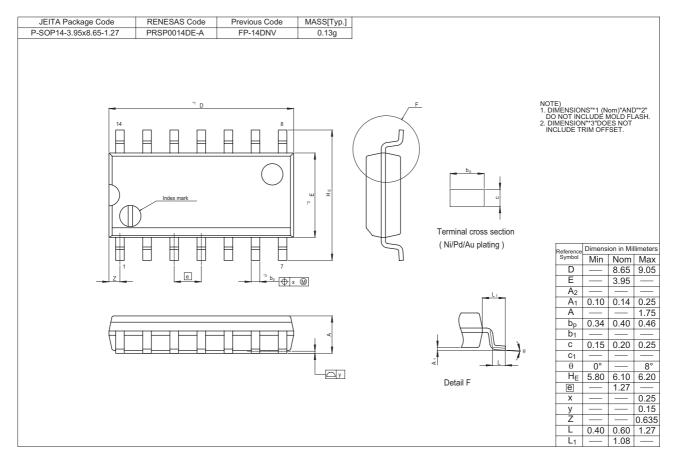
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Тур	Max	Min	Max		
Maximum clock frequency	$f_{\text{max}}$	2.0	_	_	5	_	4	MHz	
		4.5	1	_	25	_	20		
		6.0		_	29	_	24		
Propagation delay time	t <sub>PLH</sub>	2.0	_	_	185	_	230	ns	Clock to Q <sub>1</sub>
		4.5	_	14	37	_	46		
		6.0	_	_	31	_	39		
	t <sub>PHL</sub>	2.0	_	_	185	_	230	ns	Clock to Q <sub>1</sub>
		4.5	_	14	37	_	46		
		6.0	_	_	31	_	39		
	t <sub>PHL</sub>	2.0	_	_	185	_	230	ns	Reset to output
		4.5	_	13	37	_	46		
		6.0	_	_	31	_	39		
Removal time	$t_{rem}$	2.0	100	_	_	125	_	ns	
		4.5	20	0	_	25	_		
		6.0	17	_	_	21	_		
Pulse width	t <sub>w</sub>	2.0	80	_	_	100	_	ns	
		4.5	16	4	_	20	_		
		6.0	14	_	_	17	_		
Output rise/fall time	t <sub>TLH</sub>	2.0	_	_	75	_	95	ns	
	t <sub>THL</sub>	4.5	1	5	15	_	19		
		6.0	_	_	13	_	16		
Input capacitance	Cin		_	5	10	_	10	pF	

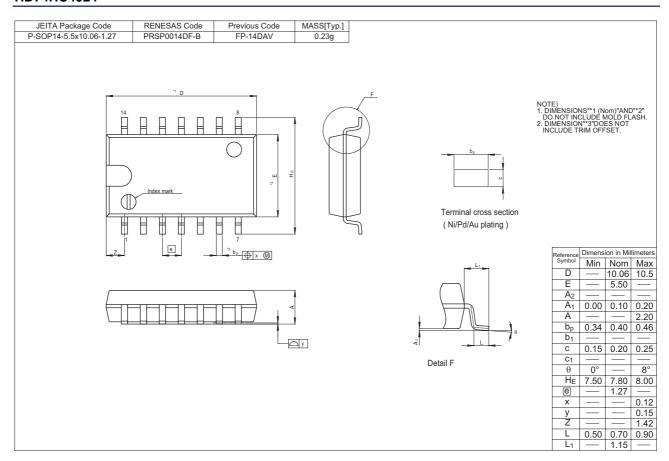
### **Test Circuit**



### **Package Dimensions**







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