

# 8-Bit Up/Down Counter

## SN54/74LS469A

74LS469A

### Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMA-controller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments

### Description

The 'LS469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ( $\overline{LD}$ ,  $\overline{UD}$ ,  $\overline{CBI}$ ) provide one of four operations which occur synchronously on the rising edge of the clock ( $CK$ ).

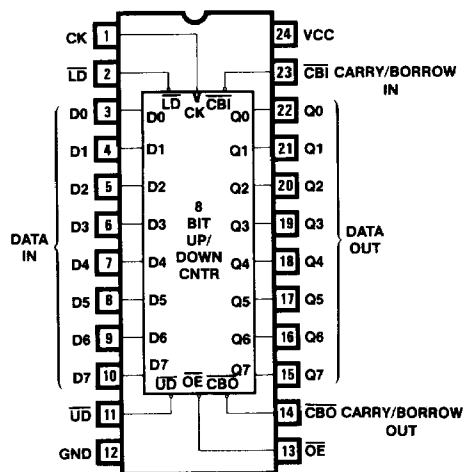
The LOAD operation loads the inputs ( $D7-D0$ ) into the output register ( $Q7-Q0$ ). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ( $\overline{CBI} = \text{LOW}$ ), and the up/down control line ( $\overline{UD}$ ) is LOW, otherwise the operation is a HOLD. The carry-out ( $\overline{CBO}$ ) is TRUE ( $\overline{CBO} = \text{LOW}$ ) when the output register ( $Q7-Q0$ ) is all HIGHS, otherwise FALSE ( $\overline{CBO} = \text{HIGH}$ ). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ( $\overline{CBI} = \text{LOW}$ ), and the up/down control line ( $\overline{UD}$ ) is HIGH, otherwise the operation is a HOLD. The borrow-out ( $\overline{CBO}$ ) is TRUE ( $\overline{CBO} = \text{LOW}$ ) when the output register ( $Q7-Q0$ ) is all LOWs, otherwise FALSE ( $\overline{CBO} = \text{HIGH}$ ).

The data output pins are enabled when  $\overline{OE}$  is LOW, and disabled (HI-Z) when  $\overline{OE}$  is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469A 8-bit up/down counters may be cascaded to provide larger counters.

### Ordering Information

| PART NUMBER | PACKAGE    | TEMPERATURE |
|-------------|------------|-------------|
| SN54LS469A  | JS, W, 28L | Mil         |
| SN74LS469A  | NS, JS     | Com         |

### Logic Symbol



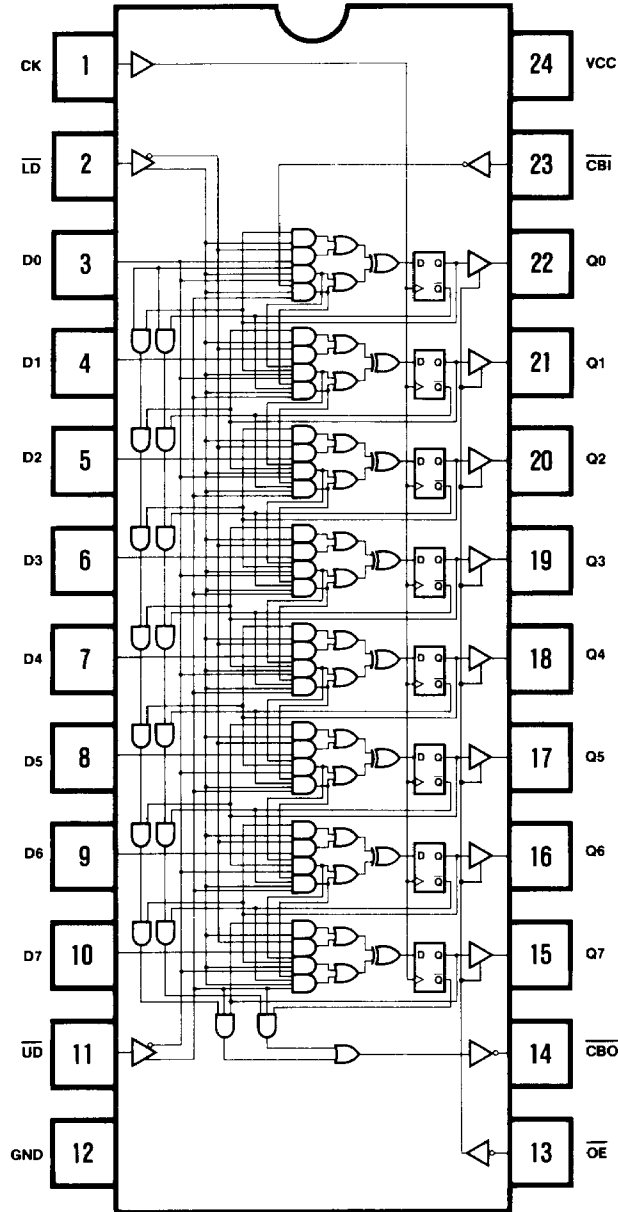
### Function Table

| $\overline{OE}$ | $CK$ | $\overline{LD}$ | $\overline{UD}$ | $\overline{CBI}$ | $D7-D0$ | $Q7-Q0$   | OPERATION |
|-----------------|------|-----------------|-----------------|------------------|---------|-----------|-----------|
| H               | *    | *               | *               | *                | *       | Z         | HI-Z*     |
| L               | ↑    | L               | X               | X                | D       | D         | LOAD      |
| L               | ↑    | H               | L               | H                | X       | Q         | HOLD      |
| L               | ↑    | H               | L               | L                | X       | Q plus 1  | INCREMENT |
| L               | ↑    | H               | H               | H                | X       | Q         | HOLD      |
| L               | ↑    | H               | H               | L                | X       | Q minus 1 | DECREMENT |

\* When  $\overline{OE}$  is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Logic Diagram

8-Bit Up/Down Counter



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### Absolute Maximum Ratings

|                                |                |
|--------------------------------|----------------|
| Supply voltage $V_{CC}$ .....  | 7.0 V          |
| Input voltage .....            | 5.5 V          |
| Off-state output voltage ..... | 5.5 V          |
| Storage temperature .....      | -65° to +150°C |

### Operating Conditions

| SYMBOL   | PARAMETER                      | MILITARY |      |      | COMMERCIAL |      |      | UNIT |
|----------|--------------------------------|----------|------|------|------------|------|------|------|
|          |                                | MIN      | TYP† | MAX  | MIN        | TYP† | MAX  |      |
| $V_{CC}$ | Supply voltage                 | 4.5      | 5    | 5.5  | 4.75       | 5    | 5.25 | V    |
| $T_A$    | Operating free-air temperature | -55      |      | 125* | 0          |      | 75   | °C   |
| $t_w$    | Width of clock                 | Low      | 35   | 15   | 25         | 15   |      | ns   |
|          |                                | High     | 20   | 7    | 15         | 7    |      |      |
| $t_{su}$ | Setup time                     | 40       | 20   |      | 30         | 20   |      | ns   |
| $t_h$    | Hold time                      | 0        | -15  |      | 0          | -15  |      |      |

\* Case temperature

### Electrical Characteristics Over Operating Conditions

| SYMBOL        | PARAMETER                     | TEST CONDITIONS   |                        | MIN                        | TYP† | MAX  | UNIT          |    |
|---------------|-------------------------------|---|------------------------|----------------------------|------|------|---------------|----|
| $V_{IL}^{**}$ | Low-level input voltage       |   |                        |                            |      | 0.8  | V             |    |
| $V_{IH}^{**}$ | High-level input voltage      |   |                        | 2                          |      |      | V             |    |
| $V_{IC}$      | Input clamp voltage           | $V_{CC} = \text{MIN}$   | $I_I = -18 \text{ mA}$ | -0.8                       | -1.5 |      | V             |    |
| $I_{IL}$      | Low-level input current       | $V_{CC} = \text{MAX}$   | $V_I = 0.4 \text{ V}$  | -0.02                      | 0.25 |      | mA            |    |
| $I_{IH}$      | High-level input current      | $V_{CC} = \text{MAX}$   | $V_I = 2.4 \text{ V}$  |                            | 25   |      | $\mu\text{A}$ |    |
| $I_I$         | Maximum input current         | $V_{CC} = \text{MAX}$   | $V_I = 5.5 \text{ V}$  |                            | 1    |      | mA            |    |
| $V_{OL}$      | Low-level output voltage      | $V_{CC} = \text{MIN}$<br>$V_{IL} = 0.8 \text{ V}$<br>$V_{IH} = 2 \text{ V}$ | Mil                    | $I_{OL} = 12 \text{ mA}$   | 0.3  | 0.5  | V             |    |
|               |                               |   | Com                    | $I_{OL} = 24 \text{ mA}$   |      |      |               |    |
| $V_{OH}$      | High-level output voltage     | $V_{CC} = \text{MIN}$<br>$V_{IL} = 0.8 \text{ V}$<br>$V_{IH} = 2 \text{ V}$ | Mil                    | $I_{OH} = -2 \text{ mA}$   | 2.4  | 2.8  | V             |    |
|               |                               |   | Com                    | $I_{OH} = -3.2 \text{ mA}$ |      |      |               |    |
| $I_{OZL}$     | Off-state output current      | $V_{CC} = \text{MAX}$<br>$V_{IL} = 0.8 \text{ V}$<br>$V_{IH} = 2 \text{ V}$ |                        | $V_O = 0.4 \text{ V}$      |      | -100 | $\mu\text{A}$ |    |
| $I_{OZH}$     |                               |   |                        | $V_O = 2.4 \text{ V}$      |      | 100  |               |    |
| $I_{OS}$      | Output short-circuit current* | $V_{CC} = 5.0 \text{ V}$  |                        | $V_O = 0 \text{ V}$        | -30  | -70  | -130          | mA |
| $I_{CC}$      | Supply current                | $V_{CC} = \text{MAX}$   |                        |                            | 140  | 180  |               | mA |

\* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

\*\*  $V_{IL}$  and  $V_{IH}$  parameters are, in effect, input conditions of D.C. and functional output tests are not directly tested.  $V_{IL}$  is specified at  $\leq 0.8 \text{ V}$  and  $V_{IH}$  is specified at  $\geq 2.0 \text{ V}$ . † All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

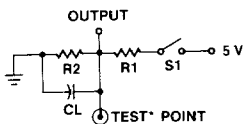
### Switching Characteristics Over Operating Conditions

| SYMBOL    | PARAMETER                | TEST CONDITIONS<br>(See Test Load/Waveforms) | MILITARY |      |     | COMMERCIAL |      |     | UNIT |
|-----------|--------------------------|--|----------|------|-----|------------|------|-----|------|
|           |                          |  | MIN      | TYP† | MAX | MIN        | TYP† | MAX |      |
| $f_{MAX}$ | Maximum clock frequency* | Commercial                                   | 16.6     |      |     | 25         |      |     | MHz  |
| $t_{PD}$  | CI to CO delay           | $R_1 = 200 \Omega$                           |          | 15   | 35  |            | 15   | 25  | ns   |
| $t_{CLK}$ | Clock to Q               | $R_2 = 390 \Omega$                           |          | 10   | 25  |            | 10   | 15  | ns   |
| $t_{PD}$  | Clock to CO              | Military                                     |          | 25   | 60  |            | 25   | 40  | ns   |
| $t_{PZX}$ | Output enable delay      | $R_1 = 390 \Omega$                           |          | 11   | 25  |            | 11   | 20  | ns   |
| $t_{PXZ}$ | Output disable delay     | $R_2 = 750 \Omega$                           |          | 10   | 25  |            | 10   | 20  | ns   |

\*  $f_{MAX}$  is derived from:  $1/\text{MAX} [(t_{su} + t_h) \cdot t_w(\text{Low}) + t_w(\text{High}) \cdot t_{CLK}]$ .

### Test Load

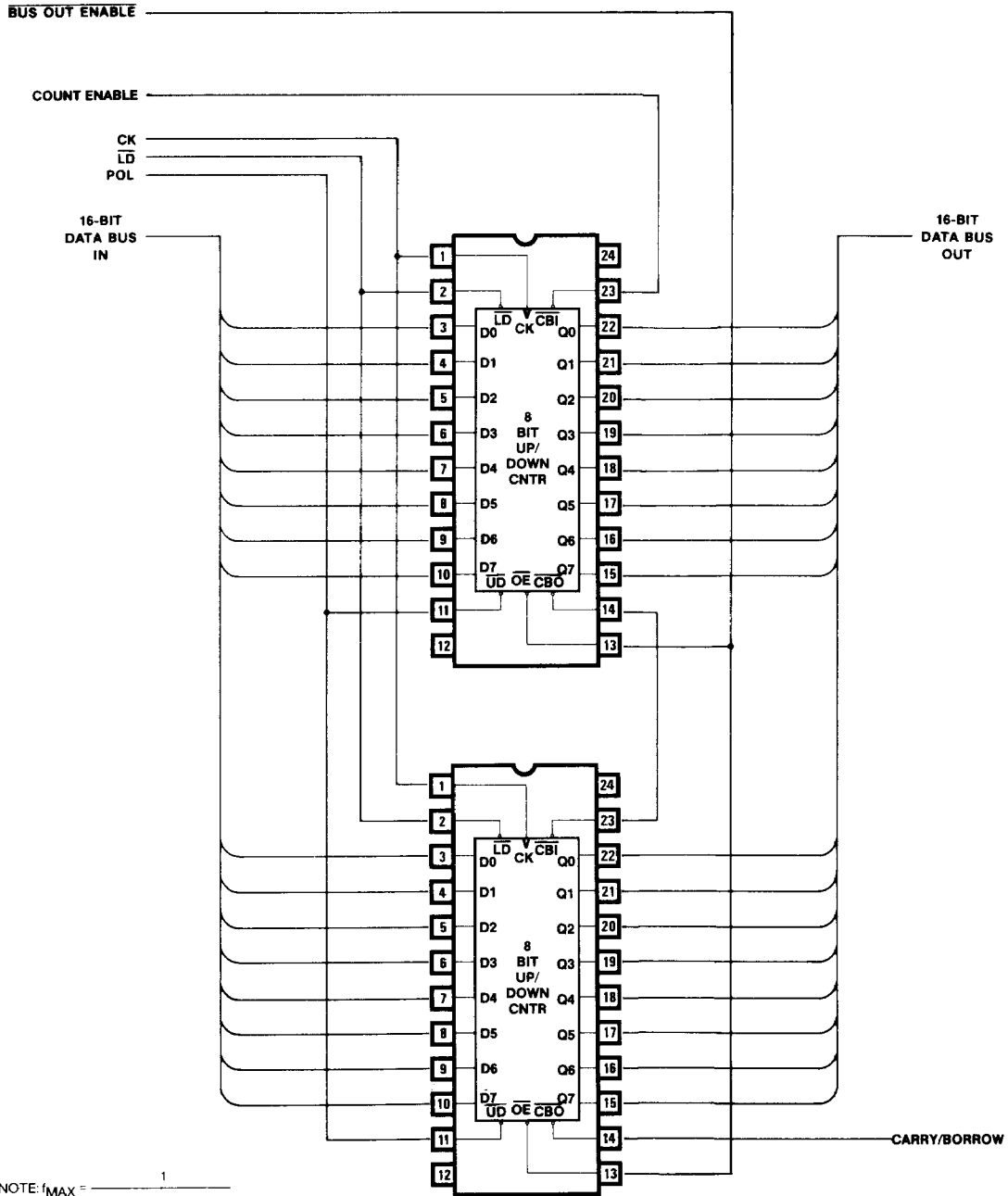
\* The "Test Point" is driven by the outputs under test, and observed by instrumentation



- Notes:
- $t_{PD}$  is tested with switch  $S_1$  closed.  $C_L = 50 \text{ pF}$  and measured at 1.5 V output level.
  - $t_{PZX}$  is measured at the 1.5 V output level with  $C_L = 50 \text{ pF}$ .  $S_1$  is open for high impedance to "1" test, and closed for high impedance to "0" test.
  - $t_{PXZ}$  is tested with  $C_L = 5 \text{ pF}$ .  $S_1$  is open for "1" to high impedance test, measured at  $V_{OH} = 0.5 \text{ V}$  output level;  $S_1$  is closed for "0" to high impedance test measured at  $V_{OL} = 0.5 \text{ V}$  output level.

Application

16-Bit Up/Down Counter



NOTE:  $t_{MAX} = \frac{1}{f_{PD,CLK TO CO} + f_{SU}}$

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